COMMUNICATIONS

IC Handbook

GEC PLESSEY

SEMICONDUCTORS

Foreword

GEC Plessey Semiconductors (GPS) has a world-class reputation for ICs for radio frequency applications. GPS offer state-of-the-art ICs for cellular and cordless phones, cellular and cordless infrastucture, and pagers.

Originally supplying a range of radio parts such as amplifiers, synthesisers and prescalers, GPS has developed and enhanced its technologies to suit much higher system integration, and now offers some of the most advanced integrated circuits available. Today, GPS provides cost effective, high performance solutions for tomorrow's handheld radios, and even credit card sized pagers, with their emphasis on reduced size and minimum power consumption (to increase battery life).

GPS is one of very few companies with the complete range of semiconductor technology for the integration of a radio system:

- leading edge RF bipolar technologies with on-chip capacitors and inductors
- mixed signal CMOS for RF/IF (intermediate frequency) and voice processing and coding
- digital CMOS with a library of advanced functions such as the Pine and Oak DSPs and the ARM 32bit RISC microprocessor
- SAW Filter technology
- advanced packaging techniques.

With these, and with many years experience of implementing systems on silicon, GPS is ideally placed to support your IC requirements in the radio frequency arena.

This latest Communications Handbook details some of the latest developments in chipsets for analog cellular systems and for advanced pagers. It also introduces a wide range of Surface Acoustic Wave - SAW - Filters for digital cellular (such as GSM and PCS) and digital cordless (such as DECT) applications. Take a look at what's in there and give us a call !

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Product List - alpha numeric

Section 1

PLLs (Phased Lock Loop)

GEC PLESSEY

SEMICONDUCTORS

NJ88C33

FREQUENCY SYNTHESISER (I²C BUS PROGRAMMABLE) WITH CURRENT SOURCE PHASE DETECTOR OUTPUTS

The NJ88C33 is a synthesiser circuit fabricated on GPS's 1.4 micron CMOS process, assuring very high performance. It is I²C compatible and can also be programmed at up to 5MHz. It contains a 16-bit R counter, a 12-bit N counter and a 7-bit A counter.

A digital phase comparator gives improved loop stability with current source outputs to reduce loop components. A voltage doubler is provided for the loop driver to improve control voltage range to the VCO when operating at low supply voltages.

FEATURES

- Easy to Use
- Low Power Consumption (15mW)
- Single Supply 2.5V to 5.5V
- Digital Phase Comparator with Current Source Outputs
- Serial (I²C Compatible) Programming, 5MHz max
- Channel Loading in 8µs
- 150MHz Input Frequency Without Prescaler at 4.5V (52MHz at 2.7V)
- Standby Modes
- Use of Two-Modulus Prescaler is Possible

APPLICATIONS

- Cordless Telephones (CT2, DECT)
- Cellular Telephones (GSM, PCN, ETACS)
- Hand Held Marine Radios
- Sonarbuoys
- Video Clock generators

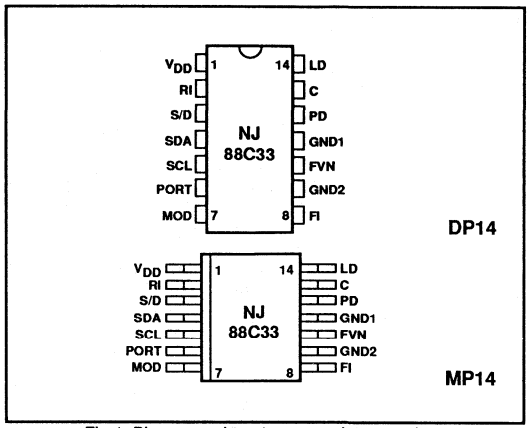


Fig.1 Pin connections (not to scale) - top views

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	-0.3V to 7V
Input voltage, V_{IM1}	-0.3 to V_{DD} +0.3V
Output voltage on pin 13, V_{IM2}	$-V_{DD}$ to 0V
Storage temperature, T_{stg}	-55°C to +125°C

ORDERING INFORMATION

NJ88C33 MA DP (Industrial - Plastic DIL package)
NJ88C33 MA MP (Industrial - Miniature Plastic DIL package)

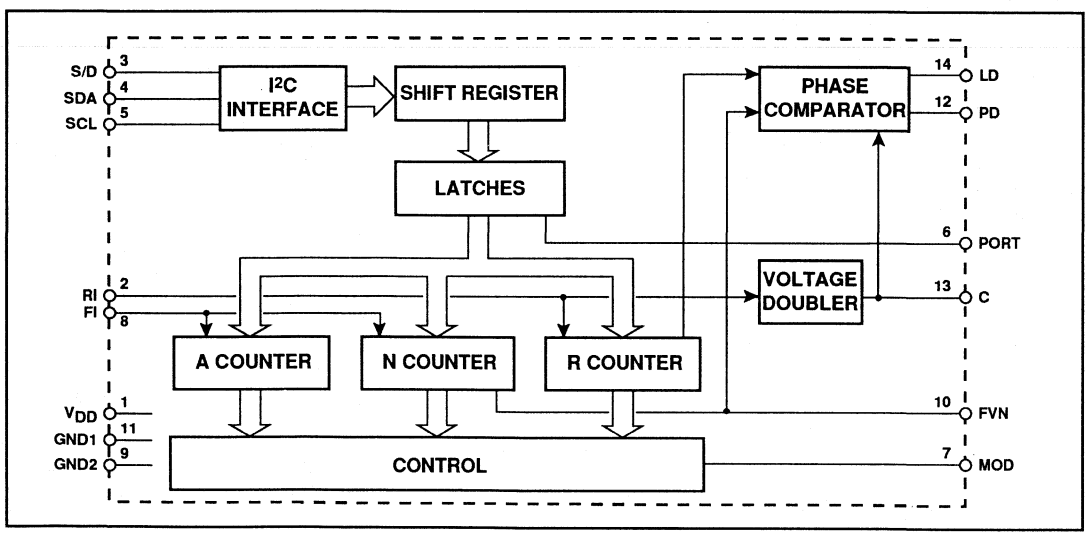


Fig.2 Simplified block diagram of NJ88C33

PIN DESIGNATIONS

Pin No.	Pin Name	Description
1	V_{DD}	Supply voltage (normally 5V or 3V).
2	RI	Reference frequency input from an accurate source, normally a crystal oscillator. The input is normally an AC coupled sinewave but may be a DC coupled square wave.
3	S/D	Single/dual modulus operating mode selection input. Single modulus operation is selected by driving the pin low. 'High' selects dual modulus mode.
4	SDA	I²C bus data input pin. It is also an open-drain output for generating I²C bus acknowledge pulses.
5	SCL	I²C bus clock input. It can be clocked at up to 5MHz.
6	PORT	Output control pin, which can be programmed via the I²C bus. It can be connected to the S/D pin to select single or dual modulus mode under bus control.
7	MOD	Modulus control pin. It is high in single modulus mode but switches in dual modulus operation. In dual modulus mode, MOD remains low during operation of the A counter until A=0; MOD then remains high until N=0, when both counters are reloaded. It can be programmed via the I²C bus as an open-drain or push-pull output.
8	FI	Frequency input from a VCO or prescaler. The input is normally an AC coupled sinewave but may be a DC coupled square wave.
9	GND2	Dedicated ground for the FI input buffer. It should be connected to the VCO ground or the prescaler ground, if used. Any noise on this pin will affect the performance of the VCO loop.
10	FVN	Open-drain output from the N counter.
11	GND1	Ground supply pin (global).
12	PD	Tristate current output from the phase detector. The polarity of the output can be programmed via the I²C bus.
13	C	Voltage doubler output. The operation of the doubler can be controlled via the I2C bus. In applications where the voltage doubler is switched off, this pin should be connected to GND1; a reservior capacitor should be connected from this pin to GND1 for applications where it is switched on.
14	LD	Open-drain lock detect output - requires integration if used.

OPERATING RANGE

Test conditions (unless otherwise stated):

PLL locked, RI = 10MHz

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	2.5	5	5.5	V	
Ambient temperature	T_{amb}	-40		+85	°C	
Supply current						
Single modulus	I_{DD}		2.1	3.0	mA	FI = 50MHz, V_{FI} = 150mVrms, N,R > 1000 without voltage doubler, V_{DD} = 5V, T_{amb} = 25°C
Dual modulus	I_{DD}		2	3.0	mA	FI = 10MHz, V_{FI} = 500mVrms, N,R > 1000 without voltage doubler, V_{DD} = 5V, T_{amb} = 25°C
Standby mode	I_{DD}			1	µA	FI = 50MHz, V_{FI} = 150mVrms, preamp off, divider off, V_{DD} = 5V, T_{amb} = 25°C
Standby mode	I_{DD}		1.0	1.5	mA	FI = 50MHz, V_{FI} = 150mVrms, preamp on, divider off, V_{DD} = 5V, T_{amb} = 25°C

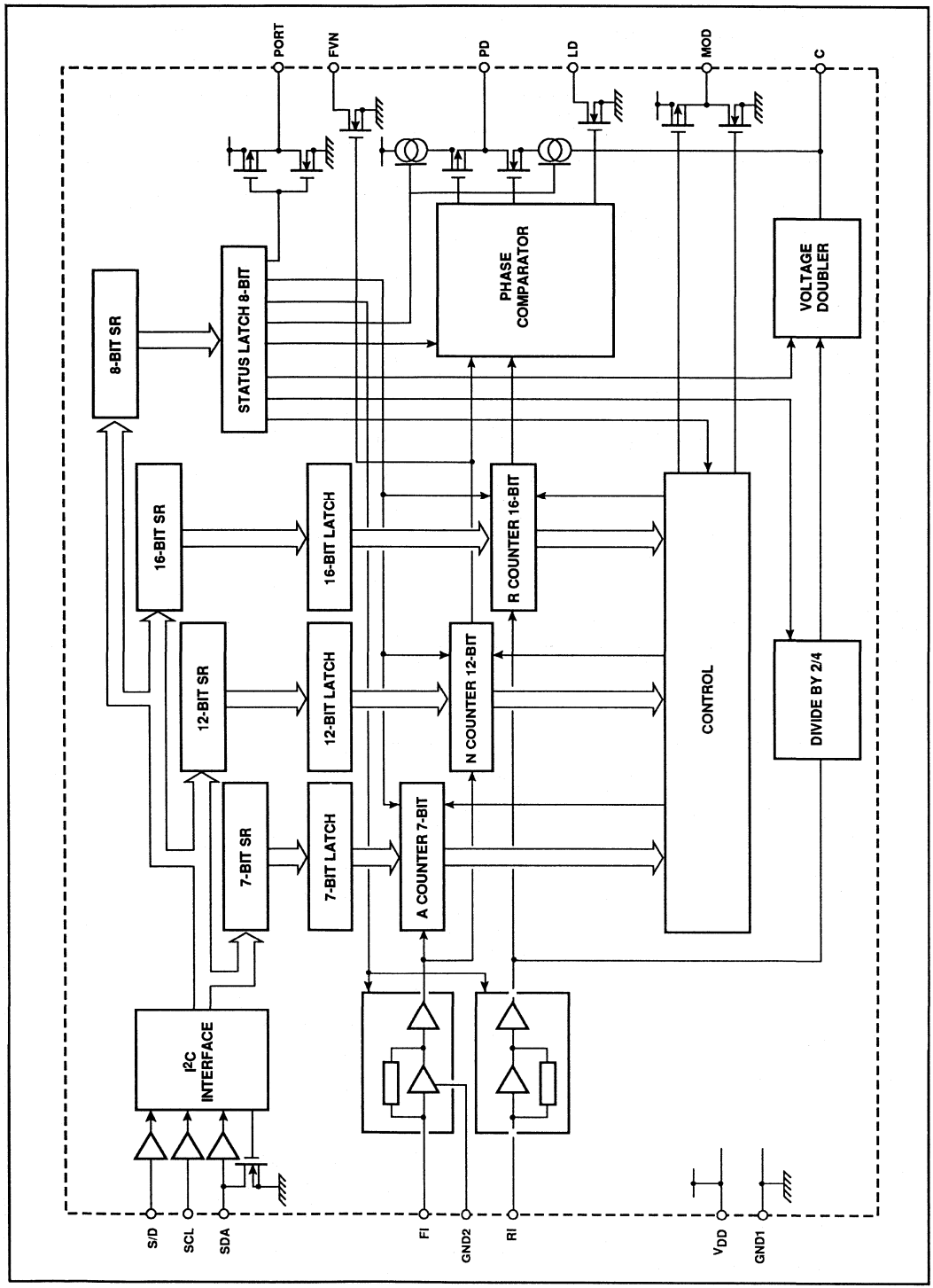


Fig.3 Functional block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

V_{DD} = 4.5V to 5.5V, T_{amb} = -40°C to +85°C

INPUT SIGNALS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input Signals SDA, SCL, S/D						
Input voltage high	V_{IH}	0.7V_{DD}		V_{DD}	V	
Input voltage low	V_{IL}	0		0.3V_{DD}	V	
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	µA	V_{IN} = V_{DD} = 5.5V
Input signal RI						
Input frequency	f_{max}			52	MHz	Sinewave input
Input voltage	V_{Irms}	100			mV	Note 1, 2
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	µA	V_{IN} = V_{DD} = 5.5V
Input signal FI						Dual modulus operation
Input frequency	f_{max}			52	MHz	Sinewave input
Input voltage	V_{Irms}	50			mV	Note 1, 2
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	µA	V_{IN} = V_{DD} = 5.5V
Input signal FI						Single modulus operation
Input frequency	f_{max}			150	MHz	Sinewave input
Input voltage	V_{Irms}	30			mV	FI = 0-70MHz Note 1, 2
	V_{Irms}	100			mV	FI = 70-120MHz Note 1, 2
	V_{Irms}	200			mV	FI = 120-150MHz Note 1, 2
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	µA	V_{IN} = V_{DD} = 5.5V

Note.1 Lowest noise floor achieved at 10dB above this level with I²C bus operating. The source impedance should be less than 2kΩ.

Note.2 DC coupled input amplitude V_{IRMS} > 0.8V_{DD}.

OUTPUT SIGNALS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output Signals SDA, LD						
Output voltage low	V_{OL}			0.4	V	Open drain, I_{OL} = 3mA
Output Signal PD						C_L = 400pF, tristate output
High current mode (see Fig.4)	I_{HU}	1.9	2.5	3.1	mA	0 < V_{PD} < 4.5, V_{DD} = 5V, T = 25°C Note 1
	I_{HD}	-1.9	-2.5	-3.1	mA	0.4 < V_{PD} < 5, V_{DD} = 5V, T = 25°C Note 1
Low current mode	I_{LU}	0.475	0.625	0.775	mA	0 < V_{PD} < 4.6, V_{DD} = 5V, T = 25°C Note 1
	I_{LD}	-0.475	-0.625	-0.775	mA	0.4 < V_{PD} < 5, V_{DD} = 5V, T = 25°C Note 1
Tristate	I_Z		50		nA	T_{amb} = -25°C to +60°C
Output Signal FVN						Open drain output
Output voltage low	V_{OL}			0.4	V	I_{OL} = 1mA
Output low pulse width	t_{WL}			1/FI		C_L = 30pF
Output Signals MOD, PORT						Push-pull output
Output voltage high	V_{OH}	V_{DD}-0.4			V	IOH = 0.5mA
Output voltage low	V_{OL}			0.4	V	I_{OL} = 0.5mA
Output Signal LD						Open drain output
Output voltage low	V_{OL}			0.4	V	I_{OL} = 3mA, C_L = 30pF
Output low pulse width	t_{WL}		10	1/FVN	ns	Loop locked
				$1/f_c$		Loop not locked
						FVN = FI/N
						f_C = RI/R

Note.1 Temperature coefficient for current is typically -0.7%/°C

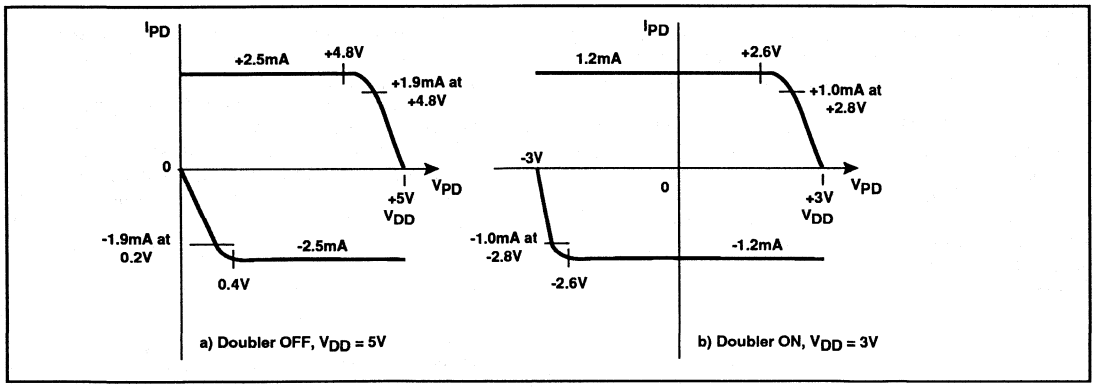


Fig. 4 Typical output signal PD, high current mode

VOLTAGE DOUBLER $V_{DD} \leq 3V$

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output Pin C						
Output voltage	V_C	$-V_{DD}$		$-V_{DD} + 0.8V$	V	f_{VD} = 2MHz, I_{OC} = 0µA, V_{DD} = 3V
	V_C	$-V_{DD}$		$-V_{DD} + 1.5V$	V	f_{VD} = 2MHz, I_{OC} = 100µA, V_{DD} = 3V
Current Consumption	I_D			100	µA	f_{VD} = 2MHz, I_{OC} = 0µA, V_{DD} = 3V

TIMING INFORMATION

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input Signal RI						
Input frequency	f_{max}	0		52	MHz	
Input frequency	f_{max}	0		10	MHz	V_{DD} = 2.7V
Rise time	t_R			1.5	µs	
Fall time	t_F			1.5	µs	
Slew rate		3			V/µs	
Input Signal FI						Dual modulus
Input frequency	f_{max}	0		52	MHz	
Input frequency	f_{max}	0		20	MHz	V_{DD} = 2.7V
Rise time	t_R			1.5	µs	
Fall time	t_F			1.5	µs	
Slew rate		3			V/µs	
Input Signal FI						Single modulus
Input frequency	f_{max}			150	MHz	
Input frequency	f_{max}	0		52	MHz	V_{DD} = 2.7V
Rise time	t_R	0		1.5	µs	
Fall time	t_F			1.5	µs	
Slew rate		3			V/µs	
Output Signal PORT						
Rise time	t_R			1	µs	C_L = 30pF
Fall time	t_F			1	µs	C_L = 30pF
Output Signal FVN						
Fall time	t_F		20		ns	C_L = 30pF
Output Signal MOD						
Rise time	t_R			10	ns	C_L = 30pF
Fall time	t_F			10	ns	C_L = 30pF
Delay time (L→H)	t_{DLH}			15	ns	C_L = 30pF Measured from +Ve edge of FI
Delay time (H→L)	t_{DHL}			15	ns	C_L = 30pF Measured from +Ve edge of FI

PHASE COMPARATOR

The phase comparator produces current pulses of duration equal to the difference in phase between the comparison frequency (fc=RI/R), and f_{VN}, the divided-down VCO frequency (FI/N).

When status bit 4 is set high the positive polarity mode of the output PD is selected. When fc leads f_{VN} the PD output goes high; when f_{VN} leads fc it goes low. Similarly, selecting the negative polarity mode of PD by programming bit 4 of the status register low causes PD to have the inverse polarity. The loop filter integrates the current pulses to produce a voltage drive to the VCO.

No pulses are produced when locked. The lock detect output, LD, produces a logic '0' pulse equal to the phase difference between f_c and f_{VN}.

When the phase difference between fc and f_{VN} is too small to be resolved by the phase detector then no current pulses are produced. In this region the loop does not reduce the close-in noise on the VCO output. This can be overcome using a very high value resistor to leak a few nanoAmps of current from the filter and keep the loop on the edge of the region.

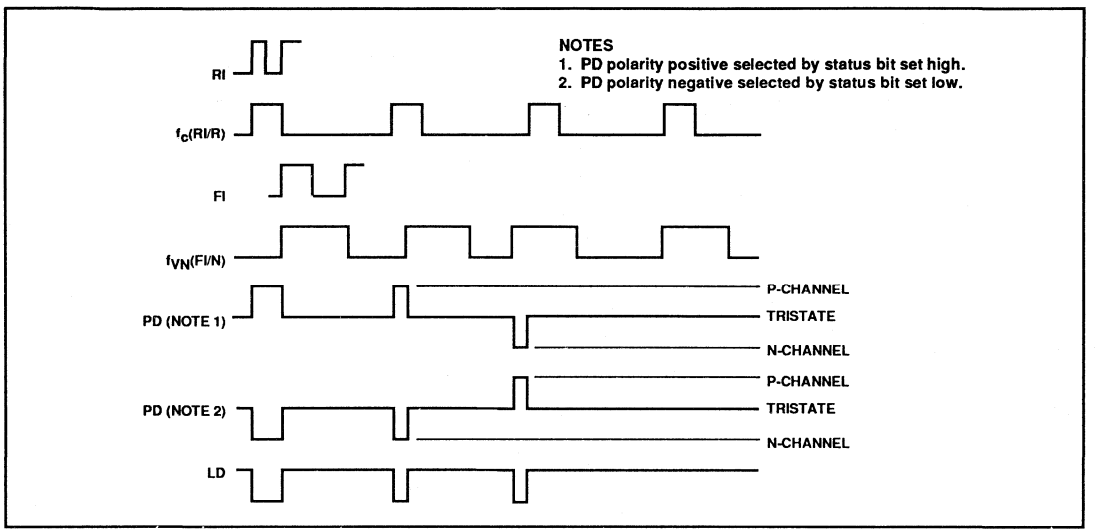


Fig. 5 Phase comparator phase diagram

PROGRAMMING

Transmission Protocol

I²C programming messages consist of an address byte followed by a sub-address byte followed by 1, 2 or 3 bytes of data. Bit 7 of the address byte must match the setting of the S/D pin for the address to be recognised. This allows for separate addressing of two NJ88C33 synthesisers on the same bus. The sub-address should be set to select the correct registers to be programmed and should be followed by the appropriate number of data bytes. Registers are not programmed until the complete message protocol has been checked.

Each message should commence with a START condition and end with a STOP condition unless followed immediately by another transfer, when the STOP condition may be omitted.

Data is transferred from the shift register to the latches on a STOP condition or by a second START condition.

A START condition is indicated by a falling edge on the Serial Data line, SDA, when the Serial Clock line. SCL, is high.

A rising edge on SDA when SCL is high indicates a STOP condition as shown in Fig.6.

Data on SDA is clocked into the NJ88C33 on the rising edge of SCL. The NJ88C33 acknowledges each byte transferred to it by pulling the SDA line low for one cycle of SCL after the last bit has been received.

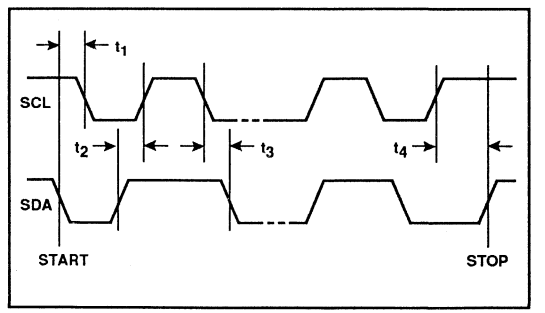


Fig. 6 I²C timing diagram

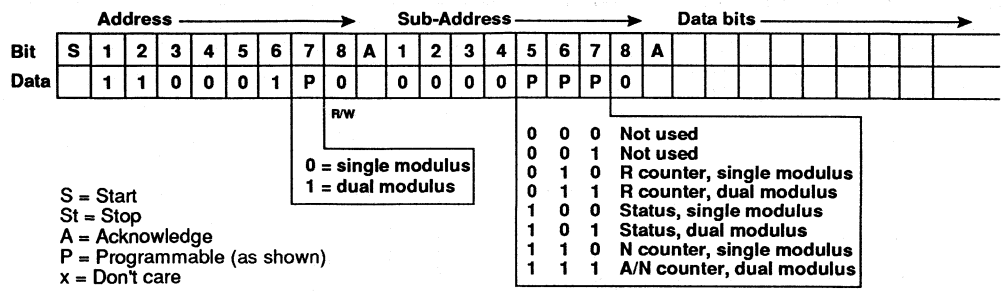
I2C TIMING INFORMATION

VDD = 4.5V to 5.5V, Tamb = -40°C to +85°C

Parameter	Symbol	Value		Unit
		Min.	Max.	
Serial clock frequency	f_{SCL}		5	MHz
SCL hold after START	t_1	200		ns
Data set-up time	t_2	20		ns
Data hold after SCL low	t_3	0		ns
SCL set-up before STOP	t_4	20		ns

Address and Sub-Address Formats

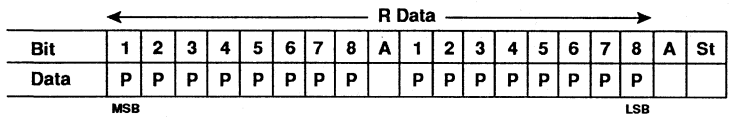
The correct addressing sequence for the NJ88C33 is shown below. The START condition is followed by the address byte, the acknowledge from the NJ88C33, the sub-address byte, another acknowledge then the associated data. The correct values for each address and sub-address are listed, together with the message selection options.



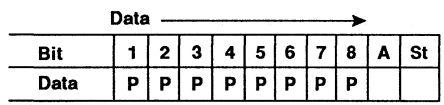
Data Formats

Each of the data formats should be preceded contiguously by the addressing sequence given above.

R counter : single or dual modulus



Status : single or dual modulus

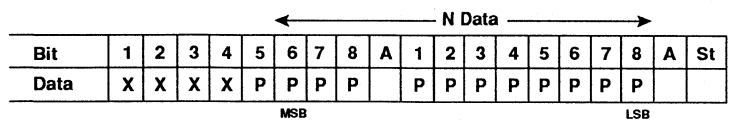


Status Byte		
Bit	**0**	**1**
1	PORT = low	PORT = high
2	Counters off (1)	Counters on
3	FI and RI off (2)	FI and RI on
4	PD = polarity negative	PD = polarity positive
5	PD bias = 0.625mA	PD bias = 2.5mA
6	f_{VD} = RI/2	f_{VD} = RI/4
7	Doubler off	Doubler on (3)
8	MOD = push-pull	MOD = open drain

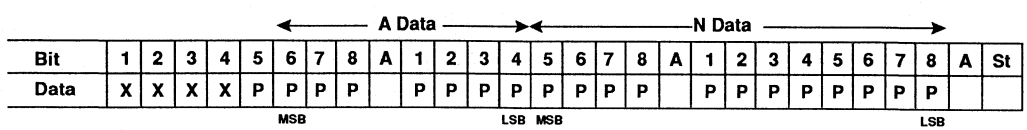
NOTES

1. In this standby mode the counters are disabled but the voltage doubler and I²C interface can both function.
2. In this standby mode the FI and RI preamplifiers are disabled, which stops the counters and the voltage doubler. The I²C interface still operates.
3. The voltage doubler should only be used when $V_{DD} \leq 3.0V$

N counter : single modulus



A/N counters : dual modulus



APPLICATION CIRCUITS

Single Modulus

In this mode, the NJ88C33 synthesiser can be used with or without a fixed modulus prescaler. The R counter is programmed with a value to produce a comparison frequency fc. When the N counter is changed by 1 the loop is no longer in lock and the phase detector output produces current pulses to bring the loop back into lock. These pulses are integrated by the loop fiiter to produce the VCO voltage drive. When the VCO loop is locked, FI/N=f_c i.e., the VCO frequency is N x f_c.

Using a prescaler with a division ratio P, the smallest VCO output frequency step is Pf_c and the VCO frequency is PNf_c.

If a low pass filter is connected to the lock detect output as shown and sampled by the microprocessor, the proximity of the synthesiser loop to lock can be evaluated.

The A counter is not used in this mode.

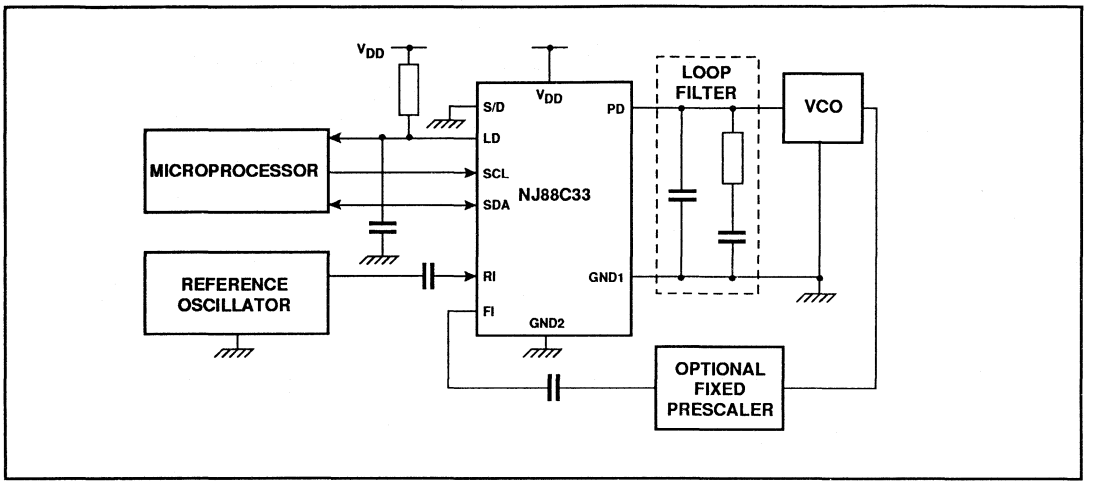


Fig. 7 Single modulus application

Dual Modulus

This mode allows much higher frequencies to be used in conjunction with a prescaler but maintains the step size, fc. In this mode, a dual modulus prescaler (with ratios P and P + 1) must be used with the NJ88C33. The A counter controls the MOD output, which is used to select the division ratio of the prescaler.

When the A counter is non-zero, the MOD output is low and goes high when the A counter has counted down to zero. MOD remains high until the N counter reaches zero, when both counters are re-loaded. Thus, the prescaler divides by P for N-A cycles and by P + 1 for A cycles of FI. The VCO frequency is given by $PNf_c + Af_c$.

Note that programming A = 0 produces a count of 128 cycles.

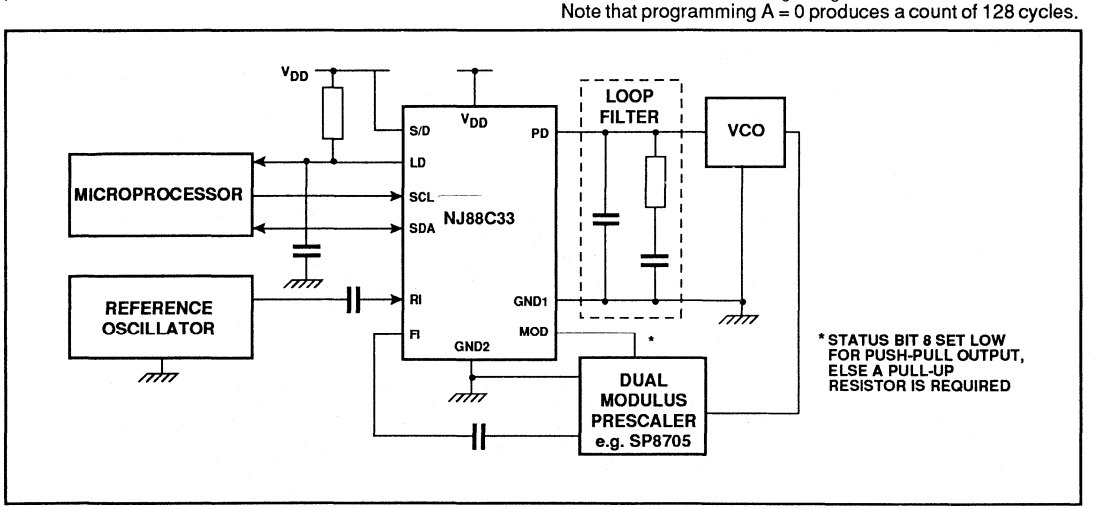


Fig. 8 Dual modulus application

VCO Driving Without Voltage Doubler

To switch off the voltage doubler, bit 7 of the status register is programmed low. This will reduce current consumption and minimise noise. The voltage doubler output C should be connected to GND1 as connection to GND2 would induce noise in the VCO loop.

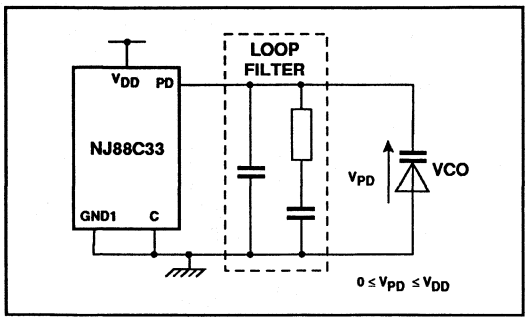


Fig. 9 Driving a VCO without voltage doubler

VCO Driving With Voltage Doubler

The voltage doubler is switched on by setting bit 7 of the status register high. It is recommended that a reservoir capacitor of at least 1µF be connected from C to GND1.

The voltage doubler is designed to boost VCO drive in low voltage applications.

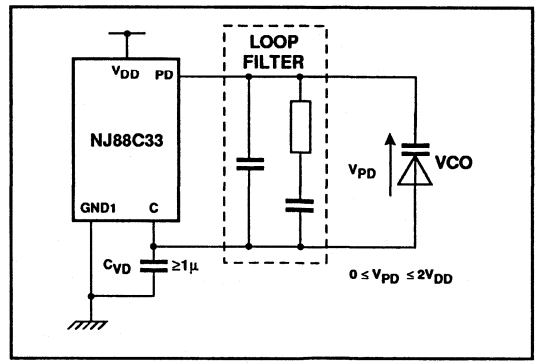


Fig. 10 Driving a VCO using the voltage doubler

Further Applications Information

A stand-alone programmer card and an evaluation board are available for evaluating the NJ88C33. The programmer card allows two sets of variables to be programmed into both the divider and status registers during alternate programming cycles, at either the standard I²C bus rate of 100kHz or at 2MHz.

Initialisation is with either a manual push-button or by an external logic level pulse; a synchronisation output is provided to allow a quick assessment of 'step' and 'settle' responses to be made.

The NJ88C33 evaluation board (Fig. 11) dernonstrates the preferred layout technique - providing a reference oscillator, a 60 to 80MHz VCO and a simple loop filter to complete a minimal frequency synthesiser loop. The two units allow analysis of different loop variables as well as the selection of comparison frequencies for fast frequency-hopping loops.

Application Note: AN94, *'Using* the NJ88C33 *PLL Synthesiser'* explains the design equations and demonstrates the use of the device, and is available from your local GPS customer service centre.

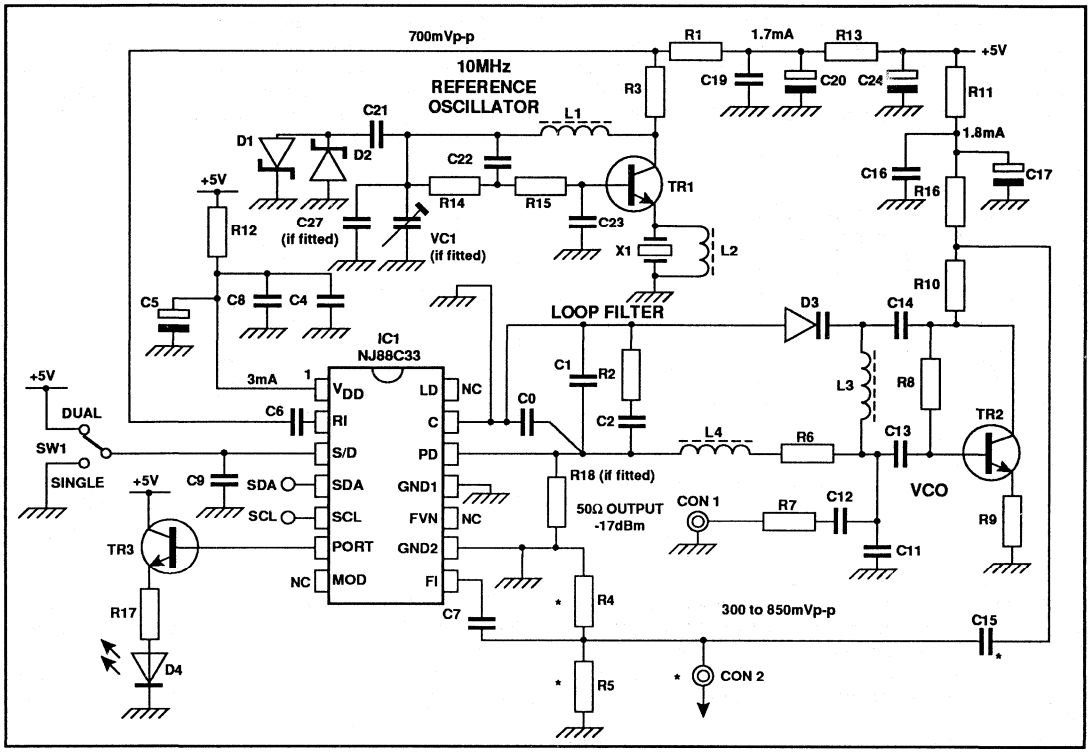


Fig. 11 Typical applications circuit

* Insert C15, delete R4 and R5 if CON2 is to be used to monitor the VCO. Delete C15 insert R4 and R5 if CON is to provide an external source, otherwise short C15 and delete R4, R5 and CON2.

COMPONENT LIST FOR FIG. 11

Capacitors		Capacitors		Resistors		Inductors		Miscellaneous	
C0	1nF 10%	C17	22µF/35V Elect.	R1	270Ω	L1	15µH 10%	IC1	NJ88C33
C1	100nF 10%	C19	10nF 10%	R2	470Ω	L2	220µH 10%	X1	10.00MHz 5ppm series
C2	1µF Tant.	C20	22µF/35V Elect.	R3	330Ω	L3	180nH 20%	SW1	Miniature slide switch
C4	10nF 10%	C21	10nF 10%	R4	100Ω	L4	470µH 10%	CON1	SMC socket
C5	22µF/35V Elect.	C22	10nF 10%	R5	100Ω			CON2	SMC socket
C6	10nF 10%	C23	22pF 5% NPO	R6	1kΩ	**Diodes**		PCB	C33ISS2
C7	1nF 10%	C24	22µF/35V Elect.	R7	120Ω				
C8	1nF 10%	C27	22pF 5% NPO	R8	27kΩ	D1	1N6263 Schottky		
C9	1nF 10%	VC1	3p5-22p	R9	Link	D2	1N6263 Schottky		
C11	150pF 5% NPO			R10	1kΩ	D3	BBY40 varicap		
C12	1nF 10%			R11	10Ω	D4	5mm red LED		
C13	1nF 10%			R12	10Ω				
C14	2p7 ± 0.5pF NPO			R13	10Ω	**Transistors**			
C15	10nF 10%			R14	22kΩ				
C16	10nF 10%			R15	2.7kΩ	TR1	BFS17 RF NPN		
				R16	330R	TR2	BFS17 RF NPN		
				R17	100Ω	TR3	2N3904 Switching		
				R18	33MΩ				

NOTES
1. With the exception of electrolytics, all capacitors are surface mount types.
2. All resistors are 0.25W, ±2%.
3. C0, C1, C2, C11, C12, C13 and C14 must be low leakage types.
4. R18 may be required to optimise VCO close in noise performance.

NJ88C50

DUAL LOW POWER FREQUENCY SYNTHESISER

The NJ88C50 is a low power integrated circuit, designed as the heart of a fast locking PLL subsystem in a mobile radio application. It is manufactured on GEC Plessey Semiconductors 1.4 micron double polysilicon CMOS process, which ensures that low power and low noise performance is achieved. The device contains two synthesisers, one for the generation of VHF signals up to 125MHz and a second for UHF (when used with a mulitmodulus prescaler such as the SP8713/14/15). The main synthesiser has the capability of driving a dual speed loop filter and also can perform Fractional-N interpolation. Both synthesisers use current source outputs from their phase detectors to minimise external components. Various sections may be powered down for battery economy.

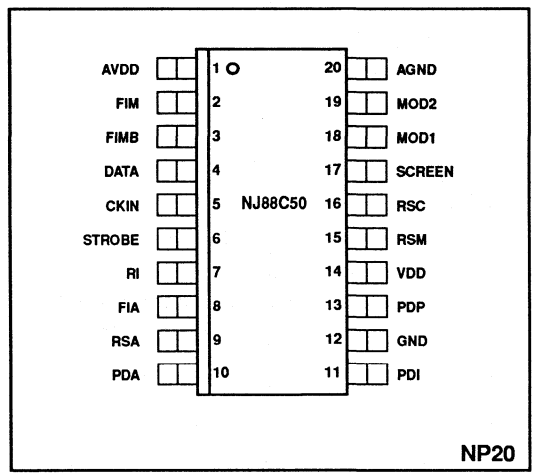


Fig.1 Pin assignment

FEATURES

- 30MHz main synthesiser
- 125MHz auxiliary synthesiser
- Programmable output current from phase detector - up to 10mA
- High input sensitivity
- Fractional-N interpolator
- Supports up to 4 modulus prescalers
- SSOP package

APPLICATIONS

- NMT, AMPS, ETACS cellular
- GSM, IS-54, RCR-27 cellular
- DCS1800 microcellular
- DLMR, DSRR, TETRA
- DECT, PHP cordless telephones

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-55°C to +150°C
Operating temperature	-40°C to +85°C
Supply voltage	-0.5 to 7.0V
Voltage on any pin	-0.3V to (V_{DD} + 0.3V)

ORDERING INFORMATION

NJ88C50\IG\NPAS - (Industrial temp range in SSOP package)

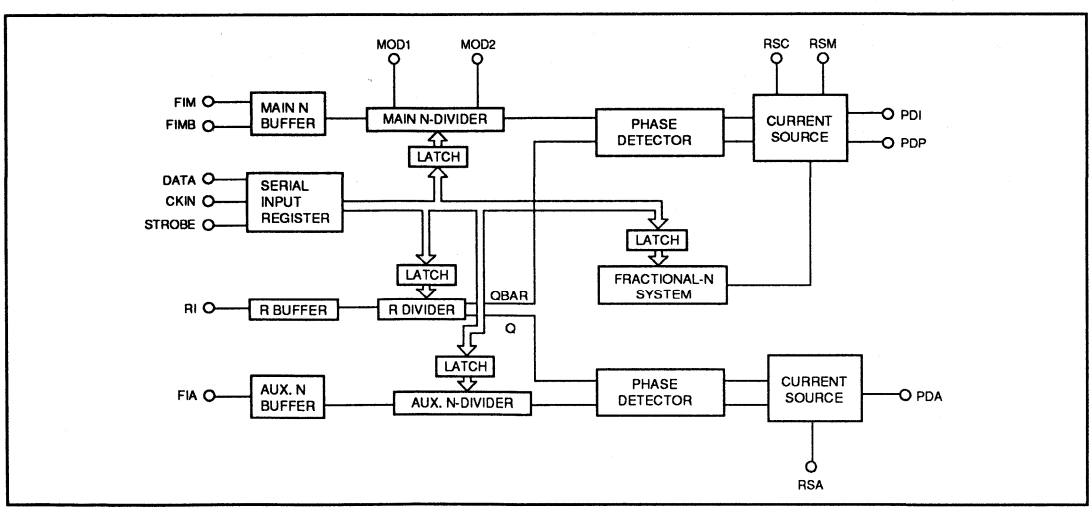


Fig.2 Simplified block diagram

ARCHITECTURE

Fig.2 shows a simplified block diagram of the NJ88C50, a more detailed description of each block and its function is given later in this datasheet.

The synthesiser consists of the following blocks

- 35MHz reference frequency input buffer
- 35MHz programmable reference divider
- 125MHz Auxiliary synthesiser input buffer
- 125MHz Auxiliary synthesiser programmable divider
- Auxiliary synthesiser phase detector with current source outputs
- 30MHz main synthesiser input buffer (differential inputs)
- 30MHz main synthesiser programmable divider and control logic
- Main synthesiser Fractional-N interpolation system
- Main synthesiser phase detector with dual current source outputs

PIN DESCRIPTION

Pin	Name	Function
1	AVDD	Analog supply pin (nominally 5V).
2	FIM	Main synthesiser balanced input buffer, may be used with single ended prescaler output if Fimb is biased.
3	FIMB	Main synthesiser balanced input buffer, may be used with balanced prescaler output, or biased for single ended operation.
4	DATA	Serial input for programming data.
5	CKIN	Serial clock input for programming bus.
6	STROBE	Program enable pin, active low.
7	RI	Master reference frequency input, should be a.c coupled from an accurate source.
8	FIA	Auxiliary synthesiser frequency input, should be a.c coupled.
9	RSA	Current setting resistor connection defining auxiliary phase detector output current.
10	PDA	Tristate current output from auxiliary phase detector.
11	PDI	Tristate current output from the main synthesiser's phase detector giving integral control.
12	GND	Digital ground supply pin.
13	PDP	Tristate current output from the main synthesiser's phase detector giving proportional control.
14	VDD	Digital supply pin (nominally 5V).
15	RSM	Current setting resistor connection defining main synthesiser's phase detector output currents.
16	RSC	Current setting resistor connection defining the compensation current for fractional-N ripple elimination in the main synthesiser's current source outputs.
17	SCREEN	To be connected to ground to provide isolation of the modulus control pins from RF interference.
18	MOD1	Modulus control pin (see truth table).
19	MOD2	Modulus control pin (see truth table).
20	AGND	Analog ground supply pin.

It is recommended that power supply pins are well decoupled to minimise power rail born interference.

FUNCTIONAL DESCRIPTION

The NJ88C50 has been designed using a modular concept, and its operation can be best summarised as these component blocks.

Reference divider

The reference divider is used to provide the reference signals needed for both the main and auxiliary synthesiser phase detectors. The divider allows for a twelve bit number to be loaded, via the serial bus, to select the required division ratio. Division ratios of 3 to 4095 can be used.

The reference divider input stage will accept a low level, AC coupled, sinewave input. It is anticipated that in most systems this will be provided by a stable reference source up to 35MHz, and so encompasses all the common TCXO (temperature controlled crystal oscillator) frequencies, such as 9.6, 12.8, 13.0, 19.44 and 26MHz.

A standby mode is supported so that the reference divider can be powered down, this is achieved using two of the serial program control bits.

To reduce the possibility of unwanted interaction between the main and auxiliary synthesisers, the charge pumps do not take current at the same time. To achieve this the output of the reference divider has a duty factor of approximately 50:50, which then allows the Q and QBAR taps to be used for the auxiliary and main synthesisers respectively. By doing this the current pulses can be taken alternatively, minimising modulation of the power supply rails as current is drawn.

The reference divider consists of a 12 bit programmable divider followed by a 4 bit binary counter. This 4 bit counter gives a choice of divide by M, 2M, 4M or 8M.

A pair of programmable control bits are used to determine which of the divide by M, 2M, 4M or 8M outputs is supplied to the auxiliary synthesiser's phase detector and a further pair of control bits are used to determine which are supplied to the main synthesiser's phase detector.

Auxiliary synthesiser

The auxiliary synthesiser operates over an input frequency range from 1 to 125MHz, without the use of an external prescaler. The synthesiser consists of a 12 bit N divider and a digital phase comparator with current source outputs. The reference frequency is supplied by the shared reference divider. Current source outputs allow a passive loop filter to be used.

When the auxiliary synthesiser is not in use, a standby mode is supported so that power consumption is reduced. This is achieved using one of the serial program control bits.

The divider is programmed with a 12 bit word allowing division ratios of 3 to 4095 to be used.

The auxiliary phase detector consists of the 2 D-type phase and frequency detector shown in Figure.3 below, the high and low outputs of which drive on-chip, opposing complementary charge pumps. This type of phase detector design eliminates non linearity or deadband around the zero phase error (locked) condition.

The charge pump output current level is set by an external resistor on the RSA pin (pin 9) up to a limit of 250μA +/-10%. A pull up current pulse will indicate that the VCO frequency must be increased, whilst a pull down pulse indicates that the frequency must be decreased.

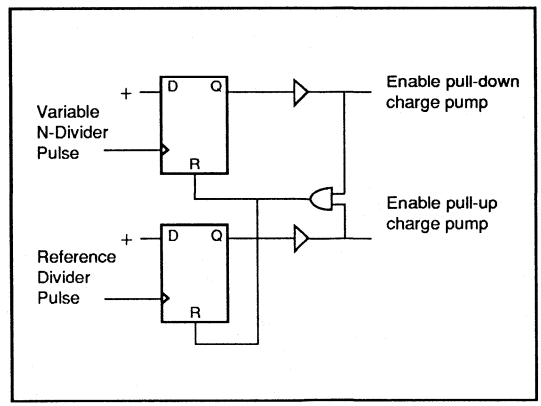


Fig.3 Auxiliary phase detector

Main Synthesiser

The main synthesiser is capable of operating at frequencies up to 30MHz. The synthesiser uses the 12 bit reference divider, shared with the auxiliary synthesiser, a 12 bit up/down N divider and a digital phase comparator with current source outputs.

The device also has a number of features which increase the design flexibility and performance of the synthesiser. These include fractional-N operation, speed up mode and support of 2, 3 and 4 modulus prescalers. A description of the operation and advantages of each of these features is given.

The main N divider input buffer will accept inputs from an external prescaler, either as balanced (2 wire) ECL levels at frequencies up to 30MHz, or DC coupled to a single ended prescaler output. Single ended operation requires the other buffer input (pin 3) to be externally biased to the correct slicing voltage for the prescaler and also externally decoupled.

If the inputs are in the form of balanced ECL levels, there must not be a skew of greater than 2ns between one input changing and the second input changing. The relationship of the signals is shown below in Fig.4.

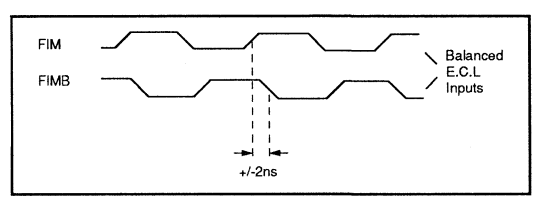


Fig.4 Maximum input skew

The main N divider is programmable so that it can determine how many cycles of each division ratio the external prescaler will perform.

The total division ratio of the output from the system VCO to the synthesiser's phase detector may be expressed as N_{TOT} and R1, R2, R3 and R4 are the available prescaler ratios and N1, N2, N3 and N4 are the corresponding number of cycles for each ratio selected, within one complete division cycle.

The divider is programmed via the serial data bus and the values needed to be programmed for each of the possible prescaler ratios are as follows:-

In 2 modulus mode (division ratios R1, R2)
N_{TOT} = N1.R1 + N2.R2
Programmed values needed:
N1 - a 12 bit value giving the number of times R1 is to be used
N2 - a 8 bit value giving the number of times R2 is to be used

In 3 modulus mode (division ratios R1, R2, R3)
N_{TOT} = N1.R1 + N2.R2 + N3.R3
Programmed values needed:
N1 - a 12 bit value giving the number of times R1 is to be used
N2 - a 4 bit value giving the number of times R2 is to be used
N2+N3 - a 4 bit value where N3 is the number of times R3 is to be used and (N2+N3) is modulo-16 addition

In 4 modulus mode (division ratios R1, R2, R3, R4)
N_{TOT} = N1.R1 + N2.R2 + N3.R3 + N4.R4
Programmed values needed:
N1 - a 12 bit value giving the number of times R1 is to be used
N2 - a 4 bit value giving the number of times R2 is to be used
N2+N3 - a 4 bit value where N3 is the number of times R3 is to be used.
N2+N3+N4 - a 4 bit value where N4 is the number of times R4 is to be used. (N2+N3) and (N2+N3+N4) are modulo-16 addition.

To facilitate the use of multimodulus prescalers the N divider is based upon a twelve bit up/down counter which functions as follows

The first value, N1, is loaded into the counter which then counts down from N1 to zero. During this time, the modulus ratio R1 is selected.

When the counter reaches zero modulus R2 is selected and the counter then counts up to the N2 value. If 2 modulus operation is chosen, the counter is then reloaded with N1 and the count is repeated.

For operation with 3 or 4 modulus devices, the counter continues to count up once it has reached the N2 value. The count continues to the N2+N3 value and during this time the R3 ratio is selected. In the 3 modulus case, when the N2+N3 value is reached the counter is then reloaded with the N1 value and the modulus ratio R1 is selected.

For 4 modulus operation the counter will continue its count up to the N2+N3+N4 value before reloading the N1 value. During this time the R4 modulus is selected.

If N2, N3, or N4 are set to zero this will give a full count of 16 for the corresponding modulus.

The N divider block also has a special control line from the Fractional-N logic. When required this control will cause the total division ratio to be increased from N to N+1. This is achieved by forcing a cycle which would have normally used a prescaler ratio R1 to use ratio R2 instead. R1 and R2 are chosen so that R2 equals R1+1.

Further explanation of the operation of the synthesiser when using 2, 3 or 4 modulus prescaler is given in the section on multimodulus division (page 8).

The phase detector used on the main synthesiser is similar to the type used on the auxiliary synthesiser (Figure.3). In this case, however, the detector will drive two pairs of complimentary charge pumps, one of which is intended to drive the loop integrator capacitor to provide integral control, whilst the other provides proportional control for the VCO. This system is shown in Fig 5, and has applications where fast locking of the loop is required.

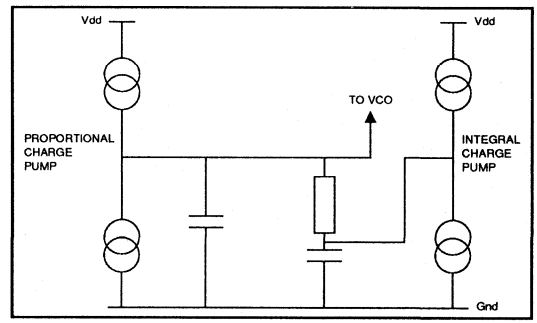


Fig.5 Loop filter using both charge pumps

MODES OF OPERATION

Normal Mode

The synthesiser will operate in normal mode while the strobe line of the serial data bus is low. In this mode the following current levels are produced. The charge pump providing the proportional feedback term will have a normal current level designated by Iprop(0), that is set by an external bias resistor, RSM. Iprop(0) will vary when different N-divider ratios are programmed, so that it is proportional to the total division ratio. To avoid the necessity of computing the total division ratio on chip, an eight bit number representing the most significant bits of Ntot will be loaded via the serial data bus. Iprop(0) is therefore given by

$$Iprop(0) = CN.Ibo$$

where CN is the loaded eight bit number and the value Ibo is scaled from the external current setting resistor RSM where Ibo = Irsm/32. Typically Ibo = 1μA ,and therefore Iprop(0) will have a maximum value equal to 255μA.

The normal value of Iprop, Iprop(0), is obtained while the strobe line of the serial programming bus is held low. In this condition, the second charge pump providing the integral feedback term is inactive.

Speed up Mode

In speed up mode the loop bandwith during switching is increased to allow faster initial frequency acquisition. This is done by using the dual phase detector outputs (PDP and PDI) connected to a standard passive loop filter as shown in fig.5. The effect of this is to increase the loop gain and hence the bandwidth while maintaining a constant phase margin when switching between speed up mode and normal mode.

The synthesiser operates in speed up mode when the strobe line goes high loading either word A or word A2 (see programming section Page 8-Page 9) and it will stay in this mode until the strobe line goes low. In this mode the following current levels are produced. The charge pump providing the proportional feedback will increase its current from Iprop(0) to a value Iprop(1), where

$$Iprop(1) = 2^{L+1} \cdot Iprop(0)$$

where L is a two bit number loaded as part of the serial programming data. Iprop(1) will therefore be 2, 4, 8 or 16 times Iprop(0). The charge pump supplying Iprop is specified up to a value of 1mA.

Also when the strobe line goes high loading word A or word A2, the charge pump providing the integral feedback term becomes active at a current level Iint given by

$$Iint = K.Iprop(1)$$

where K is a four bit number loaded as part of the serial programming data. Although Iint can be programmed to be 240 times greater than Iprop(0), the charge pump supplying Iint is only specified up to a value of 10mA.

For all charge pumps, a pull-up current indicates the VCO frequency should be increased while a pull-down current indicates the VCO frequency should be decreased.

For the proportional and integral charge pumps, the selected pulse current levels will remain substantially constant over the charge pumps output voltage ranges tabulated in the electric characteristics. "Substantially constant" means that the current will not have changed by more than 10% of the value measured at 2.5 volts on the output.

FRACTIONAL-N OPERATION

Conventional, non fractional-N synthesisers have a frequency resolution or step size equal to the phase detector comparison frequency. Fractional-N refers to a technique which allows finer frequency steps to be obtained.

The synthesised frequency with a conventional synthesiser is equal to N times the phase detector comparison frequency, where N is the programmable integer loop divide ratio. Using fractional-N the value of N is alternated between N and N+1 in order to simulate a fractional part. For example 9000.375 would be simulated by alternating between 9000 and 9001 in the pattern

9000, 9000, 9001, 9000, 9000, 9001, 9000, 9001 (mean value of 9000.375).

On the NJ88C50 the fractional-N circuit consists of an accumulator which can be set to overflow at a value of 5 or 8 (FMOD in programming word D, see page 9). The value in the accumulator, A, is incremented once every comparison cycle of the main phase detector and every time the accumulator overflows the total division ratio of the synthesiser and prescaler is increased from N to N+1. To obtain the pattern described above N=9000 and FMOD would be set to mod8 and the incremental value, NF(programmed in word A) would be set to 3. The accumulator would then behave as shown below.

Increment Value	Accumulator Value	Total Division Ratio
3	3	9000
3	6	9000
3	1	9001
3	4	9000
3	7	9000
3	2	9001
3	5	9000
3	0	9001

Varying NF allows different fractions to be obtained. If NF=1 and FMOD=8 the accumulator would overflow once in every 8 cycles giving a value of 9000.125. Similarly if NF=4 the accumulator overflows every other cycle giving 9000.5.

For a given step size this increase in resolution means a higher comparison frequency at the phase detector, and therefore a lower overall division ratio. For example,

with a step size = 200kHz
and carrier frequency = 900MHz

Non fractional-N synthesiser
Comparison frequency=200kHz
Division ratio=$\frac{900MHz}{200kHz}$=4500

Fractional-N synthesiser (using 5ths)
Comparison frequency=1MHz
Division ratio=$\frac{900MHz}{1MHz}$=900

In most applications the phase noise is proportional to the overall division ratio. Therefore fractional-N gives lower phase noise. This higher comparison frequency and lower phase noise allows circuits to be built with wider loop bandwidths while keeping the same stability. This means that phase locked loops (PLLs) can be made to either switch faster for a given phase noise or be quieter for a given switching speed, compared to conventional designs.

However the alternation between the N and N+1 values causes a ripple in the output frequency. This ripple is not desirable in radio frequency synthesisers. This ripple or jitter waveform is predictable from the pattern of N and N+1 values and so can be cancelled.

The instantaneous accumulator value, A, is proportional to the cumulative frequency error caused by ignoring the fractional part during the periods of the divide by N. The accumulator value, A, may therefore be used to generate a waveform corresponding to the jitter waveform, that is then used to cancel the jitter out of the phase detector. This jitter compensation current pulse is equal to A.Icomp where Icomp represents the step size as A is incremented.

Corresponding to the two alternative values of Iprop, Iprop(0) and Iprop(1), Icomp will take the values Icomp(0) and Icomp(1). Icomp is always pull-up, and the magnitude of its steps for perfect jitter compensation are related to the value of Iprop by the factors

0 , 1/Q.Ntot , 2/Q.Ntot , 3/Q.Ntot Q-1/Q.Ntot
where Q = accumulator modulus in use (5 or 8)

Since

$I_{prop}(0) = CN.I_{bo}$

and CN is an approximation to Ntot apart from a scaling factor, the value of Icomp(0) required becomes independent of Ntot and its steps are

0 , 1/Q , 2/Q , 3/Q ..... Q-1/Q times Ibo.(scaling factor)

where scaling factor = $\frac{\text{Max. value of CN to be used}}{\text{Corresponding max. value of Ntot}}$

therefore $I_{co} = \frac{1}{Q} \times \frac{CN(max)}{Ntot(max)} \times I_{bo}$

and $I_{comp}(0) = A.I_{co}$

where Ico is scaled from the external current setting resistor RSC.

$I_{co} = I_{rsc}/128.$

Typically Ntot(max) might be 10000, with CN(max)=250 and Q=8, so the current step will be of magnitude Ibo/320. Since Ibo is only 1 uA, this is a very small value; however this value only applies if Icomp is a continuous current. Icomp however will be a short current pulse coincident with the Iprop pulse, in order to cancel jitter components over the widest possible frequency range.

When the duty factor of Icomp is taken into account, its pulse value may be increased accordingly. Icomp is therefore generated as a pulse of fixed width equal to two periods of the input reference clock frequency, with a timing that straddles the active edge of the reference divider output pulse supplied to the main phase detector, as shown below: (Fig 6).

Since the duty factor of Icomp is 2/M and depends on the value of M programmed, it is possible to set the peak pulse value of Icomp(0) by means of the external current setting resistor RSC to correspond with the value of M intended, the value of 'scaling factor' defined above, the accumulator modulus Q and the value of Ibo set by the other current setting resistor.

therefore $I_{co} = \frac{1}{Q} \times \frac{Nmax}{Ntot(max)} \times \frac{M}{2} \times I_{bo}$

This gives a typical value for Ico of 0.1μA.

The two values of Icomp, Icomp(0) and Icomp(1) are related by

$$I_{comp}(1) = 2^{L+1} .I_{comp}(0)$$

Icomp(0) occuring when the strobe line is low and Icomp(1) occuring when the strobe line is high loading either WORDA or WORDA2 (see programming section, page 8 and 9) .

Corresponding to the pull-up pulse Icomp(1) that is added to the proportional charge pump pulse Iprop(1), there is also a pull-up current pulse Icomp2 which is added to the integral charge pump pulse Iint. This pulse Icomp2 only applies when the stobe line is high (loading either WORDA or WORDA2). When the strobe line is low there will be no Iint or Icomp2 pulses. The value of Icomp2 is given by

$$I_{comp}2 = I_{comp}(1).K$$

where K is a four bit number entered as part of the serial programming data.

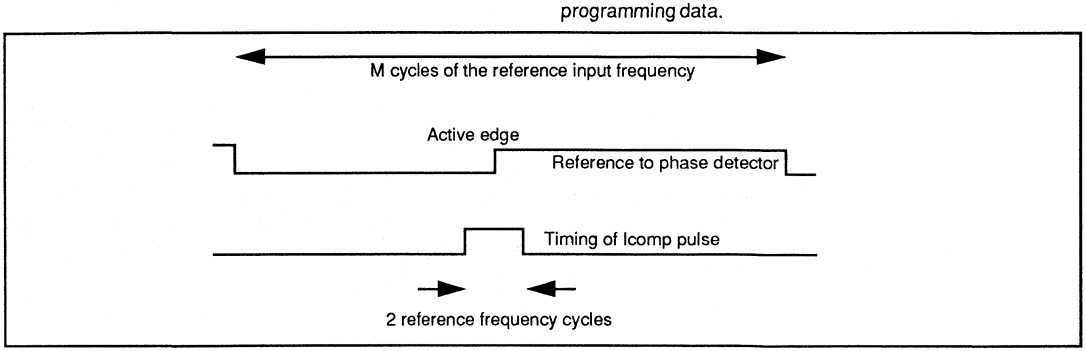


Fig.6

MULTIMODULUS DIVISION

The NJ88C50 supports the use of 2, 3 and 4 modulus prescalers. Two modulus prescalers such as the SP8714/15 are commonly used in PLLs. Additional information on using 2 modulus prescalers can be found in application note AN132 in the GEC Plessey Semiconductors Personal Communications handbook (May 1992).

When using a 2 modulus prescaler (R/R+1) the minimum division ratio above which all channels can be synthesised is given by

$$\text{Minimum division ratio} = R(R-1)$$

eg. for a 64/65 prescaler such as the SP8714/15

$$\text{Minimum division ratio} = 64(64-1) = 4032$$

When fractional-N operation is being used higher comparison frequencies are used, which are obtained by using lower division ratios. Use of a 3 or 4 modulus prescaler allows the minimum division ratio to be lowered.

For a 3 modulus prescaler (R/R+1/R+A)

$$\text{Minimum division ratio} = \underset{\overline{A}}{R(R+A+1)}+A$$

eg. for a 64/65/72 prescaler such as the SP8713

$$\text{Minimum division ratio} = \underset{\overline{8}}{64(64+8+1)}+8 = 1096$$

For a 4 modulus prescaler (R/R+1/R+A/R+B)

$$\text{Minimum division ratio} = \underset{\overline{A}\ \overline{B}}{R(A+B+R+1)}+A+B$$

eg. for a 64/65/68/80 prescaler

$$\text{Minimum division ratio} = \underset{\overline{4}\ \overline{16}}{64(4+16+64+1)}+4+16 = 852$$

An example of where three modulus division would be implemented is given below.

The system in which the synthesiser is to operate has a lowest carrier frequency of 900MHz and a channel spacing of 30kHz. However due to the lock up time requirements fractional-N operation is being used in its 8ths mode (see section on fractional-N operation), giving a comparison frequency of 30kHz x 8 = 240kHz.

Therefore,

$$\text{Minimum division ratio required} = \frac{900\times10^6}{240\times10^3} = 3750$$

If a 64/65 prescaler is used not all the channels will be selectable as the minimum required division ratio is less than the minimum allowable division ratio (4032).

If a 64/65/72 prescaler is used all the channels will now be selectable as the minimum required division ratio will now be greater than the minimum allowable division ratio (1096).

SERIAL DATA BUS

The data needed to program the synthesiser is entered via a high speed (10MBit/s) 3-wire bus, with serial data, serial clock and strobe pins. The input data is partitioned so that after initial programming the output frequency can be changed by re-programming only 24 or 32 bits. The timing diagram for the bus is given in Fig.7.

The data is programmed as either four twenty-four bit words or three twenty-four bit words and one thirty-two bit word. When initially programmed words A, B, C and D are loaded, though if the auxiliary synthesiser is disabled C is not needed. Following the initial programming the frequency can be subsequently shifted in one of the following ways:

a) If a 2 or 3 ratio prescaler is being used and CN does not need to be reprogrammed word A should be loaded.
b) If a 2 or 3 ratio prescaler is being used and CN does need to be reprogrammed word A2 should be loaded. In wide frequency band systems CN must be reprogrammed for best performance every time the frequency is changed.
c) If a four ratio prescaler is being used word A and word B should be loaded

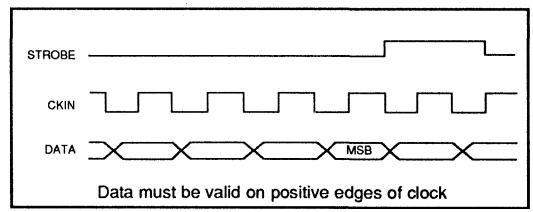


Fig.7

A strobe pulse occurs at the end of each word and loads the contents of the input shift register into the working registers, except when word B is being loaded, in which case the shift register contents are loaded into a temporary register and then loaded into the working register when either word A or A2 is loaded. The information is transferred on the rising edge of the strobe pulse which should occur one half clock period after the clock edge on which the MSB of a word is shifted in.

If word A or word A2 is being loaded, when the strobe goes high the main synthesiser will be put into speed-up mode. This mode will be maintained while the strobe remains high. During this time any pulses on the clock input will not affect the function of the synthesiser.

The information contained within each word is given below. Data bits are shifted in on the leading clock edge, with the least significant bit(LSB) of the word first and the MSB of the word last. (Note that individual sections of data within a word are loaded with the MSB of that section first. An example of this is given after this description of Word A)

Word Format

MSB.....LSB

Word A

```
|0| NF  | N1    |N2 or N2 and N2+N3|
  |3 bits| 12 bits |       8 bits      |
```

NF = Fractional-N incremental value. (MSB first)
N1 = Number of cycles prescaler ratio R1 is used. (MSB first)
N2 = Number of cycles prescaler ratio R2 is used. (MSB first)
N3 = Number of cycles prescaler ratio R3 is used. (MSB first)
If a two modulus prescaler is being used N2= 8 bits.
If a three or four modulus prescaler is being used
N2 = 4 bits and N2+N3= 4 bits(modulo-16 addition).

Therefore if the following values are required NF=3 N1=51 N2=25 the input word would be

```
0        110    110011000000    10011000
         NF        N1              N2
```

Word A2

```
|0|   NF  | N1    |N2 or N2 and  N2+N3 | CN  |
  |3  bits | 12 bits |        8 bits        |8 bits |
```

CN = Scaling factor for current setting. (MSB first)

Word B

```
|1000 |N2+N3+N4| CN  |  K  |  L  | P1,P2 |
      |   4 bits   | 8 bits|4 bits|2 bits| 2 bits |
```

N4 = Number of cycles prescaler ratio R4 is used and (N2+N3+N4) is modulo-16 addition. (MSB first)
CN = Scaling factor for current setting. (MSB first)
K = Acceleration factor for integral charge pump. (MSB first)
L = Acceleration factor for proportional charge pump. (MSB first)
P1,P2 = Number of modulii of prescaler.

No. of modulii	P2	P1
Two	0	0
Three	0	1
Four	1	0

Word C

```
|1001|  NA  |              |
     | 12 bits |  8 bits free  |
```

NA = Variable frequency for auxiliary synthesiser. (MSB first)

Word D

```
|1010 |  NR  |SM1,SM2|  DM  |SA1,SA2| DA|FMOD|LONG|
      |12 bits|  2 bits  | 1 bit  |  2 bits  |1 bit| 1 bit  | 1 bit  |
```

NR = Reference frequency division value. (MSB first)
SM1,SM2 = Main reference source select (Rmain).

SM1	SM2	RMAIN
0	0	M
0	1	2M
1	0	4M
1	1	8M

SA1,SA2 = Auxiliary reference source select (Raux).

SA1	SA2	RAUX
0	0	M
0	1	2M
1	0	4M
1	1	8M

FMOD = Fractional-N modulus select (5 or 8).

FMOD	MODULUS
0	5
1	8

DA = Disable auxiliary synthesiser.

DA=1-disabled
DA=0-enabled

DM = Disable main synthesiser.

DM=1-disabled
DM=0-enabled

LONG = Word A or A2 select.

LONG=0 Word A selected
LONG=1 Word A2 selected

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{dd} = 5V ± 10%, T_{amb} = -40 to +85°C

Static

Parameter	Min	Typ	Max	Unit	Condition
Supply voltage	4.5	5.0	5.5	V	
Supply current		6		mA	Both synthesisers on (Fia = 125MHz, Fim = 30MHz, Ri = 35MHz)
		3	5	mA	Both synthesisers on (Fia = 10MHz, Fim = 10MHz, Ri = 10MHz)
		4		mA	Main on, Auxiliary in stand-by (Fim=30MHz, Ri=35MHz)
		2	3	mA	Main on, Auxiliary in stand-by (Fim=10MHz, Ri =10MHz)
		4		mA	Auxiliary on, Main in stand-by (Fia=125MHz, Ri=35MHz)
		2	3	mA	Auxiliary on, Main in stand-by (Fia=10MHz, Ri=10MHz)
		10		µA	Main and auxiliary in standby

DYNAMIC

AC Characteristics

V_{dd} = 5V ± 10%, T_{amb} = -40 to +85°C

Input signals - RF

Parameter	Min	Typ	Max	Unit	Condition
Input-RI					
Reference input - Ri	10		35	MHz	sinewave input, Note 1
	1		35	MHz	pulse input, Note 1
Rise time			20	ns	
Fall time			20	ns	
Input voltage - Ri	0.1		1	V_{pk-pk}	Ri = 20-35MHz, Note 1
	0.25		1	V_{pk-pk}	Ri = 10-19MHz, Note 1
Input capacitance			10	pF	
Large signal input impedance	200			kΩ	Note 2
Source impedance Z_s			1.5	kΩ	Note 3
Aux synthesiser input -FIA					
Input frequency - Fia	20		125	MHz	sinewave input, Note 1
	1		125	MHz	pulse input, Note 1
Rise time			10	ns	
Fall time			10	ns	
Input voltage	0.35		1	V_{pk-pk}	Fia = 20-49MHz, Note 1
	0.1		1	V_{pk-pk}	Fia = 50-99MHz, Note 1
	0.35		1	V_{pk-pk}	Fia = 100-125MHz, Note 1
Input capacitance			10	pF	
Large signal input impedance	200			kΩ	Note 2
Source impedance			1.5	kΩ	Note 3
Main synthesiser input -FIM					
Input frequency - Fim	10		30	MHz	sinewave input
	1		30	MHz	pulse input
Rise time			50	ns	
Fall time			50	ns	
Input voltage	0.2		1	V_{pk-pk}	Single ended input
Common mode input DC voltage range	2.8		V_{dd}-1	V	
Input capacitance			10	pF	
Input impedance	100			MΩ	
Input Current			10	µA	

Notes

1. Source impedance = 50Ω
2. Virtual earth input amplifier, therfore low impedance for small signals. Impedance is high once signal amplitude exceeds typically ±0.125V.
3. Input amplifier may become unstable for higher values of Z_s.

DYNAMIC

AC Characteristics

V_{dd} = 5V ± 10%, T_{amb} = -40 to +85°C

Input signals - Logic and current defining pins

Parameter	Min	Typ	Max	Unit	Condition
Data and strobe					
Input voltage high	V_{dd}-0.8		V_{dd}	V	
Input voltage low	0		0.8	V	
Input capacitance			10	pF	
Input current			10	µA	
Clock					
Input voltage high	V_{dd}-0.8		V_{dd}	V	
Input voltage low	0		0.8	V	
Input capacitance			10	pF	
Input current			10	µA	
Input frequency			10	MHz	
Current setting pins					
Input Signal RSA		80		µA	Notes 1, 4
Input current					
Input Signal RSM		32		µA	Notes 2, 4
Input current					
Input Signal RSC		12.8		µA	Notes 3, 4
Input current					

Notes

1. The current set on pin RSA will be scaled up on chip by a factor of 3 to give the value of the auxiliary phase detector output.
2. The current set on pin RSM will be scaled down on chip by a factor of 32 to provide the current I_{bo} to the main phase detector which gives the outputs I_{prop} and I_{int}.
3. The current set on pin RSC will be scaled down on chip by a factor of 128 to provide the current I_{co} to the main phase detector which gives the outputs I_{comp} and $I_{comp\ 2}$.
4. The voltage on each of the three current setting pins (RSA, RSM, RSC) is approximately 4V. Therefore to give a typical current of 32µA on RSM for example, a 125kΩ resistor connected between the pin and GND would be required.

DYNAMIC

V_{dd} = 5V ± 10%, T_{amb} = -40 to +85°C

Output signals

Parameter	Min	Typ	Max	Unit	Condition
Modulus control - MOD1 MOD2					Push-Pull output
Output voltage high	V_{dd}-0.4		V_{dd}	V	I_{OH} = 0.5mA
Output voltage low	0		0.4	V	I_{OL} = 0.5mA

Modulus output truth table

MOD2	MOD1	Prescaler modulus
0	1	R1
0	0	R2
1	0	R3
1	1	R4

DYNAMIC

V_{dd} = 5V, T_{amb} = -40 to +85°C

Output signals - Auxiliary synthesiser

Parameter	Min	Typ	Max	Unit	Condition
Output signal - PDA					
Up current - See Note 5	-10%	I_{pda}	+10%	µA	0<V_{PD}<4.35V
Down current - See Note 5	-10%	I_{pda}	+10%	µA	0.65<V_{PD}<5V
Tristate			10	nA	

DYNAMIC

V_{dd} = 5V, T_{amb} = -40 to +85°C

Output signals - Main synthesiser, proportional output

Parameter	Min	Typ	Max	Unit	Condition
Output signal - PDP					
Iprop(0) Up *see notes 1, 3 & 4*	-10%	$+I_{bo}.CN$	+10%	µA	0<V_{PD}<4.55V, Strobe=0V
Iprop(0) Down *see notes 1, 3 & 4*	-10%	$-I_{bo}.CN$	+10%	µA	0.45<V_{PD}<5V, Strobe=0V
Iprop(1) Up *see notes 2&3*	-10%	$+I_{bo}.CN.2^{L+1}$	+10%	µA	0<V_{PD}<4.55V, Strobe=5V
Iprop(1) Down *see notes 2&3*	-10%	$-I_{bo}.CN.2^{L+1}$	+10%	µA	0.45<V_{PD}<5V, Strobe=5V
Tristate			50	nA	

Notes

1. The typical value of $I_{PROP(0)}$ is set by the programmed value of ***CN*** and the current I_{rsm} set by the external resistor RSM, where $I_{bo}=I_{rsm}/32$. I_{rsm} is typically 32µA.
2. The typical value of $I_{PROP(1)}$ is set by the value of $I_{PROP(0)}$ and the programmed value of ***L***.
3. The current output I_{PROP} is specified between 100µA and 1mA.
4. The output current is monotonic over the CN range 128-255. In standard operation CN is set at a value > 128.
5. Where I_{pda} depends on the value of current setting resistor on RSA pin (9). I_{pda} max = 250µA

DYNAMIC

V_{dd} = 5V, T_{amb} = -40 to +85°C

Output signals - Main synthesiser, integral output

Parameter	Min	Typ	Max	Unit	Condition
Output signal - PDI					
I_{INT} Up (1mA - 5mA) *see notes 1&2*	-10%	$+I_{bo}.CN.2^{L+1}.K$	+10%	mA	$0<V_{PD}<4.45V$, Strobe=5V
I_{INT} Down (1mA - 5mA) *see notes 1&2*	-10%	$-I_{bo}.CN.2^{L+1}.K$	+10%	mA	$0.35<V_{PD}<5V$, Strobe=5V
I_{INT} Up (5mA - 10mA) *see notes 1&2*	-10%	$+I_{bo}.CN.2^{L+1}.K$	+10%	mA	$0<V_{PD}<4.3V$, Strobe=5V
I_{INT} Down (5mA - 10mA) *see notes 1&2*	-10%	$-I_{bo}.CN.2^{L+1}.K$	+10%	mA	$0.5<V_{PD}<5V$, Strobe=5V
Tristate			50	nA	

Notes

1. The typical value of I_{INT} is set by the value of ***Iprop(1)*** and the programmed value of **K**.
2. The current output I_{INT} is specified between 1mA and 10mA.

DYNAMIC

V_{dd} = 5V, T_{amb} = -40 to +85°C

Output signals - Main synthesiser, under Fractional-N control

Parameter	Min	Typ	Max	Unit	Condition
Output signal - PDP					
$I_{COMP}(0)$ *see notes 1&3*	-10%	$I_{co}.Acc.$	+10%	µA	$0<V_{PD}<4.55V$, Strobe=0V
I_{COMP} (1) *see notes 2&3*	-10%	$I_{co}.Acc.2^{L+1}.$	+10%	µA	$0<V_{PD}<4.55V$, Strobe=5V
Output signal - PDI					
$I_{COMP}2$ *see notes 4&5*	-10%	$I_{co}.Acc.2^{L+1}.K$	+10%	µA	$0<V_{PD}<4.55V$, Strobe=5V

Notes

1. The typical value of $I_{COMP}(0)$ is set by the fractional-N accumulator value Acc and the current I_{rsc} set by the external resistor RSC, where $I_{co}=I_{rsc}/128$. I_{rsc} is typically 12.8µA.
2. The typical value of $I_{COMP}(1)$ is set by the value of $I_{COMP}(0)$ and the programmed value of ***L***.
3. The current output I_{COMP} is specified up to 12µA.
4. The typical value of $I_{COMP}2$ is set by the value of $I_{COMP}(1)$ and the programmed value of ***K***.
5. The current output $I_{COMP}2$ is specified up to 180µA.

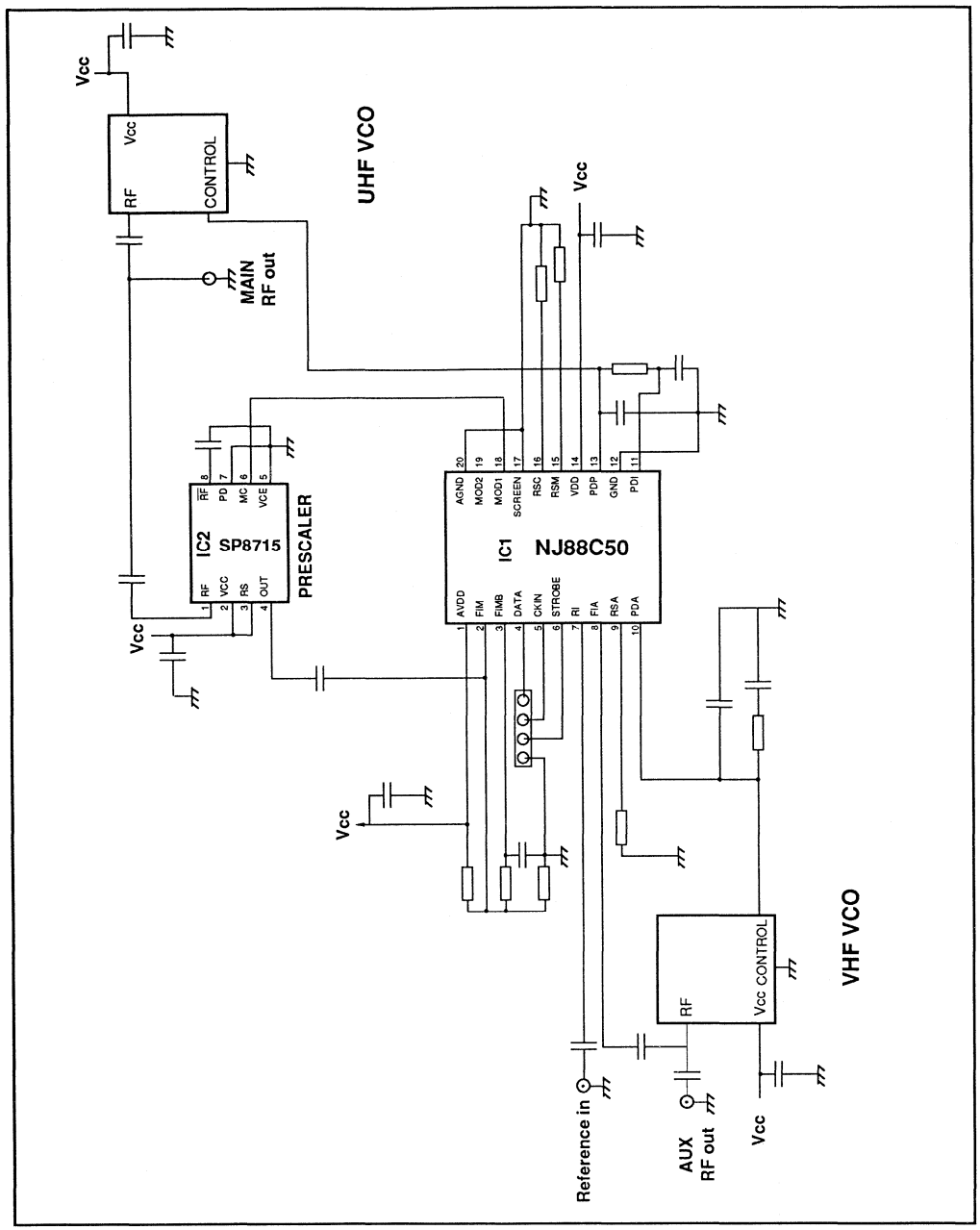


Fig.8 Typical application

Fig.8 shows a typical application, using the NJ88C50 to generate both VHF and UHF signals. External components are kept to a minimum, requiring only bias, loop filter and decoupling components. In many applications the UHF VCO is a pre-assembled and tested module to suit the end equipment use, whereas the VHF design is likely to be discrete. The circuit shown is suitable for operation up to 1.1GHz and uses a low power prescaler, the SP8715, feeding the NJ88C50 in single ended mode. This requires a biasing network around the differential input of the NJ88C50 to be used (pins 2 and 3).

Power supply and ground rails must have adequate decoupling otherwise overall performance may be impaired.

Section 2
Prescalers

GEC PLESSEY
SEMICONDUCTORS

SP8713

1100MHz VERY LOW CURRENT THREE MODULUS DIVIDER

The SP8713 is a switchable divide by 64/65/72 programmable divider which is guaranteed to operate up to 1100MHz. It will operate from a supply of 2.7V to 5.5V and requires typically 4.1mA (including the output current). It also features a power down facility for battery economy.

The RF inputs are internally biased and should be capacitively coupled to the signal source. The output is designed to interface with CMOS synthesisers, such as the NJ88C51.

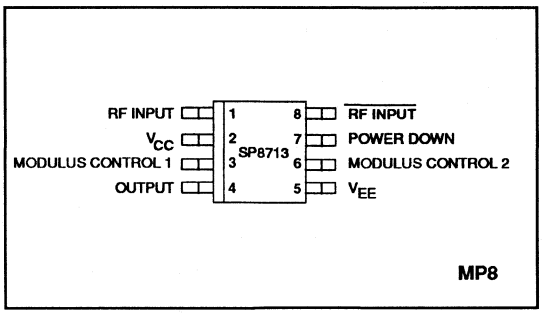


Fig. 1 Pin connections - top view

FEATURES

- Operation to 1100MHz
- Very Low Power
- Single Supply Operation 2.7V to 5.5V
- Power Down Facility for Battery Economy
- Latched Modulus Control Inputs
- Push Pull Output Drive
- ESD Protection on All Pins†

APPLICATIONS

- Cellular Telephones
- Cordless Telephones
- Mobile Radio

† ESD precautions must be observed

ORDERING INFORMATION

SP8713 IG MPAS Industrial Temperature Range
Miniature Plastic DIL Package

SP8713 IG MPAC As above supplied on Tape and Reel

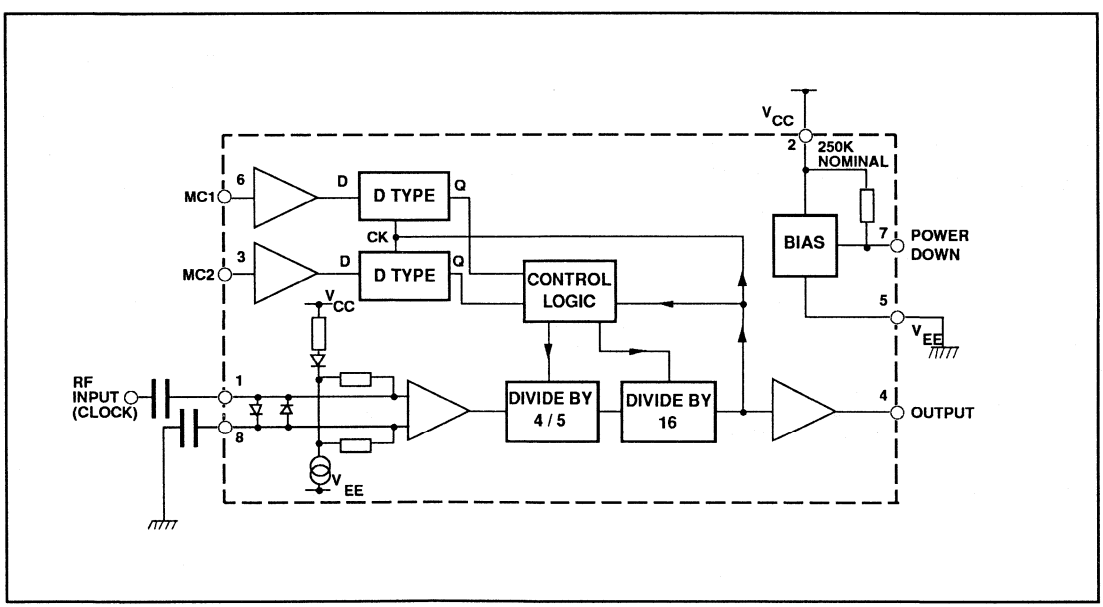


Fig. 2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{EE}=0V)	(note 1)	-0.5V to 7V
Control and RF inputs, RF output (V_{EE} =0V)	(note 1)	-0.5V to V_{CC}+0.5V
RF input current	(note 1)	10mA
Operating temperature		-40°C to +85°C
Storage temperature range		-55°C to +150°C
Maximum junction temperature		+150°C

NOTE 1. Duration <2 minutes.

ELECTRICAL CHARACTERISTICS

Guaranteed over the following conditions (unless otherwise stated):

V_{CC}=+2.7V to +5.5V (with respect to V_{EE}), Output load (pin 4) = 10pF, T_{amb} = -40°C to +85°C (note 2)

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	(note 3)		4.1	4.7	mA	Power down input low
Supply current	(note 3)		8	50	µA	Power down input high
Power down high		V_{CC}-0.5		V_{CC}	V	
Power down low		0		V_{CC}-2.0	V	
Modulus control 1 high	(note 4)	0.6V_{CC}		V_{CC}	V	Divide by 64 or 72
Modulus control 1 low	(note 4)	0		0.4V_{CC}	V	Divide by 65 or 72
Modulus control 2 high	(note 4)	0.6V_{CC}		V_{CC}	V	Divide by 72
Modulus control 2 select low	(note 4)	0		0.4V_{CC}	V	Divide by 64 or 65
Max. sinewave input frequency		1100			MHz	See Figure 5
Min. sinewave input frequency				200	MHz	See Figure 5
Min. RF input voltage				50	mV RMS	RF input 200MHz to 1100MHz. See Figure 5
Max. RF input voltage		200			mV RMS	RF input 200MHz to 1100MHz. See Figure 5
Output level (pin 4)		500	600		mV p-p	
Modulus set-up time, t_s	(notes 5,6,8)	20			ns	RF input = 1GHz
Modulus hold time, t_h	(notes 6,8)			1	ns	RF input = 1GHz
Power down time, t_{pd}	(notes 7,8)			10	µs	See Figure 9
Power down recovery time, t_{pu}	(notes 7,8)			6	µs	See Figure 9

NOTES

2. All electrical testing is performed at +85°C.
3. Typical values are measured at +25°C and V_{CC} = +5V.
4. Modulus Control and Ratio Select are high impedance inputs which can be driven directly by standard CMOS outputs.
5. Modulus control is latched at the end of the previous cycle.
6. See Figure 4.
7. See Figure 8.
8. These parameters are not tested but are guranteed by design.

OPERATING NOTES

The RF inputs are biased internally and are normally coupled to the signal source with suitable capacitors.

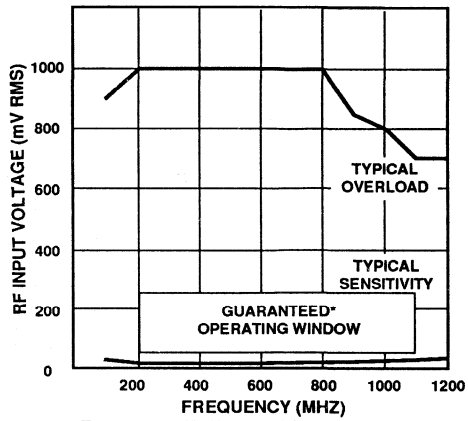
The output stage has a novel design and is intended to drive a CMOS synthesiser input. External pull-down resistors or circuits are not required. The SP8713 is not suitable for driving TTL or similar devices.

The device will operate down to DC frequencies for non-sinusoidal signals provided that the input slew rate is better than 100V/µs.

POWER DOWN (pin 7) is connected internally to a pull-up resistor. If the battery economy facility is not used, pin 7 should be connected to V_{EE}.

Modulus Control 1 (Pin 3)	Modulus Control 2 (Pin 6)	Division Ratio
L	L	65
H	L	64
H	H	72
L	H	72

Table 1 Truth table



* Tested as specified in table of Electrical Characteristics

Fig. 3 Typical input characteristics

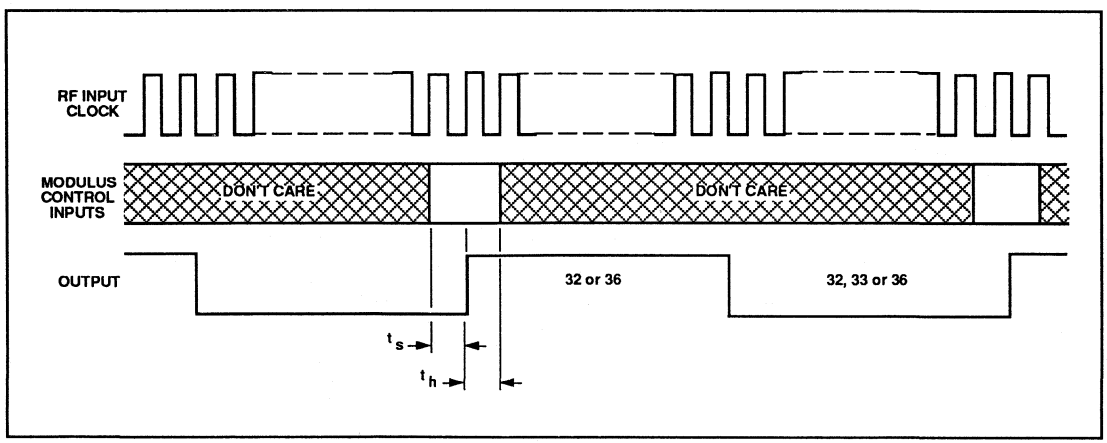


Fig. 4 Modulus control timing diagram

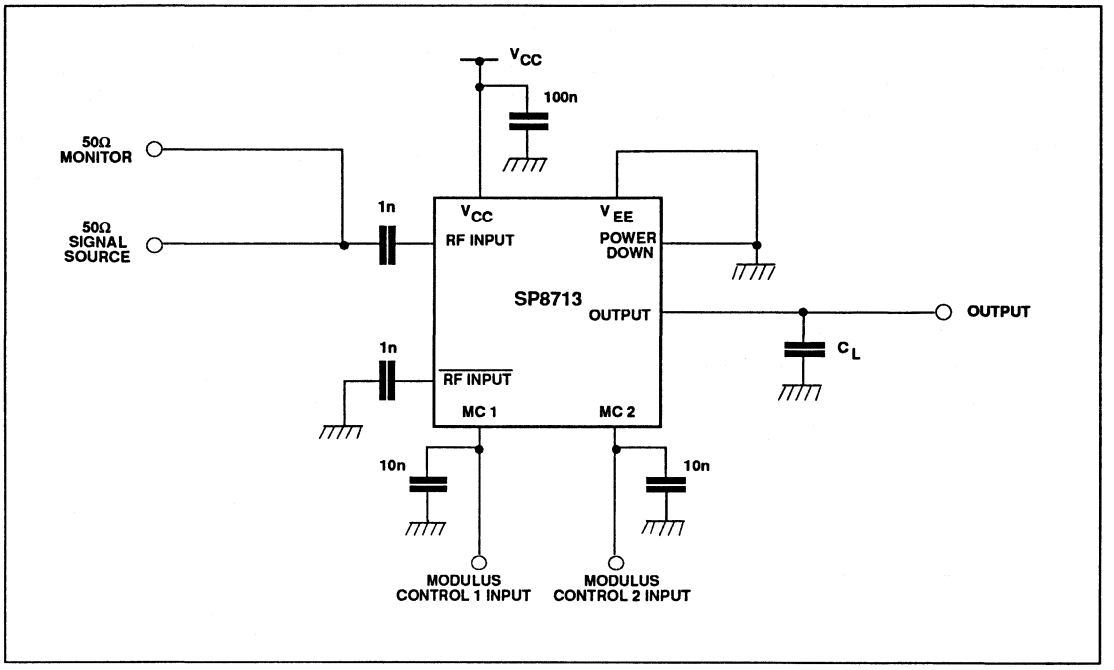


Fig. 5 Toggle frequency test circuit

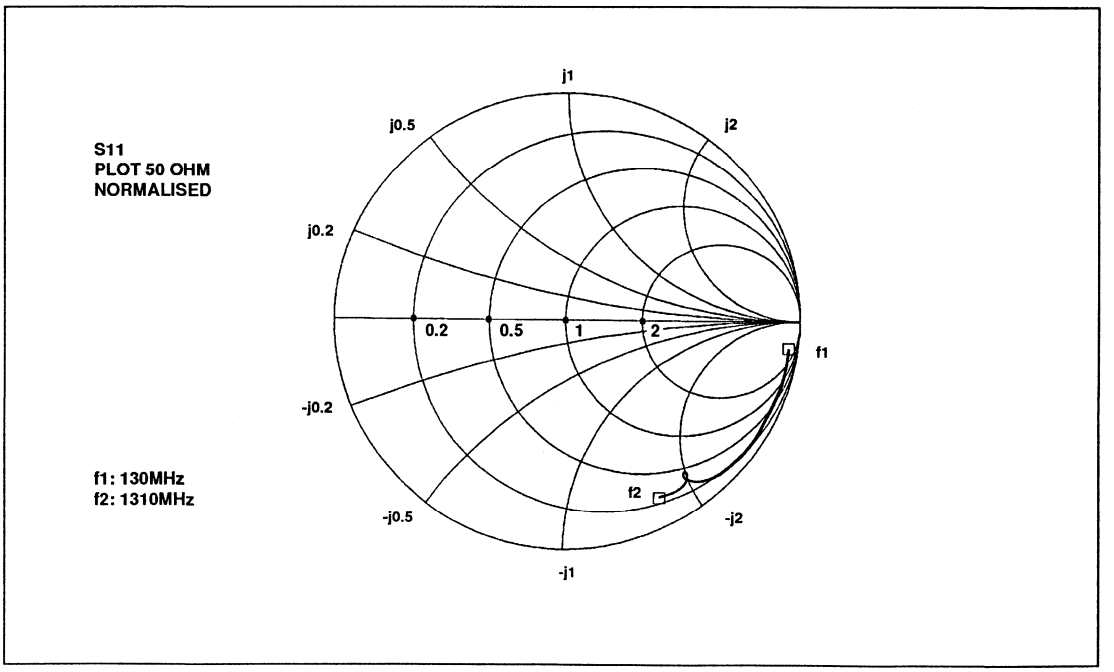


Fig. 6 Typical S11 parameter for pin 1. V_{CC} = +5.0V

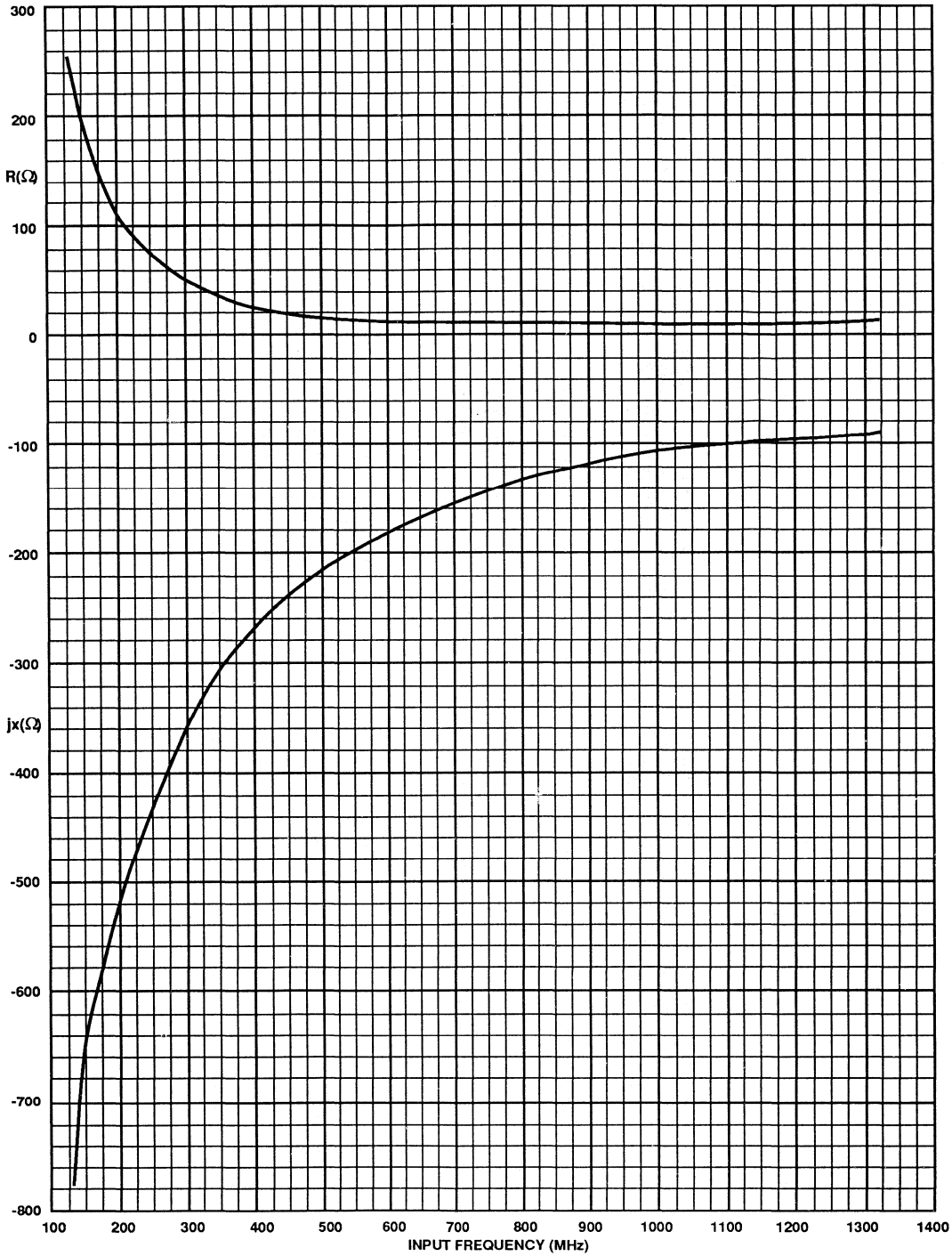


Fig. 7 Typical input impedance v. frequency

FREQ-MHZ	R (Ω)	jx (Ω)
130.000	255.068	-733.538
153.600	153.362	-688.623
177.200	153.330	-583.339
200.800	115.187	-545.839
224.400	88.649	-482.377
248.000	80.815	-441.798
271.600	71.050	-411.502
295.200	56.207	-369.645
318.800	39.526	-346.620
342.400	41.338	-323.129
366.000	38.779	-304.804
389.600	39.210	-280.556
413.200	23.809	-269.674
436.800	21.221	-255.279
460.400	27.545	-245.161
484.000	23.333	-234.680
507.600	22.227	-224.572
531.200	19.931	-211.375
554.800	17.767	-203.241
578.400	17.636	-194.613
602.000	14.607	-186.545
625.600	12.479	-182.049
649.200	13.075	-174.839
672.800	12.891	-168.320
696.400	12.583	-160.468
720.000	11.250	-156.267
743.600	10.213	-149.642
767.200	10.187	-145.328
790.800	11.269	-143.144
814.400	11.081	-137.557
838.000	10.509	-132.750
861.600	10.063	-129.254
885.200	10.172	-124.495
908.800	10.745	-120.568
932.400	10.841	-118.100
956.000	10.884	-113.395
979.600	12.260	-109.552
1003.20	12.984	-105.975
1026.80	14.508	-103.110
1050.40	16.625	-99.886
1074.00	19.260	-98.149
1097.60	22.799	-98.605
1121.20	23.285	-99.907
1144.80	21.149	-100.925
1168.40	18.956	-99.639
1192.00	16.434	-98.425
1215.60	14.377	-95.033
1239.20	13.743	-92.553
1262.80	12.711	-89.249
1286.40	12.776	-86.081
1310.00	12.598	-82.581

Table.2 Coefficients for Fig.7

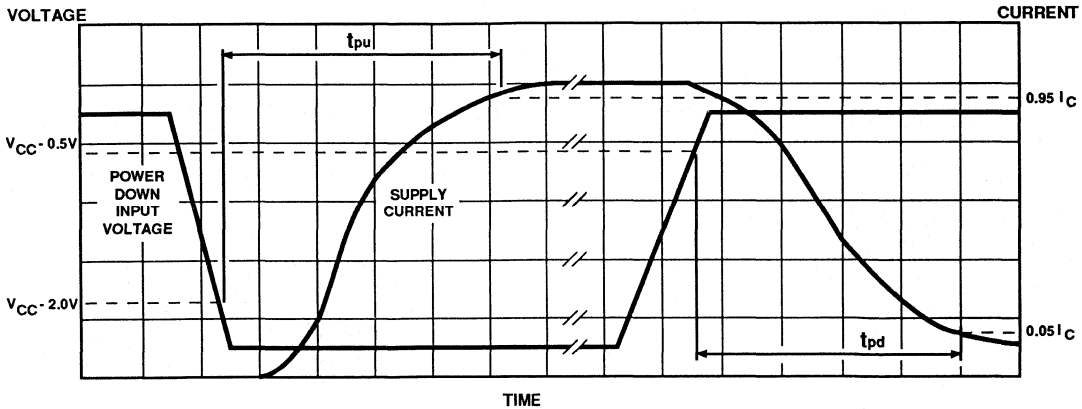


Fig. 8 Power up and power down

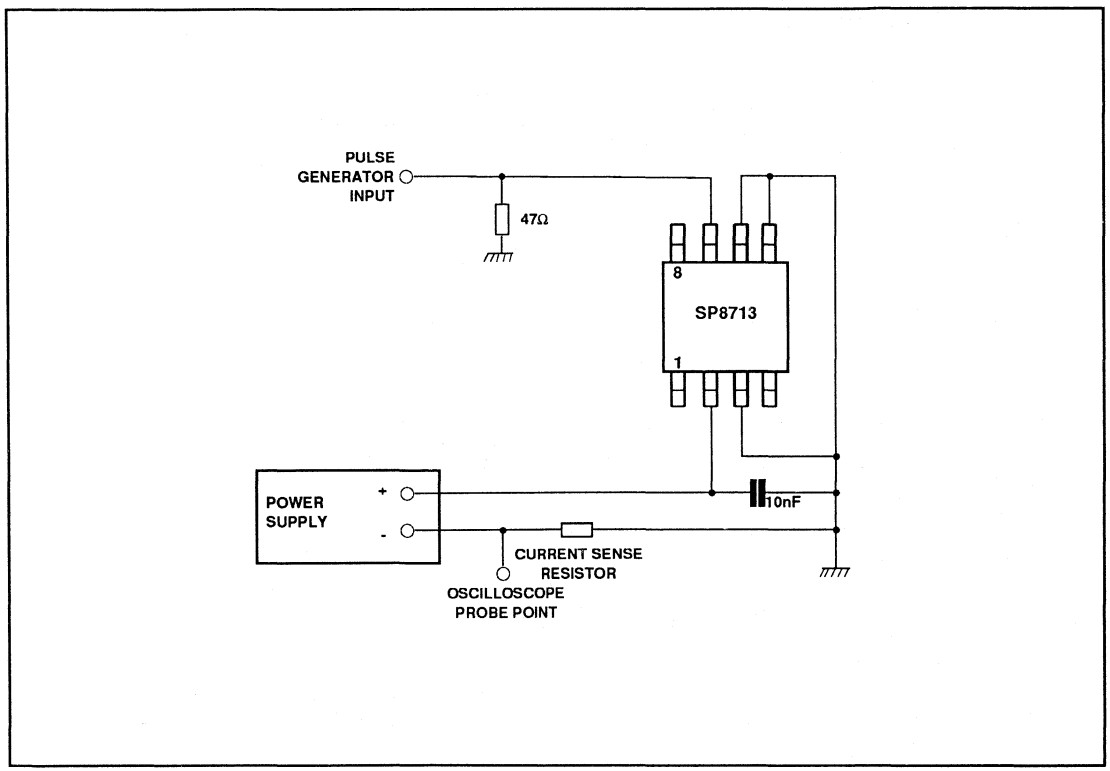


Fig. 9 Power-down time test circuit

SP8714

2100MHz VERY LOW CURRENT MULTI-MODULUS DIVIDER

The SP8714 is a switchable divide by 32/33, 64/65 programmable divider which is guaranteed to operate up to 2100MHz. It will operate from a supply of 2.7V to 5.5V and requires typically 6.8mA (including the output current). It also features a power down facility for battery economy.

The RF inputs are internally biased and should be capacitively coupled to the signal source. The output is designed to interface with CMOS synthesisers.

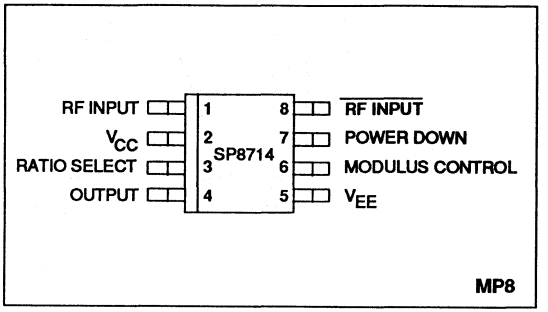


Fig. 1 Pin connections - top view

FEATURES

- Operation to 2100MHz
- Very Low Power
- Single Supply Operation 2.7V to 5.5V
- Power Down Facility for Battery Economy
- Latched Modulus Control Input
- Push Pull Output Drive
- ESD Protection on All Pins†

APPLICATIONS

- Cellular Telephones
- Cordless Telephones

† ESD precautions must be observed

ORDERING INFORMATION

SP8714 IG MPAS Industrial Temperature Range Miniature Plastic DIL Package

SP8714 IG MPAC As above supplied on Tape and Reel

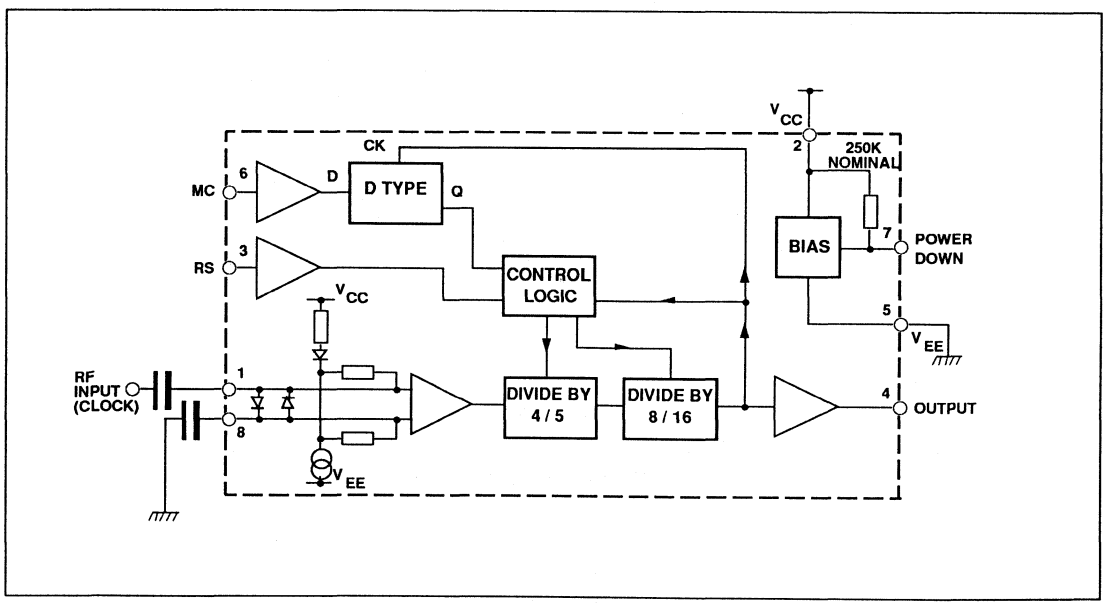


Fig. 2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{EE}=0V)	(note 1)	-0.5V to 7V
Control and RF inputs, RF output (V_{EE} =0V)	(note 1)	-0.5V to V_{CC}+0.5V
RF input current	(note 1)	10mA
Operating temperature		-40°C to +85°C
Storage temperature range		-55°C to +150°C
Maximum junction temperature		+150°C

NOTE 1. Duration <2 minutes.

ELECTRICAL CHARACTERISTICS

Guaranteed over the following conditions (unless otherwise stated):

V_{CC}=+2.7V to +5.5V (with respect to V_{EE}), Output load (pin 4) = 10pF, T_{amb} = -40°C to +85°C (note 2)

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	(note 3)		6.8	8.5	mA	Power down input low
Supply current	(note 3)		8	50	µA	Power down input high
Power down high		V_{CC}-0.5		V_{CC}	V	
Power down low		0		V_{CC}-2.0	V	
Modulus control high	(note 4)	0.6V_{CC}		V_{CC}	V	Divide by 32 or 64
Modulus control low	(note 4)	0		0.4V_{CC}	V	Divide by 33 or 65
Ratio select high	(note 4, 9)	0.6V_{CC}		V_{CC}	V	Divide by 32 or 33
Ratio select low	(note 4, 9)	0		0.4V_{CC}	V	Divide by 64 or 65
Max. sinewave input frequency		2100			MHz	See Figure 5
Min. sinewave input frequency				200	MHz	See Figure 5
Min. RF input voltage				50	mV RMS	RF input 200MHz to 2100MHz. See Figure 5
Max. RF input voltage		200			mV RMS	RF input 200MHz to 2100MHz. See Figure 5
Output level (pin 4)		500	600		mV p-p	
Modulus set-up time, t_s	(notes 5,6,8)	10			ns	RF input = 1GHz
Modulus hold time, t_h	(notes 6,8)			1	ns	RF input = 1GHz
Power down time, t_{pd}	(notes 7,8)			10	µs	See Figure 9
Power down recovery time, t_{pu}	(notes 7,8)			8	µs	See Figure 9

NOTES

2. All electrical testing is performed at +85°C.
3. Typical values are measured at +25°C and V_{CC} = +5V.
4. Modulus Control and Ratio Select are high impedance inputs which can be driven directly by standard CMOS outputs.
5. Modulus control is latched at the end of the previous cycle.
6. See Figure 4.
7. See Figure 8.
8. These parameters are not tested but are guaranteed by design.
9. The ratio select pin is not intended to be switched dynamically.

OPERATING NOTES

The RF inputs are biased internally and are normally coupled to the signal source with suitable capaitors.

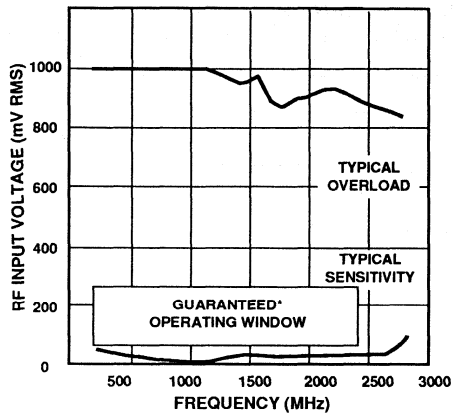
The output stage has a novel design and is intended to drive a CMOS synthesiser input. External pull-down resistors or circuits are not required. The SP8714 is not suitable for driving TTL or similar devices.

The device will operate down to DC frequencies for non-sinusoidal signals provided that the input slew rate is better than 100V/μs.

POWER DOWN (pin 7) is connected internally to a pull-up resistor. If the battery economy facility is not used, pin 7 should be connected to V_{EE}.

Ratio Select (Pin 3)	Modulus Control (Pin 6)	Division Ratio
L	L	65
L	H	64
H	L	33
H	H	32

Table 1 Truth table



* Tested as specified in table of Electrical Characteristics

Fig. 3 Typical input characteristics

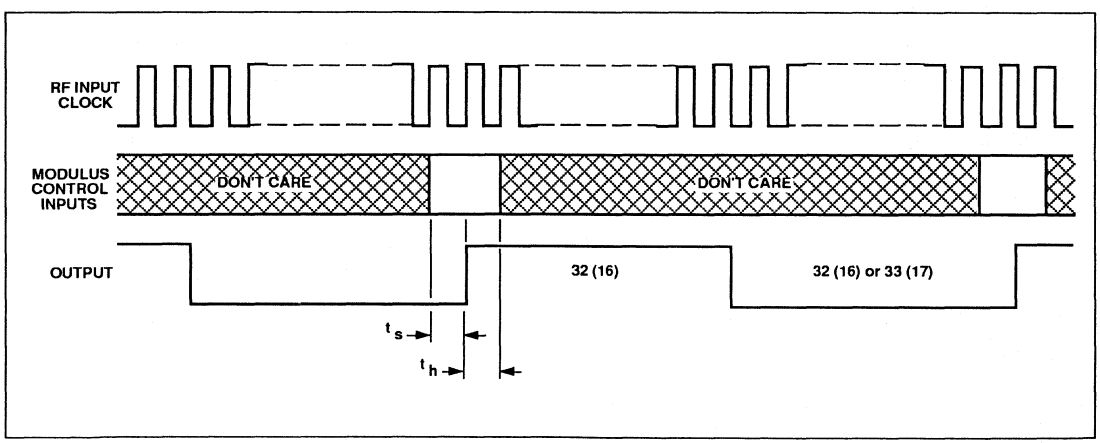


Fig. 4 Modulus control timing diagram

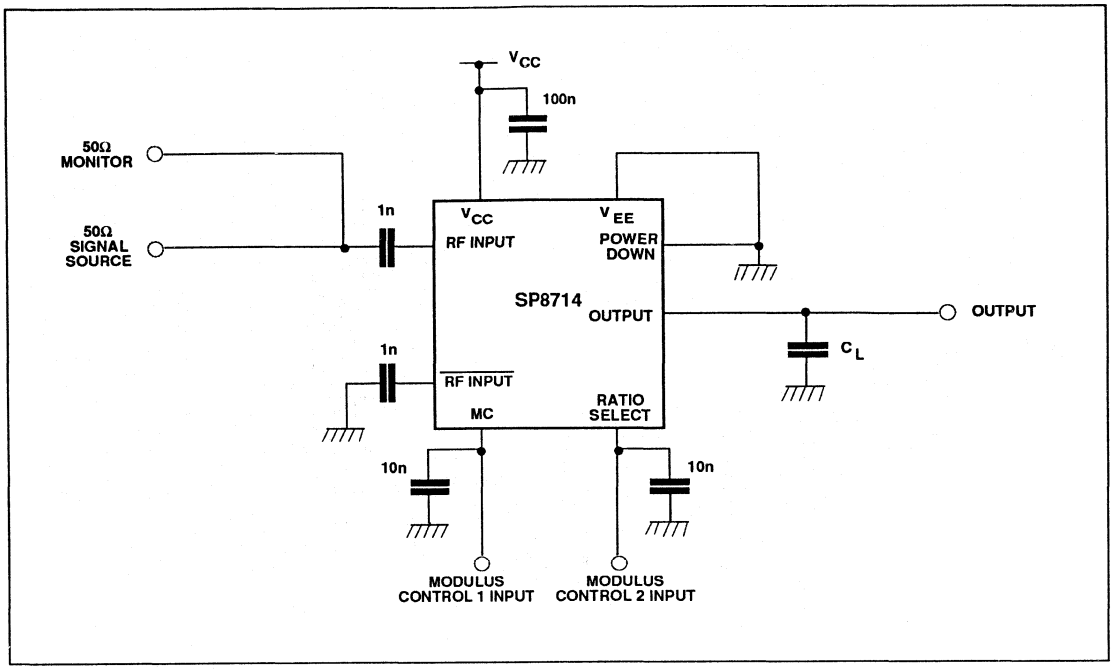


Fig. 5 Toggle frequency test circuit

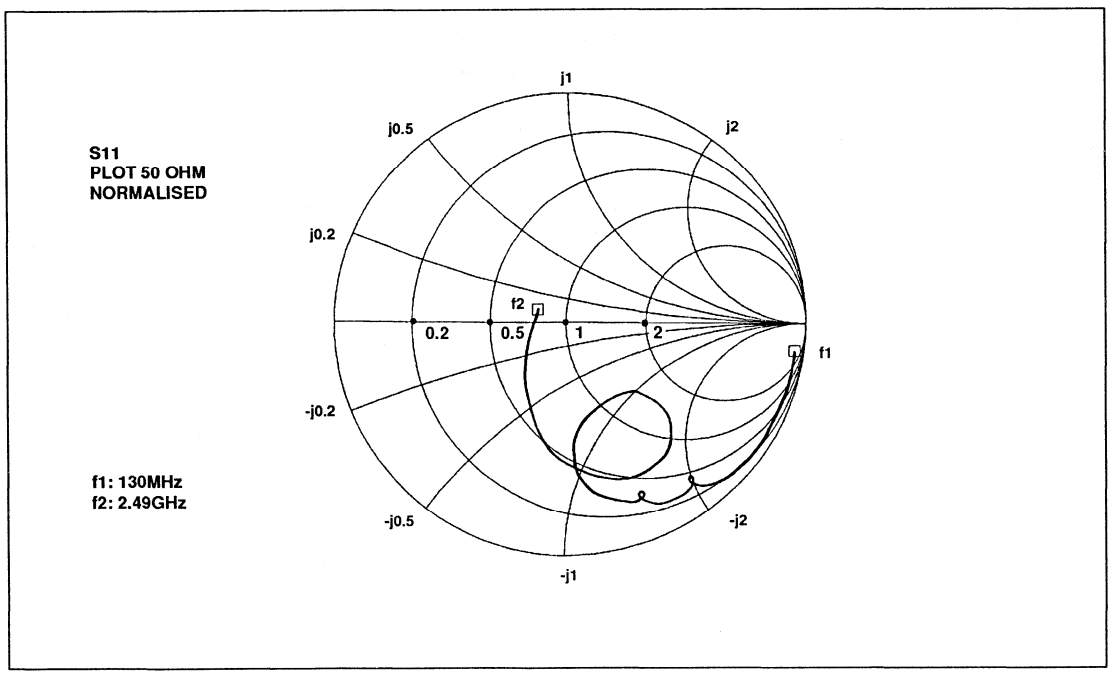


Fig. 6 Typical S11 parameter for pin 1. V_{CC} = +5.0V

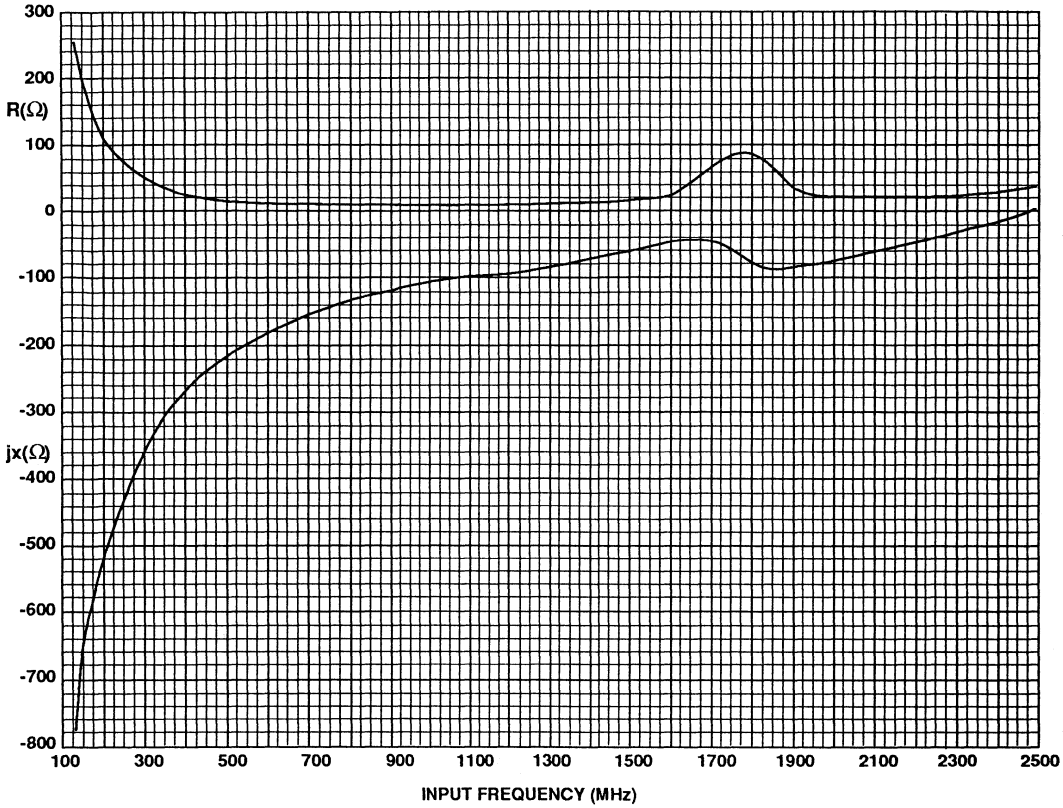


Fig. 7 Typical input impedance v. frequency

FREQ-MHZ	R (Ω)	jx (Ω)
130.000	255.068	-733.538
177.200	153.330	-583.339
224.400	88.649	-482.377
271.600	71.050	-411.502
318.800	39.526	-346.620
366.000	38.779	-304.804
413.200	23.809	-269.674
460.400	27.545	-245.161
507.600	22.227	-224.572
554.800	17.767	-203.241
602.000	14.607	-186.545
649.200	13.075	-174.839
596.400	12.583	-160.468
743.600	10.213	-149.642
790.800	11.269	-143.144
838.000	10.509	-132.750
885.200	10.172	-124.495
332.400	10.841	-118.100
979.600	12.260	-109.552
1026.80	14.508	-103.110
1074.00	19.260	-98.149
1121.20	23.285	-99.907
1168.40	18.956	-99.639
1215.60	14.377	-95.033
1262.80	12.711	-89.249
1310.00	12.598	-82.581
1357.20	14.565	-77.212
1404.40	19.164	-71.976
1451.60	15.001	-70.250
1498.80	15.864	-61.898
1546.00	18.993	-53.403
1593.20	26.822	-44.704
1640.40	39.830	-41.522
1687.60	47.875	-43.255
1734.80	63.267	-44.879
1782.00	74.259	-67.801
1829.20	58.878	-86.964
1876.40	42.530	-87.052
1923.60	32.302	-80.484
1970.80	27.333	-73.570
2018.00	24.894	-67.291
2065.20	23.369	-60.620
2112.40	23.577	-54.716
2159.60	23.023	-49.220
2206.80	23.325	-43.340
2254.00	24.623	-37.163
2301.20	26.340	-30.805
2348.40	28.632	-24.040
2395.60	31.161	-17.165
2442.80	34.219	-8.172
2490.00	39.808	-4.368

Table.2 Coefficients for Fig.7

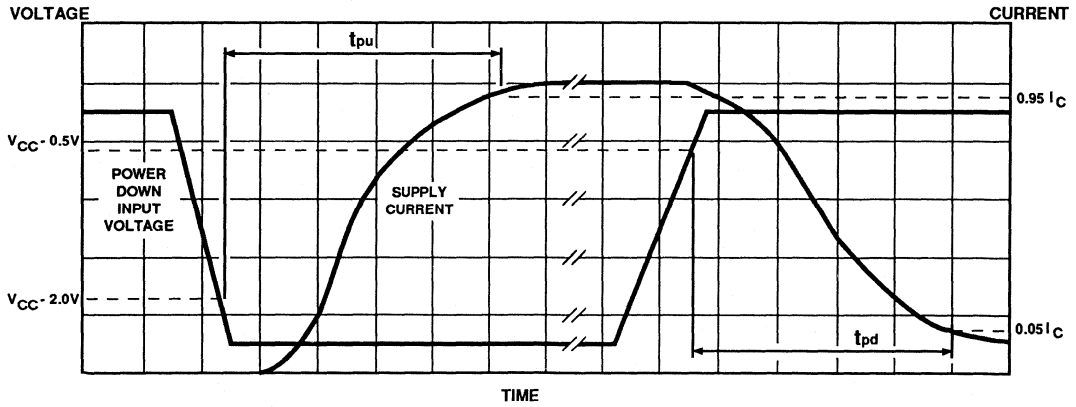


Fig. 8 Power up and power down

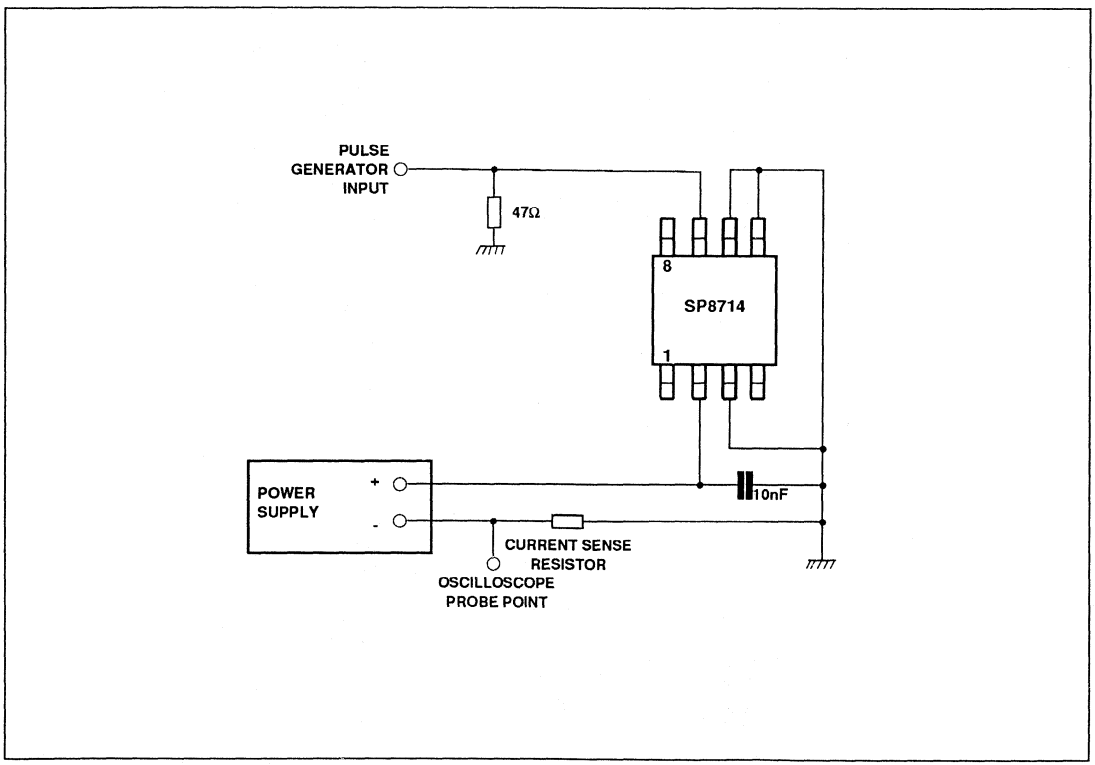


Fig. 9 Power-down time test circuit

SP8715

1100MHz VERY LOW CURRENT MULTI-MODULUS DIVIDER

The SP8715 is a switchable divide by 64/65, 128/129 programmable divider which is guaranteed to operate up to 1100MHz. It will operate from a supply of 2.7V to 5.5V and requires typically 3.6mA (including the output current). It also features a power down facility for battery economy.

The RF inputs are internally biased and should be capacitively coupled to the signal source. The output is designed to interface with CMOS synthesisers.

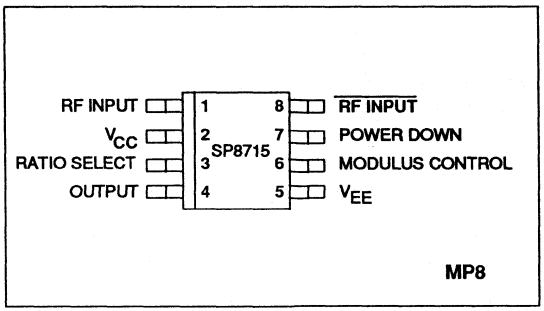


Fig. 1 Pin connections - top view

FEATURES

- Operation to 1100MHz
- Very Low Power
- Single Supply Operation 2.7V to 5.5V
- Power Down Facility for Battery Economy
- Latched Modulus Control Input
- Push Pull Output Drive
- ESD Protection on All Pins†

APPLICATIONS

- Cellular Telephones
- Cordless Telephones
- Mobile Radio

† ESD precautions must be observed

ORDERING INFORMATION

SP8715 IG MPAS Industrial Temperature Range Miniature Plastic DIL Package

SP8715 IG MPAC As above supplied on Tape and Reel

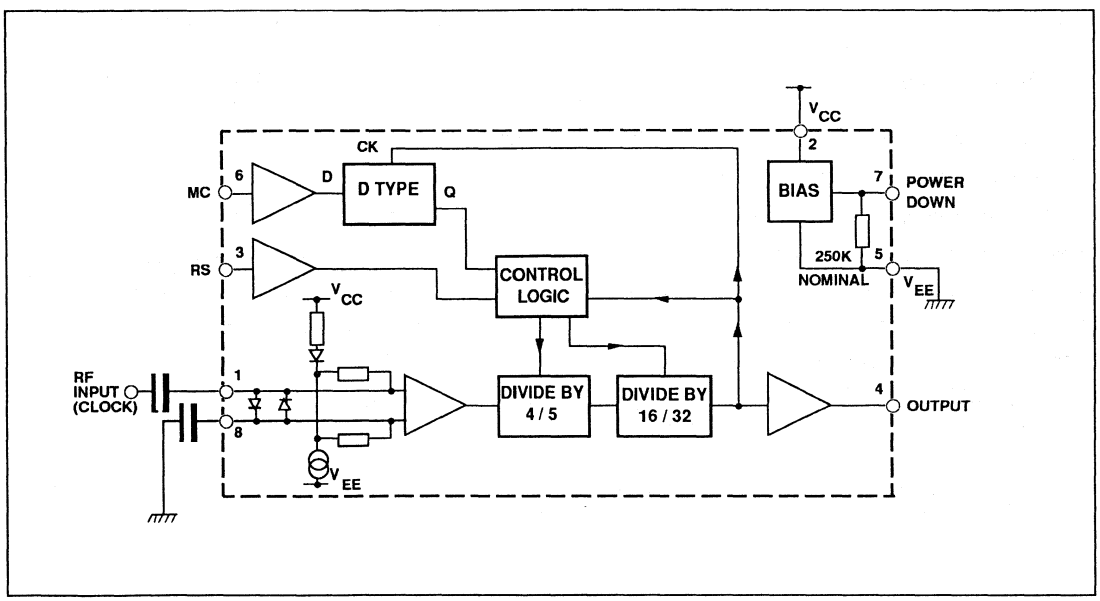


Fig. 2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{EE}=0V)	(note 1)	-0.5V to 7V
Control and RF inputs, RF output (V_{EE} =0V)	(note 1)	-0.5V to V_{CC}+0.5V
RF input current	(note 1)	10mA
Operating temperature		-40°C to +85°C
Storage temperature range		-55°C to +150°C
Maximum junction temperature		+150°C

NOTE 1. Duration <2 minutes.

ELECTRICAL CHARACTERISTICS

Guaranteed over the following conditions (unless otherwise stated):

V_{CC}=+2.7V to +5.5V (with respect to V_{EE}), Output load (pin 4) = 10pF, T_{amb} = -40°C to +85°C (note 2)

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	(note 3)		3.6	4.2	mA	Power down input low
Supply current	(note 3)		8	50	µA	Power down input high
Power down high		V_{CC}-0.5		V_{CC}	V	
Power down low		0		V_{CC}-2.0	V	
Modulus control high	(note 4)	0.6V_{CC}		V_{CC}	V	Divide by 64 or 128
Modulus control low	(note 4)	0		0.4V_{CC}	V	Divide by 65 or 129
Ratio select high	(note 4, 9)	0.6V_{CC}		V_{CC}	V	Divide by 64 or 65
Ratio select low	(note 4, 9)	0		0.4V_{CC}	V	Divide by 128 or 129
Max. sinewave input frequency		1100			MHz	See Figure 5
Min. sinewave input frequency				200	MHz	See Figure 5
Min. RF input voltage				50	mV RMS	RF input 200MHz to 1100MHz. See Figure 5
Max. RF input voltage		200			mV RMS	RF input 200MHz to 1100MHz. See Figure 5
Output level (pin 4)		500	600		mV p-p	
Modulus set-up time, t_s	(notes 5,6,8)	20			ns	RF input = 1GHz
Modulus hold time, t_h	(notes 6,8)			1	ns	RF input = 1GHz
Power down time, t_{pd}	(notes 7,8)			10	µs	See Figure 9
Power down recovery time, t_{pu}	(notes 7,8)			6	µs	See Figure 9

NOTES

2. All electrical testing is performed at +85°C.
3. Typical values are measured at +25°C and V_{CC} = +5V.
4. Modulus Control and Ratio Select are high impedance inputs which can be driven directly by standard CMOS outputs.
5. Modulus control is latched at the end of the previous cycle.
6. See Figure 4.
7. See Figure 8.
8. These parameters are not tested but are guaranteee by design.
9. The ratio select pin is not intended to be switched dynamically.

OPERATING NOTES

The RF inputs are biased internally and are normally coupled to the signal source with suitable capaitors.

The output stage has a novel design and is intended to drive a CMOS synthesiser input. External pull-down resistors or circuits are not required. The SP8715 is not suitable for driving TTL or similar devices.

The device will operate down to DC frequencies for non-sinusoidal signals provided that the input slew rate is better than 100V/µs.

POWER DOWN (pin 7) is connected internally to a pull-down resistor. If the battery economy facility is not used, pin 7 should be either left unconnected or connected to V_{EE}.

Ratio Select (Pin 3)	Modulus Control (Pin 6)	Division Ratio
L	L	129
L	H	128
H	L	65
H	H	64

Table 1 Truth table

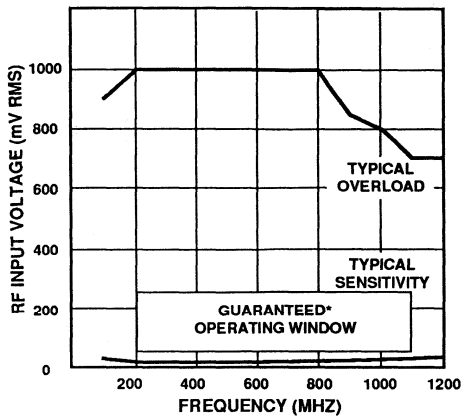


Fig. 3 Typical input characteristics

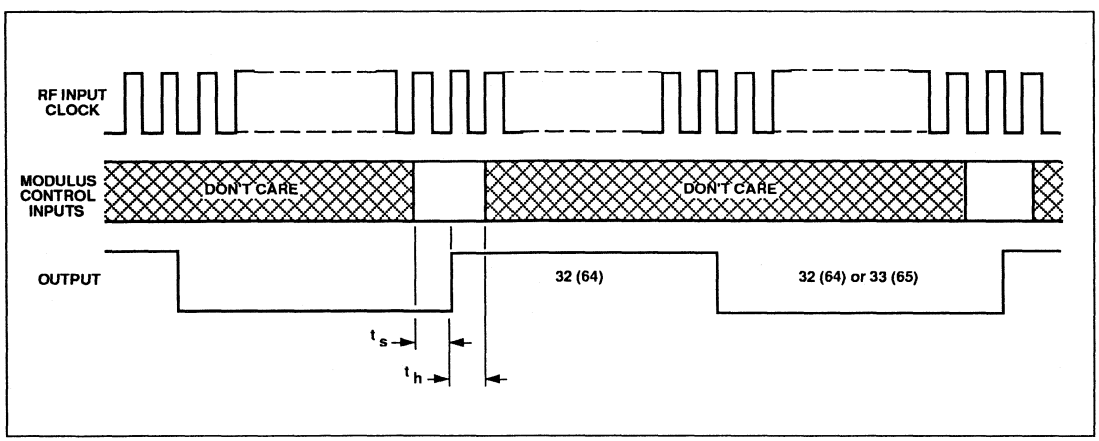


Fig. 4 Modulus control timing diagram

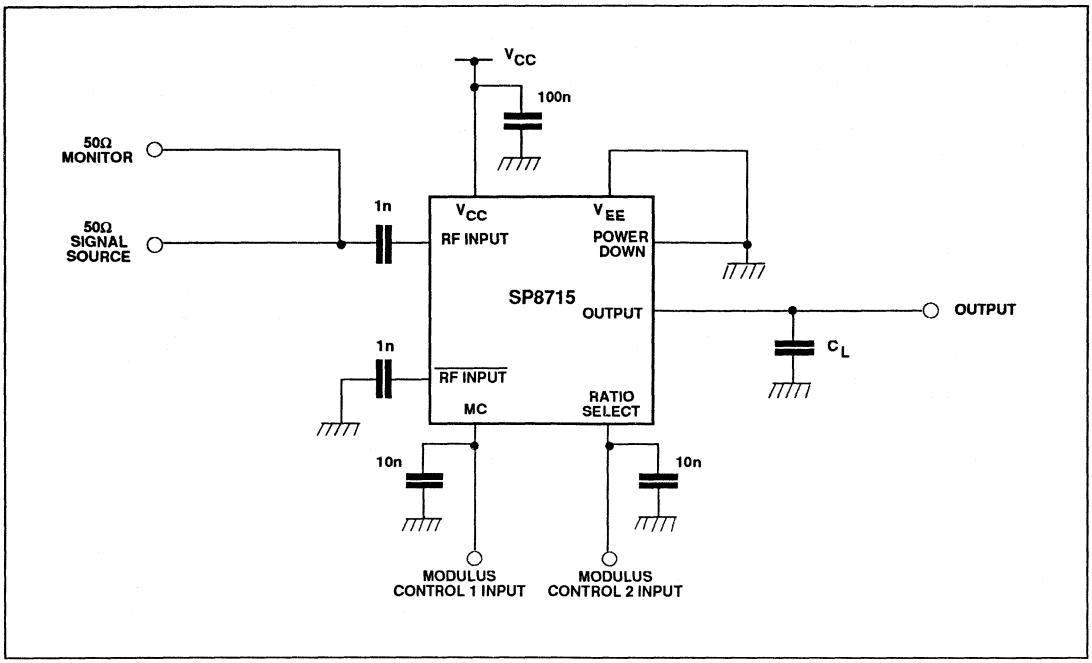


Fig. 5 Toggle frequency test circuit

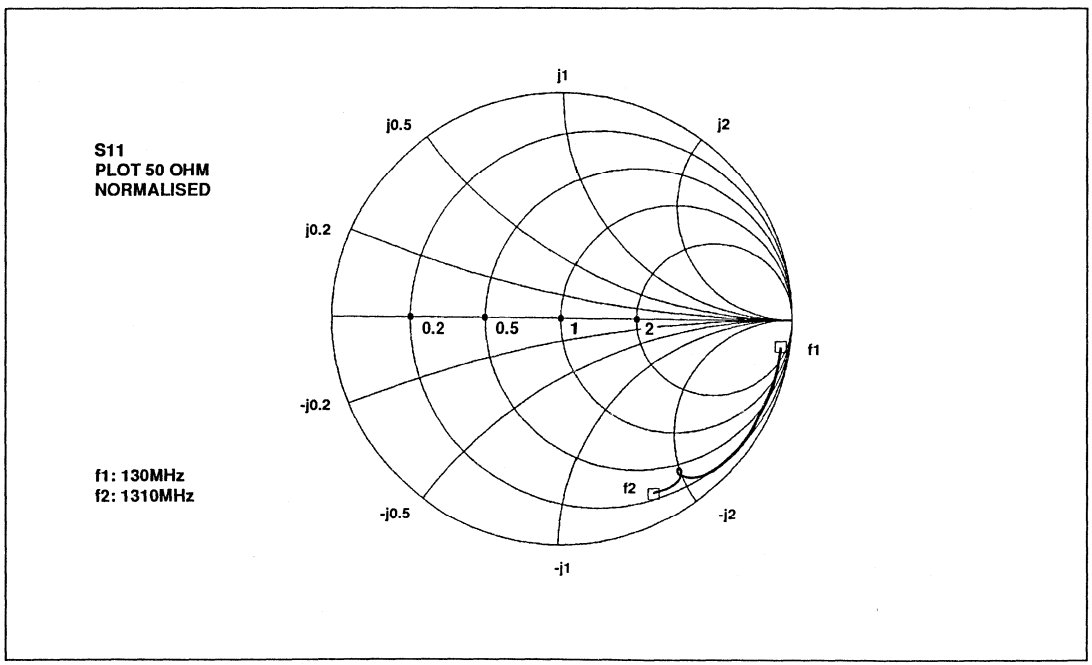


Fig. 6 Typical S11 parameter for pin 1. V_{CC} = +5.0V

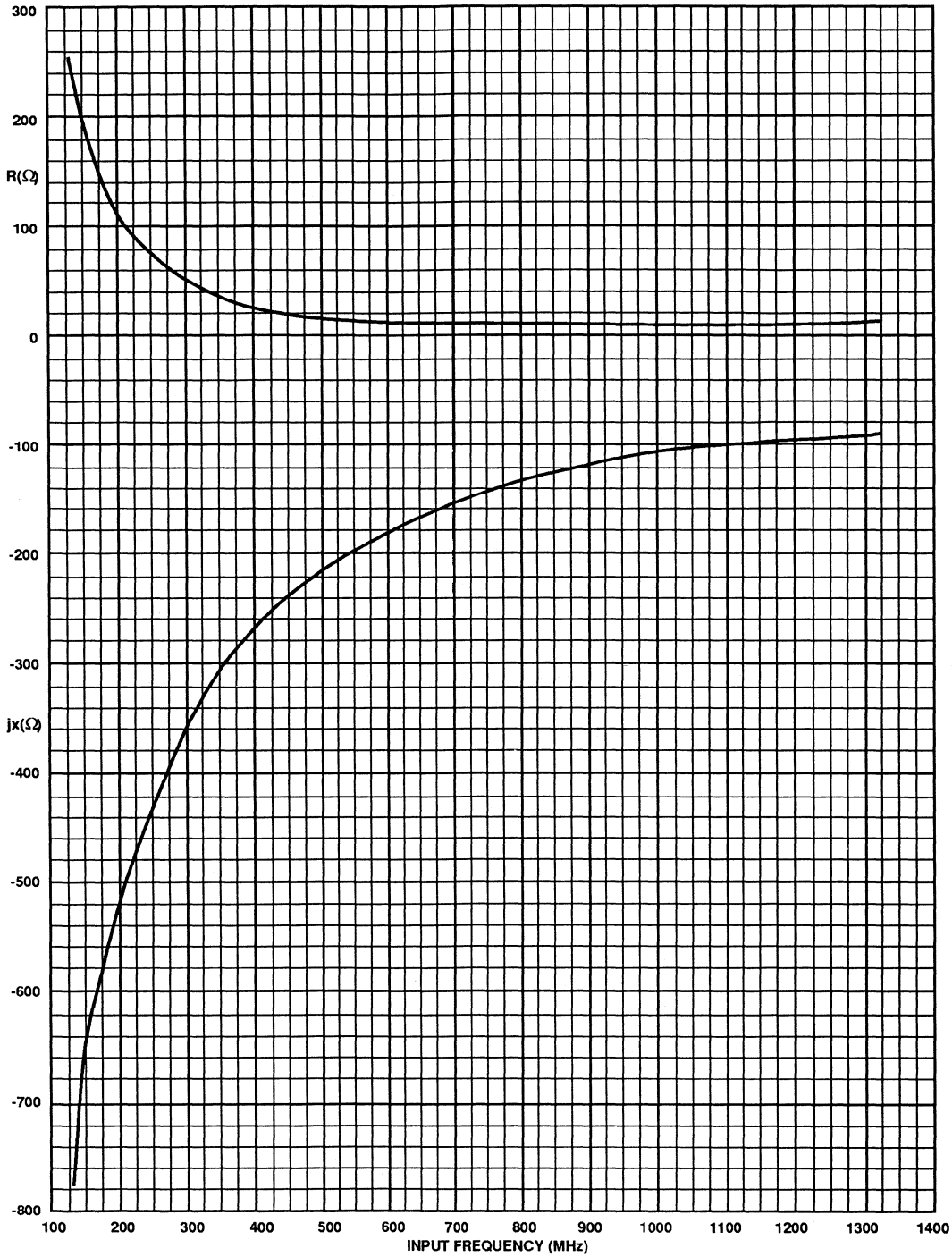


Fig. 7 Typical input impedance v. frequency

FREQ-MHZ	R (Ω)	jx (Ω)
130.000	255.068	-733.538
153.600	153.362	-688.623
177.200	153.330	-583.339
200.800	115.187	-545.839
224.400	88.649	-482.377
248.000	80.815	-441.798
271.600	71.050	-411.502
295.200	56.207	-369.645
318.800	39.526	-346.620
342.400	41.338	-323.129
366.000	38.779	-304.804
389.600	39.210	-280.556
413.200	23.809	-269.674
436.800	21.221	-255.279
460.400	27.545	-245.161
484.000	23.333	-234.680
507.600	22.227	-224.572
531.200	19.931	-211.375
554.800	17.767	-203.241
578.400	17.636	-194.613
602.000	14.607	-186.545
625.600	12.479	-182.049
649.200	13.075	-174.839
672.800	12.891	-168.320
696.400	12.583	-160.468
720.000	11.250	-156.267
743.600	10.213	-149.642
767.200	10.187	-145.328
790.800	11.269	-143.144
814.400	11.081	-137.557
838.000	10.509	-132.750
861.600	10.063	-129.254
885.200	10.172	-124.495
908.800	10.745	-120.568
932.400	10.841	-118.100
956.000	10.884	-113.395
979.600	12.260	-109.552
1003.20	12.984	-105.975
1026.80	14.508	-103.110
1050.40	16.625	-99.886
1074.00	19.260	-98.149
1097.60	22.799	-98.605
1121.20	23.285	-99.907
1144.80	21.149	-100.925
1168.40	18.956	-99.639
1192.00	16.434	-98.425
1215.60	14.377	-95.033
1239.20	13.743	-92.553
1262.80	12.711	-89.249
1286.40	12.776	-86.081
1310.00	12.598	-82.581

Table.2 Coefficients for Fig.7

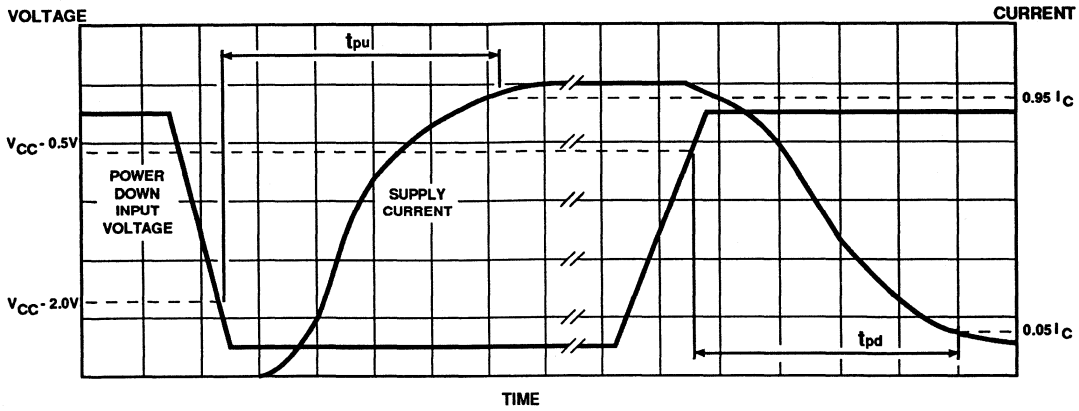


Fig. 8 Power up and power down

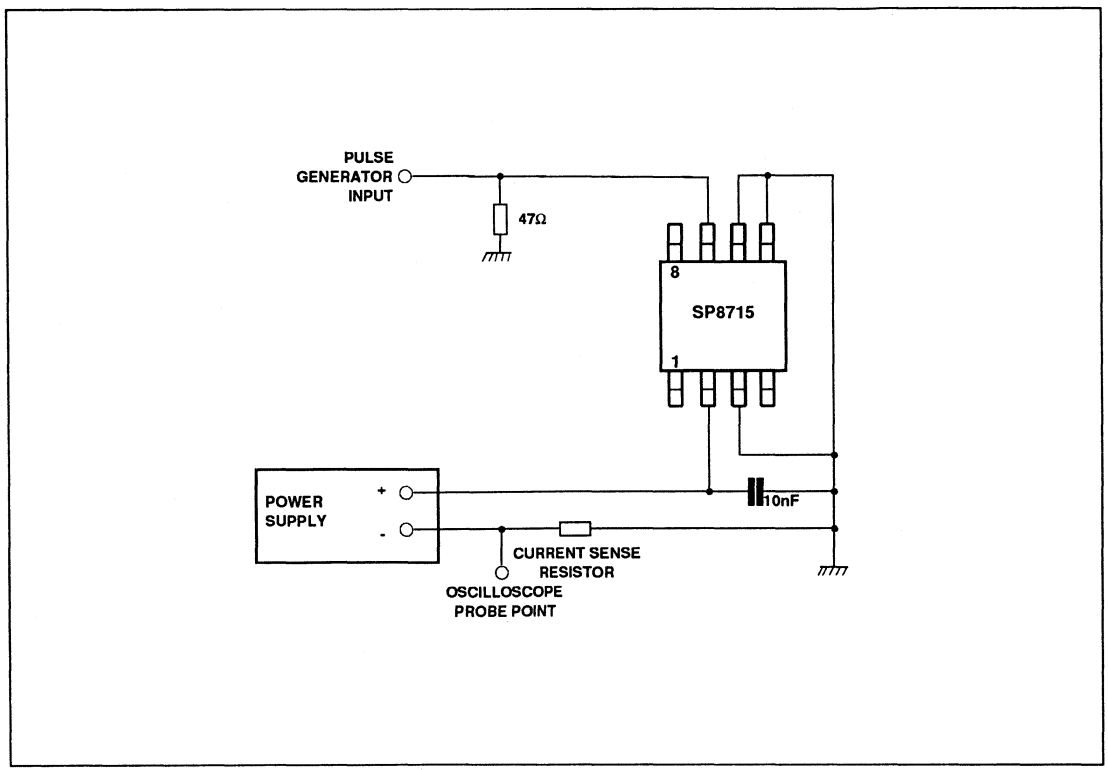


Fig. 9 Power-down time test circuit

Section 3

Paging Receivers & Decoders

GEC PLESSEY
SEMICONDUCTORS

SL6609A

DIRECT CONVERSION FSK DATA RECEIVER

This device is an advanced direct conversion receiver for operation up to 470MHz. The design is based on the SL6609 receiver and is a pin for pin product upgrade. The device integrates all functions to translate a binary FSK modulated RF signal into a demodulated data stream. Adjacent channel rejection is provided using tuneable gyrator filters. To assist operation in the presence of large interfering signals both RF and audio AGC functions are provided.

The device also includes a 1 volt regulator capable of sourcing up to 5mA, a battery flag and the facility of incorporating a more complex post detection filter off-chip. Both battery flag and data outputs have open collector outputs to ease their interface with other devices.

FEATURES

- Very low power operation - typ 3.0mW
- Single cell operation for most of the device. Limited functional blocks operating via an inverter
- Superior sensitivity of -130dBm
- Operation at wide range of paging data rates 512, 1200, 2400 baud
- On chip 1 volt regulator
- Small package offering SSOP

APPLICATIONS

- Credit card pagers
- Watch pagers
- Small form factor pagers i.e. PCMCIA
- Low data rate data receivers i.e. Security/remote control

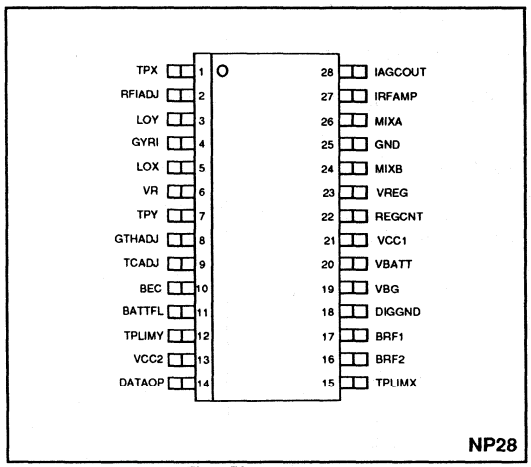


Fig.1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6V
Storage temperature	-55°C to +150°C
Operating temperature	-20°C to +70°C

ORDERING INFORMATION

SL6609A / KG / NPDS - SSOP devices in anti-static sticks
SL6609A / KG / NPDE - SSOP devices in tape and reel

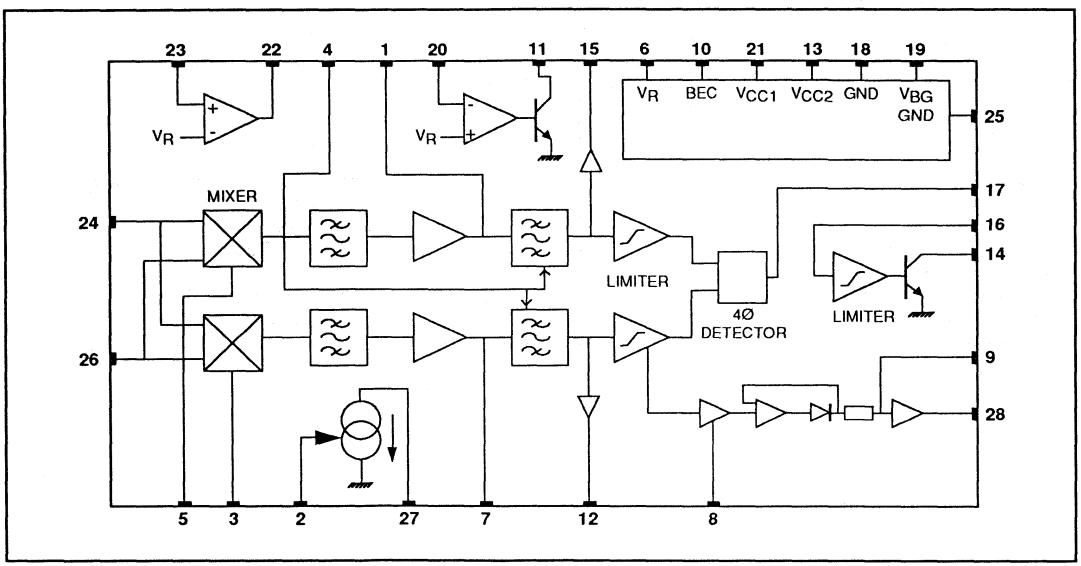


Fig.2 Block diagram of SL6609A

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
Tamb = 25°C, VCC1 = 1.3V, VCC2 = 2.7V

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
VCC1 - Supply voltage	21	0.95	1.3	2.8	V	VCC1 ≤ VCC2 - 0.7 volts
VCC2 - Supply voltage	13	1.8	2.7	3.5	V	
ICC1 - Supply current	21,27,28		1.5	1.8	mA	Includes IRF. Does not include regulator supply. Audio AGC inactive
ICC2 - Supply current	11,13,14		550	700	µA	Batt flag & Data O/P high Pin 27 voltage: 0.3 - 1.3V
Power down ICC1	21,27,28			1	µA	
Power down ICC2	11,13,14			8	µA	
1 volt regulator	23	0.95	1.0	1.05	V	I Load = 3mA. Ext PNP. ß >= 100, V_{CE} = 0.1 volt
Band gap voltage reference	19	1.15	1.21	1.27	V	
Band gap current source	19			20	µA	
Voltage reference	6	0.93	1.0	1.07	V	
Voltage reference sink/source	6			10	µA	VCC1 > 1.1V
1 volt regulator load current		0.25	3	5	mA	
Turn on Time			5		ms	Stable data o/p when 3dB above sensitivity. C_{BG} and C_{VR} = 2.2µF
Turn off Time			1		ms	Fall to 10% of steady state current C_{BG} and C_{VR} = 2.2µF
Detector output current	17		+/-4		µA	
RF current source						
Current Source (IRF)	27	400	500	600	µA	Pin 27 voltage: 0.3 - 1.3V
Decoder						
Sensitivity		40			µVrms	Signal injected at TPX and TPY B.E.R. ≤ 1 in 30 5KHz deviation @ 1200 bits/sec BRF capacitor = 1nF
Output mark space ratio	14	7:9		9:7		
Data O/P Sink Current	14	100		500	µA	Output logic low
Data O/P Leakage Current	14			1.0	µA	Output logic high

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
Tamb = 25°C, VCC1 = 1.3V, VCC2 = 2.7V

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
Battery Economy						
Input logic high	10	(V_{CC2} - 0.3)			V	Powered Up
Input logic low	10			0.3	V	Powered Down
Input current	10		0.05	1	µA	Powered Up
Input current	10		6	8	µA	Powered down transient initial
Battery Flag Input						
Input current	20			1		µA
Battery Flag Output						
Battfl Sink Current	11	50		500	µA	(VBATT-VR) > 20mV
Battfl leakage current	11			1	µA	(VBATT-VR) < -20mV
Mixers						
Gain to "IF Test"		34		41	dB	LO inputs driven in parallel with 50mVRMS @ 50MHz.IF = 2kHz
RF input impedance	24, 26					See Figs.8a, 8b
LO input impedance	3, 5					See Fig.9
LO DC bias voltage	3, 5				V	Equal to Pin 21 (VCC1)
Audio AGC						
Max Audio AGC Sink Current	28	45	65	85	µA	

RECEIVER CHARACTERISTICS (GPS Demonstration board)

Measurement conditions unless stated V_{CC1} = 1.3V, V_{CC2} = 2.7V, LNA = 18dB Power Gain, 2dB Noise figure,
Carrier frequency 153MHz, BER 1 in 30, Tamb = 25°C
(TPx/TPy typically:- 160mV_{pp} ±10% for - 73dBm RF input to the LNA)

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
Sensitivity		-130	-128	-125	dBm	1200 bps Δf = 4kHz LO = -18dBm
Intermodulation		52	56		dB	1200 bps Δf = 4kHz LO = -18dBm
Adjacent channel		68	73		dB	1200 bps Δf = 4kHz LO = -18dBm Channel spacing 25kHz
Centre frequency acceptance			+/-2.3		kHz	1200 bps Δf = 4kHz LO = -18dBm
Deviation acceptance			+/-2.2		kHz	1200 bps Δf = 4kHz LO = -18dBm

RECEIVER CHARACTERISTICS (GPS Demonstration board)

Measurement conditions unless stated V_{CC1} = 1.3V, V_{CC2} = 2.7V, LNA = 20dB Power Gain, 2dB Noise figure,
Carrier frequency 282MHz, BER 1 in 30, Tamb = 25°C
(TPx/TPy typically:- 160mV$_{pp}$ ±10% for - 73dBm RF input to the LNA)

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
Sensitivity		-130	-128 -125.5	-125 -122	dBm dBm	1200 bps Δf = 4kHz 2400 bps Δf = 4.5kHz LO = -15dBm
Intermodulation (IP3)		52 49	56 53.5		dB	1200 bps Δf = 4kHz 2400 bps Δf = 4.5kHz LO = -15dBm
Intermodulation (IP2)		47	52		dB	1200 bps Δf = 4kHz LO = -15dBm
Adjacent channel		67 64	72.5 69.5		dB	1200 bps Δf = 4kHz 2400 bps Δf = 4.5kHz LO = -15dBm Channel spacing 25kHz
Centre frequency acceptance		+/-1.9	+/-2.3 +/-2		kHz	1200 bps Δf = 4kHz 2400 bps Δf = 4.5kHz LO = -15dBm
Deviation acceptance			+/-2.2 +/-2		kHz	1200 bps Δf = 4kHz 2400 bps Δf = 4.5kHz LO = -15dBm

RECEIVER CHARACTERISTICS

Measurement conditions unless stated V_{CC1} = 1.3V, V_{CC2} = 2.7V, LNA = 22dB Power Gain, 2dB Noise figure,
Carrier frequency 470MHz, BER 1 in 30, Tamb = 25°C
(TPx/TPy typically:- 140mV$_{pp}$ ±10% for - 73dBm RF input to the LNA)

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
Sensitivity		-128	-126	-123	dBm	1200 bps Δf = 4kHz LO = -15dBm
Intermodulation		50	55.5		dB	1200 bps Δf = 4kHz LO = -15dBm
Adjacent channel		67	72.5		dB	1200 bps Δf = 4kHz LO = -15dBm Channel spacing 25kHz
Centre frequency acceptance			+/- 2.3		kHz	1200 bps Δf = 4kHz LO = -15dBm
Deviation acceptance			+/- 2.2		kHz	1200 bps Δf = 4kHz LO = -15dBm

OPERATION OF SL6609A

The SL6609A is a Direct Converson Receiver designed for use up to 470MHz. It is available in a 28 pin SSOP package and it integrates all the facilities required for the conversion of an RF FSK signal to a base-band data signal.

Low Noise Amplifier

To achieve optimum performance it is necessary to incorporate a Low Noise RF Amplifier at the front end of the receiver. This is easily biased using the on chip voltage and current sources provided.

All voltages and current sources used for bias of the RF amplifier, receiver and mixers should be RF decoupled using suitable capacitors (see Fig.4 for a suitable Low-Noise-Amplifier).

Local Oscillator

The Local Oscillator signal is applied to the device in phase quadrature. This can be achieved with the use of two RC networks operating at the -3dB/45° transfer characteristic, giving a full 90° phase differential between the LO ports of the device. Each LO port of the device also requires an equal level of drive from the Oscillator. (see Fig.5).

Gyrator Filters

The on chip filters include an adjustable gyrator filter. This may be adjusted with the use of an additional resistor between Pin 4 and GND. This allows flexibility of filter characterstics and also allows for compensation for possible process variations.

Audio AGC

The Audio AGC fundamentally consists of a current sink which is controlled by the audio (baseband data) signal. It has three parameters that may be controlled by the user. These are the Attack (turn on) time, Decay (duration) time and Threshold level (see Figs.6 and 7). See Application note for details.

Regulator

The on chip regulator must be used in conjunction with a suitable PNP transistor to achieve regulation. As the transistor forms part of the regulator feedback loop the transistor should exhibit the following characteristics:-

$H_{FE} >= 100$ for $V_{CE} >= 0.1V$

Pin Number	Pin Name	Pin Description
1	TPX	X channel pre-gyrator filter test-point. This can be used for input and output
2	RFIADJ	RF current source adjustment pin
3	LOY	LO input channel Y
4	GYRI	Gyrator current adjust pin
5	LOX	LO input channel X
6	VR	VREF 1.0 V internal signal ground
7	TPY	Y channel pre-gyrator filter test point, input or output
8	GTHADJ	Audio AGC gain and threshold adjust. RSSI signal indicator
9	TCADJ	Audio AGC time constant adjust
10	BEC	Battery economy control
11	BATTFL	Battery flag output
12	TPLIMY	Y channel limiter (post gyrator filter) test point, output only
13	VCC2	Supply connection
14	DATAOP	Data output pin
15	TPLIMX	X channel limiter (post gyrator filter) test point, output only
16	BRF2	Bit rate filter 2, input to data output stage
17	BRF1	Bit rate filter 1, output from detector
18	DIG GND	Digital ground
19	VBG	Bandgap voltage output
20	VBATT	Battery flag input voltage
21	VCC1	Supply connection
22	REGCNT	1V regulator control external PNP drive
23	VREG	1V regulator output voltage
24	MIXB	Mixer input B
25	GND	Ground
26	MIXA	Mixer input A
27	IRFAMP	Current source for external LNA. Value of current output will decrease at high mixer input signal levels due to RF AGC
28	IAGCOUT	Audio AGC output current

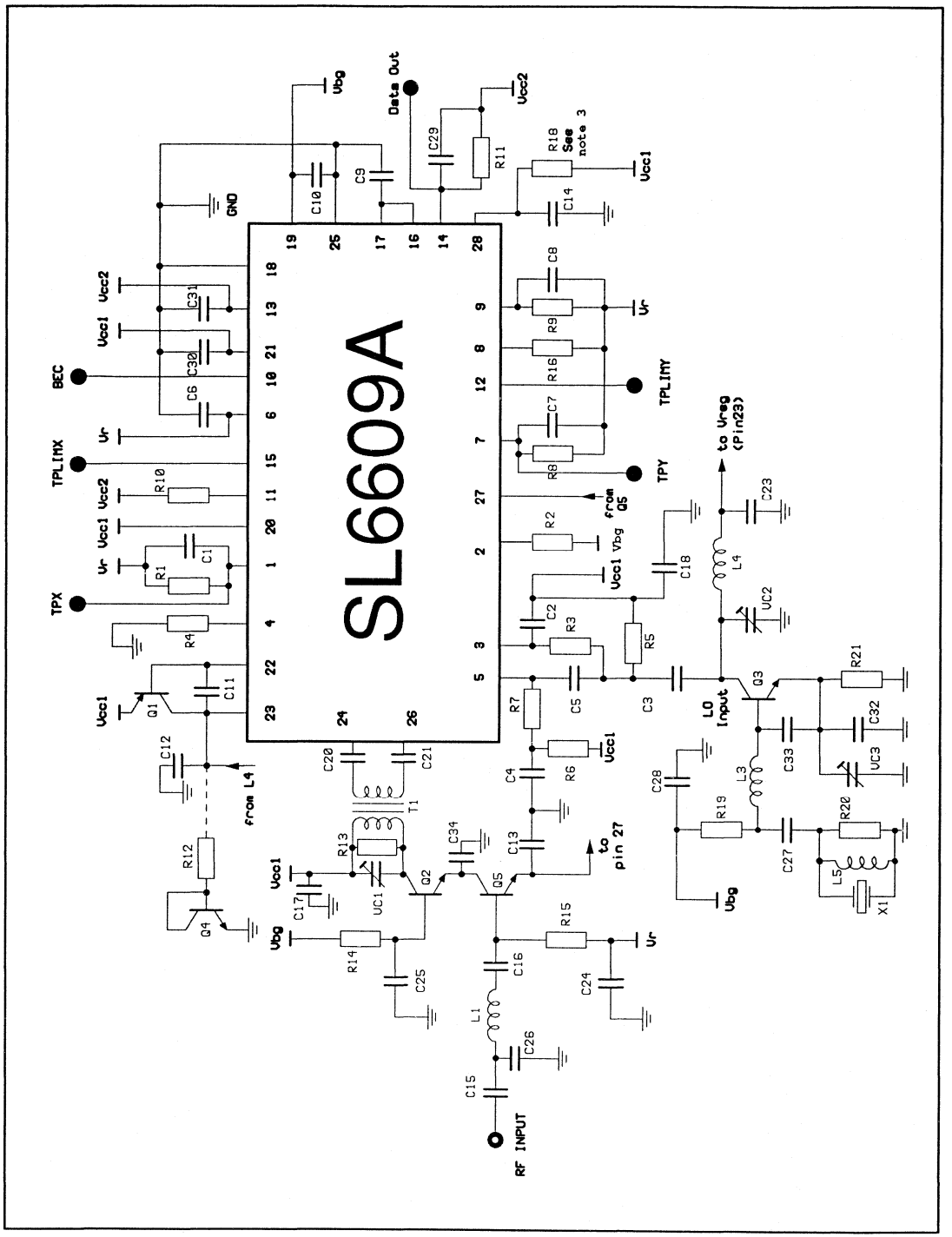


Fig.3 Application circuit board

COMPONENTS LIST FOR APPLICATION BOARD At 282MHz, 25kHz Channel Spacing.

(LO Circuit in Fig.3)

Resistors

R1	open circuit
R2	open circuit
R3	100
R4	100k
R5	1k
R6	1k
R7	100
R8	open circuit
R9	220k
R10	1M
R11	100k (6)
R12	not used
R13	1k5(1)
R14	4k7
R15	4k7
R16	33k
R17	not used
R18	0R (3)
R19	10k
R20	620
R21	1k
R22	open circuit

Capacitors

C1	1n
C2	2p7
C3	4p7
C4	1n
C5	2p7
C6	2u2
C7	1n
C8	100n
C9	1n (2)
C10	2u2
C11	100n
C12	1n
C13	1n
C14	1n
C15	1n
C16	1n
C17	1n
C17a	1n
C18	1n
C19	not used
C20	1n
C21	1n
C22	not used
C23	1n
C24	1n
C25	1n
C26	6p8
C27	1n
C28	1n
C29	100p
C30	2u2
C31	2u2
C32	4p7
C33	4p7
C34	3p3
C35	not used
VC1	1-10p
VC2	1-10p
VC3	1-10p

Inductors

L1	68n (4)
L2	not used (3)
L3	470n
L4	39n
L5	680n

Active Components

Q1	FMMT589
Q2	2SC5065 (Toshiba)
Q3	BFT25A (Philips)
Q4	not used
Q5	2SC5065 (Toshiba)
D1	Panasonic MA862 (5)

Misc

T1	30nH 1:1 Coilcraft M1686-A
Xtal	5th Overtone 94.075MHz

Notes

1. The values of R13 is determined by the set-up procedure. See Application Note.

2. The value of C9 is determined by the output data rate. Use 2nF for 512bps, 1nF for 1200bps and 470pF for 2400bps.

3. L2 is used in the Audio AGC circuit (see Fig. 6). For the characteristics of the Audio AGC current source see Fig.7. If the audio AGC is not required then the current source (Pin 28) may be disabled by connecting Pin 9 (TCADJ) to VR (Pin 6) and by connecting Pin 28 (IAGCOUT) to Vcc1, (R18). The voltage at Pin 8 may still be used as an RSSI. R9, C8, C14, C19, R17 and D1 may then be omitted. See Fig.6 for AGC component values.

4. L1 and C26 form the low noise matching network for the RF amplifier. The values given are for the RF amplifier specified in the Applications Circuit with no Audio AGC connected. i.e. R17 and D1 omitted.

5. Suggested diode for use with the Audio AGC circuit (see Fig.6) (D1 is not included on the general demonstration circuit).

6. The value of R11 is dependent on the data output load. R11 should allow sufficient current to drive the data output load.

COMPONENTS LIST FOR APPLICATION BOARD

At 470MHz, 25kHz Channel Spacing.
(LO circuit is 50Ω network as in Fig.5 - crystal oscillator not specified)

Resistors

R1	open circuit
R2	open circuit
R3	100
R4	100k
R5	100
R6	100
R7	100
R8	open circuit
R9	220k
R10	1M
R11	100k (2)
R12	300 (3)
R13	3k9 (1)
R14	4k7
R15	4k7
R16	33k
R17	open circuit (4)
R18	0R (4)
R22	open circuit

Capacitors

C1	1n
C2	3.3pF
C3	1n
C4	1n
C5	3.9pF
C6	2u2
C7	1n
C8	100n
C9	1n (2)
C10	2u2
C11	100n
C12	1n
C13	1n
C14	1n
C15	1n
C16	1n
C17	1n
C18	1n
C19	not used
C20	1n
C21	1n
C22	not used
C23	not used
C24	1n
C25	1n
C26	open circuit
C27	not used
C28	not used
C29	100p
C30	2u2
C31	2u2
C34	1p5
VC1	1-3pF

Inductors

L1	47nH (5)
L2	not used (3)
T1	16nH 2 Turn 1:1 (Coilcraft) Q4123-A

Active Components

Q1	Zetex FMMT589
Q2	Philips BFT25A
Q3	Not Used
Q4	Philips BFT25A(3)
Q5	Philips BFT25A
D1	Panasonic MA862(6)

Notes

1. The values of R13 is determined by the set-up procedure. See Application Note.

2. The value of "C9" is determined by the output data rate. Use 2nF for 512bps, 1nF for 1200bps and 470pF for 2400bps.

3. R12 & Q4 form a dummy load for the regulator. Permitted load currents for the regulator are 250µA to 5mA. The 1V regulator (output Pin 23) can be switched off by connecting Pin 23 directly to VCC2. Q1, Q4, R12 and C12 must then be omitted

4. L2 is used in the Audio AGC circuit (see Fig.6). For the characteristics of the Audio AGC current source see figure 7. If the Audio AGC is not required then the current source (Pin 28) may be disabled by connecting Pin 9 (TCADJ) to VR (Pin 6) and by connecting Pin 28 (IAGCOUT) to Vcc1, (R18). The voltage at Pin 8 may still be used as an RSSI. R9, C8, C14, C19, R17 and D1 may then be omitted.

5. L1 and C26 form the low noise matching network for the RF amplifier. The values given are for the RF amplifier specified in the Applications Circuit with no Audio AGC connected. i.e. R17 and D1 omitted.

6. Suggested diode for use with the Audio AGC circuit (D1 is not included on the general demonstration circuit).

7. The value of R11 is dependent on the data output load. R11 should allow sufficient current to drive the data output load.

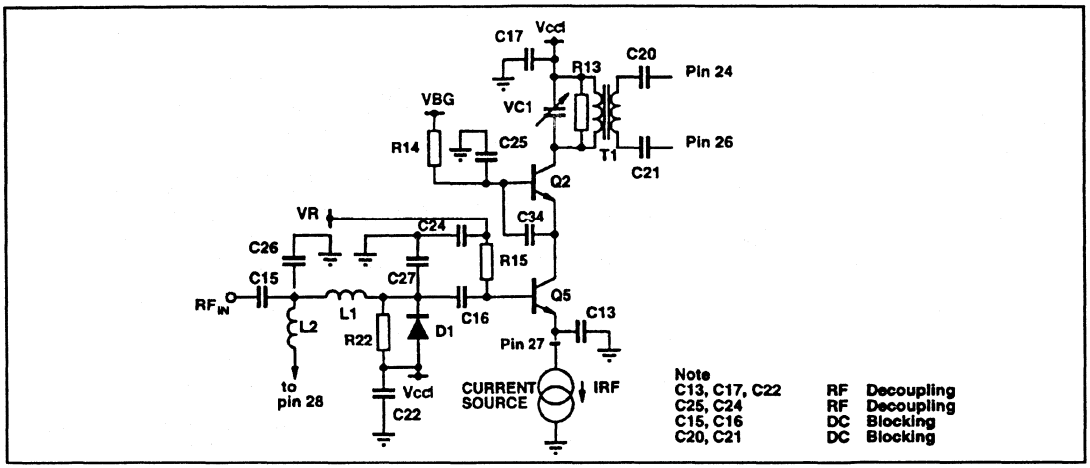


Fig.4 RF amplifier

RF Amplifier Components Values

Resistors		Capacitors		
R14, R15	4k7	C13, C15	1nF	Active components
R13	see note 1	C16, C17	1nF	D1 MA862 (Panasonic)
R22	47k	C20, C21	1nF see note 2	
		C24, C25	1nF	
		L2	820nH	

Notes:

(1) The value of R13 is determined by the set up procedure (See "Set up for optimum performance").

(2) C20 and C21 are purely for deomonstration purposes. Pin 24 and Pin 26 may be DC coupled provided that no DC voltage is applied to the mixer inputs.

Frequency Dependent Components

	153MHz	280MHz	450MHz
C26	not used	6.8p	not used
C27	not used	not used	not used
L1	150nH	68nH	39nH
C34	3p3	2p2	1p5
T1	100nH	30nH	16nH
	Coilcraft N2261-A	Coilcraft M1686-A	Coilcraft Q4123-A
VC1	1-10pF	1-10pF	1-3pF
Q4, Q5	Toshiba 2SC5065	Toshiba 2SC5065	Philips BFT25A

(See also Lo drive Network)

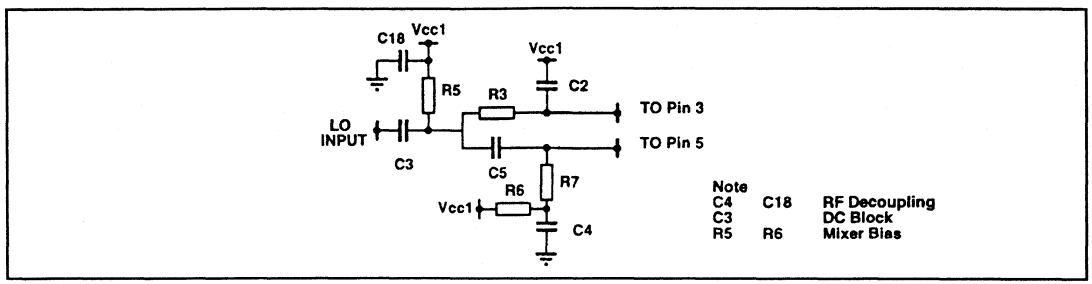


Fig.5 Local oscillator drive network

LO Drive Network Component Values

50Ohm input impedance (External LO injection)

	153MHz	280MHz	450MHz
C2	10p	5p6	3p3
C5	10p	5p6	3p9

C3, C4, C18 = 1n

R3, R5, R6, R7 = 100Ohms

Higher Input Impedance (crystal oscillator input)

	153MHz	280MHz	450MHz
C3	Set by load allowable on crystal oscillator (typical 4p7)		
C2	10p	5p6	3p3
C5	10p	5p6	3p9
R3	100	100	100
R7	100	100	100

R5, R6 = 1k

C4, C18 = 1n

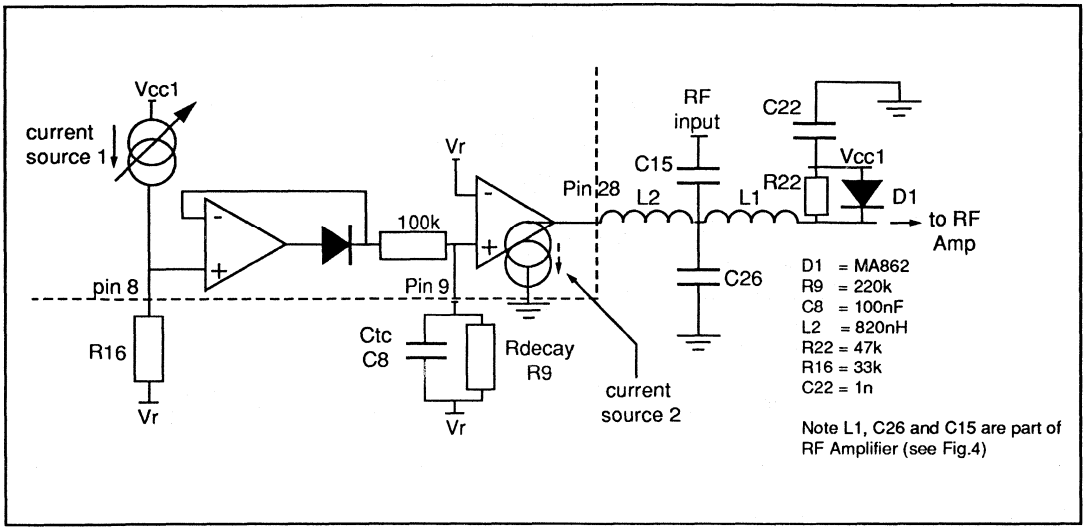


Fig.6 AGC Schematic

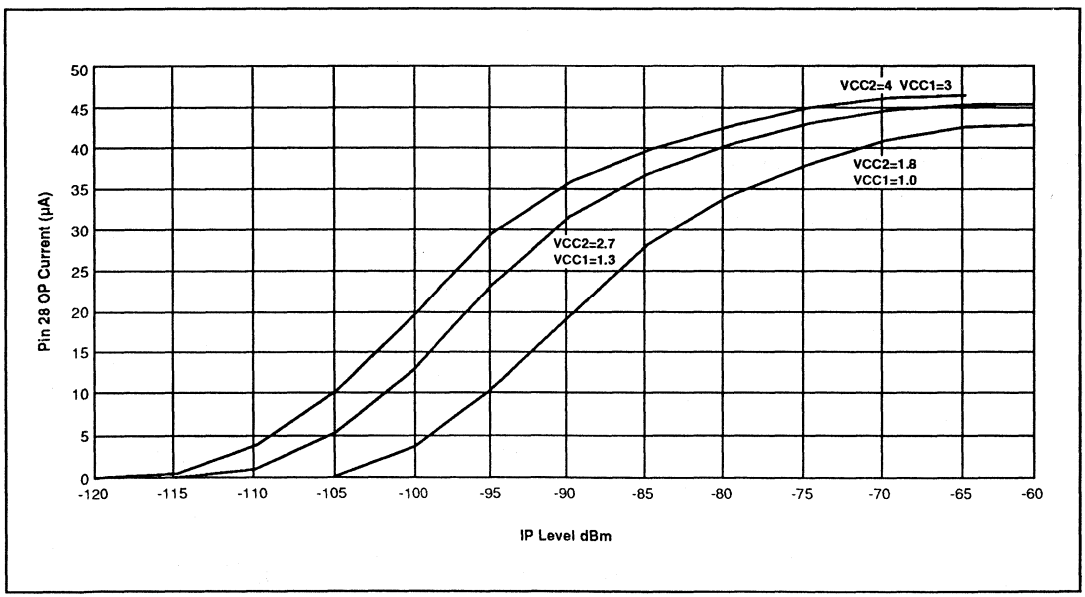


Fig.7 Audio AGC current vs. IP power at 25°C

S11

FREQ	MAG	ANG
50.000	0.969	-7.20
100.000	0.958	-14.45
150.000	0.942	-20.59
200.000	0.917	-26.40
250.000	0.893	-33.26
300.000	0.858	-39.84
350.000	0.832	-44.78
400.000	0.806	-49.01
450.000	0.781	-54.00
500.000	0.755	-59.53
550.000	0.743	-64-35
600.000	0.725	-68.43
650.000	0.703	-73.01
700.000	0.680	-78.74
750.000	0.666	-83.76
800.000	0.653	-87.48
850.000	0.636	-91.32
900.000	0.615	-97.17
950.000	0.604	-102.84
1000.00	0.600	-105.23

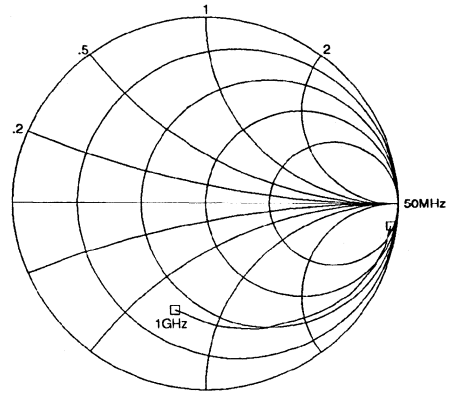


Fig.8a SL6609A Mixer A input S-Parameters

S11

FREQ	MAG	ANG
50.000	0.970	-7.06
100.000	0.960	-13.83
150.000	0.945	-19.90
200.000	0.919	-25.70
250.000	0.902	-32.18
300.000	0.872	-38.03
350.000	0.850	-43.07
400.000	0.825	-48.27
450.000	0.803	-53.58
500.000	0.776	-58.49
550.000	0.760	-63.08
600.000	0.739	-67.98
650.000	0.717	-72.63
700.000	0.698	-76.96
750.000	0.683	-81.09
800.000	0.666	-85.49
850.000	0.659	-89.51
900.000	0.647	-93.90
950.000	0.637	-98.42
1000.00	0.634	-102.40

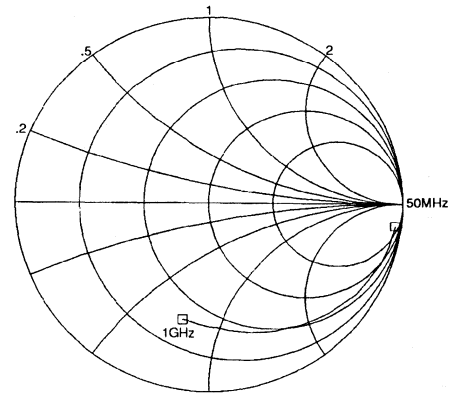


Fig.8b SL6609A Mixer B input S-Parameters

S11

FREQ	MAG	ANG
50.000	0.993	-4.17
100.000	0.995	-8.43
150.000	0.997	-12.88
200.000	0.997	-17.57
250.000	0.996	-22.63
300.000	0.986	-28.16
350.000	0.965	-33.87
400.000	0.936	-39.17
450.000	0.902	-43.88
500.000	0.872	-48.54
550.000	0.838	-52.81
600.000	0.804	-56.60
650.000	0.798	-59.47
700.000	0.810	-65.19
750.000	0.784	-71.49
800.000	0.779	-75.97
850.000	0.790	-82.54
900.000	0.788	-91.16
950.000	0.768	-100.20
1000.00	0.743	-108.52

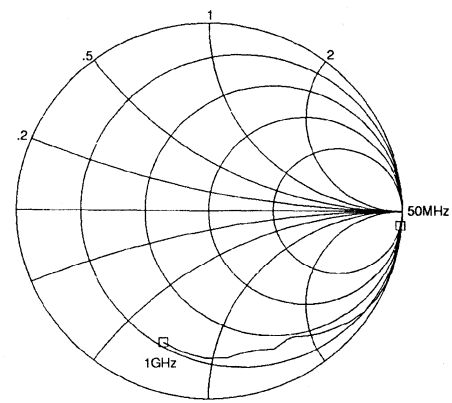


Fig.9 SL6609A LO X,Y inputs S-Parameters

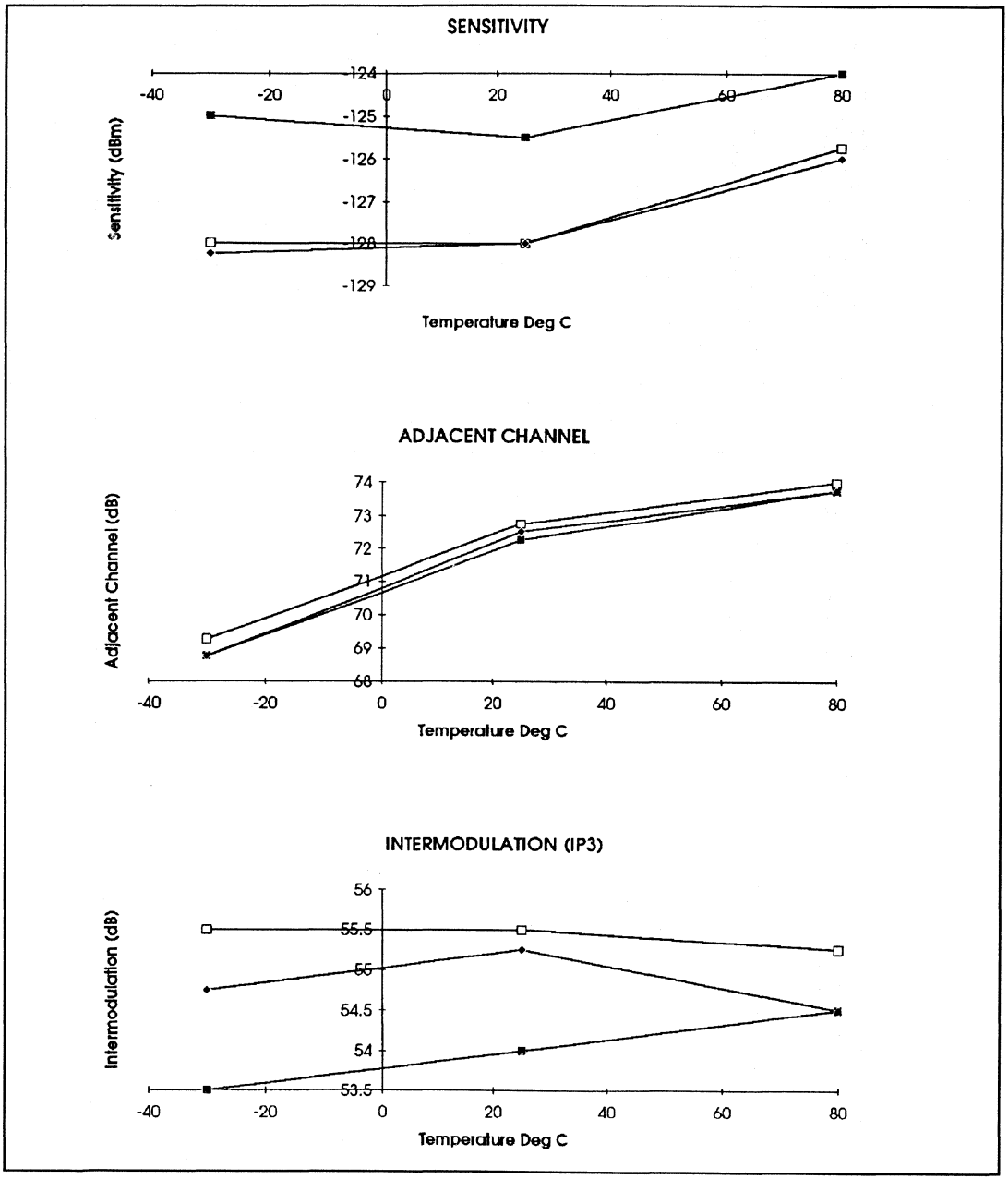


Fig.10a AC parameters vs. supply and temperature

Conditions:- 282MHz GPS demonstration board i.e. 20dB LNA, 2dB noise figure, carrier frequency 282MHz, 1200bps baud rate, 4kHz deviation frequency, BER 1 in 30.

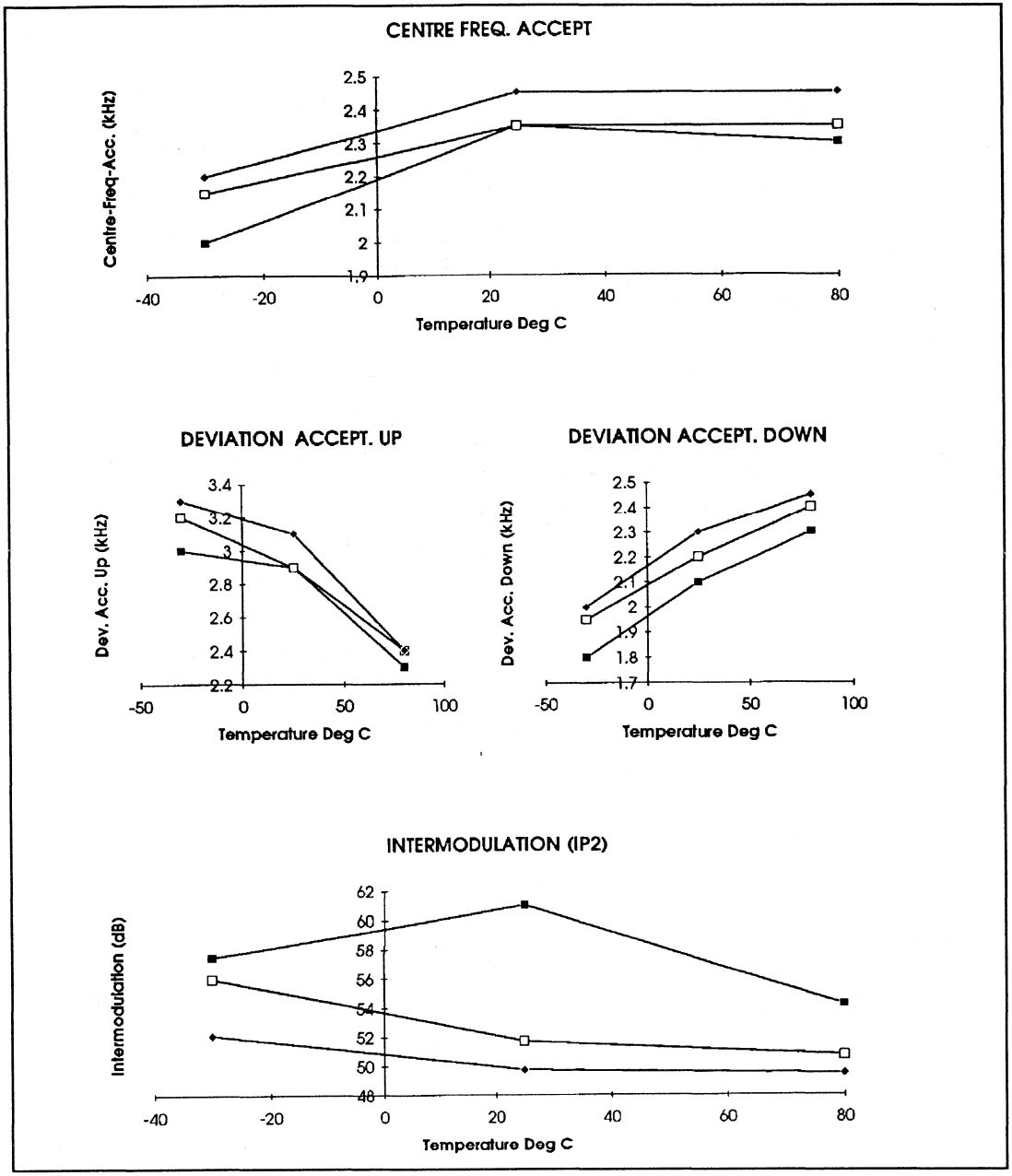
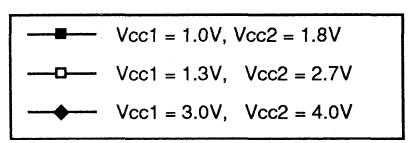


Fig.10b AC parameters vs. supply and temperature

Conditions:- 282MHz GPS demonstration board i.e. 20dB LNA, 2dB noise figure, carrier frequency 282MHz, 1200bps baud rate, 4kHz deviation frequency, BER 1 in 30.



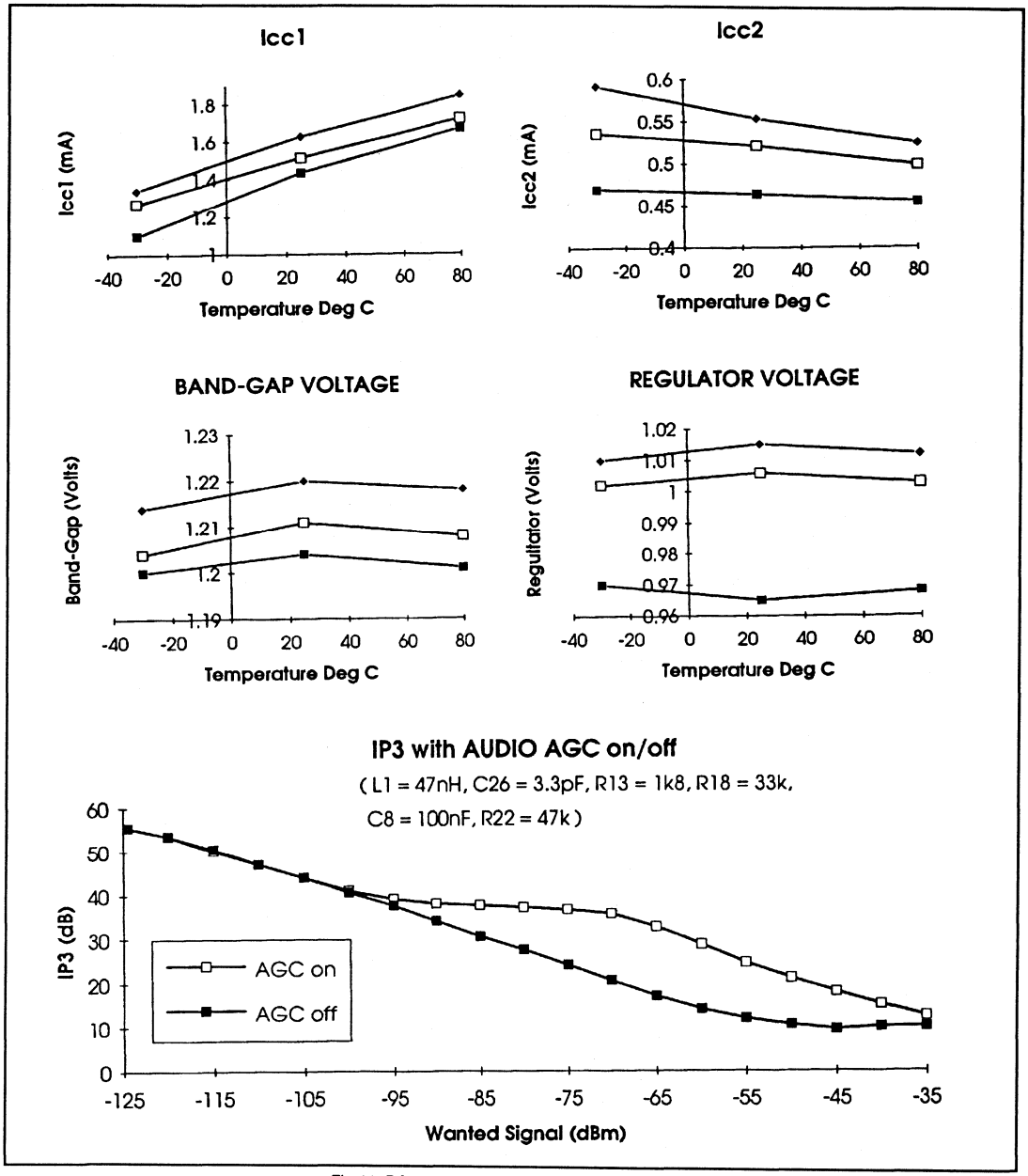


Fig.11 DC parameters vs. supply and temperature (IP3 vs audio AGC both on and off)

Conditions:- ICC1 includes 500µA LNA current but does not include the regulator supply (audio AGC inactive). ICC2 measured with BATT FLAG and DATA O/P HIGH, Fc = 282MHz.

Note 1- IP3 is level above wanted needed to reduce receiver to 1 in 30 B.E.R.

Vcc1 = 0.98V, Vcc2 = 1.78V
Vcc1 = 1.3V, Vcc2 = 2.7V
Vcc1 = 3.0V, Vcc2 = 4.0V

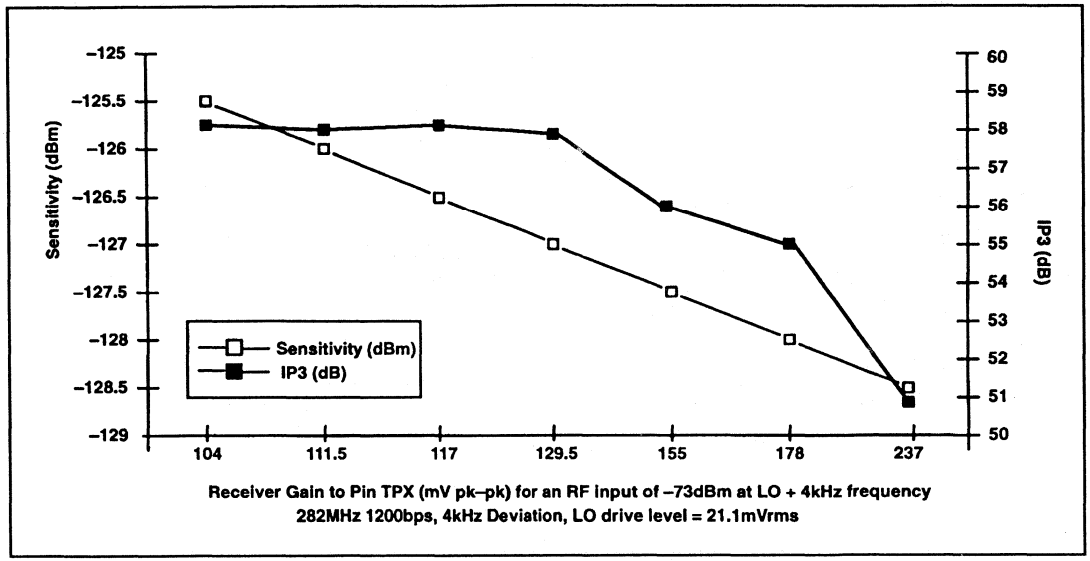


Fig.12 Sensitivity, IP3 vs Receiver Gain

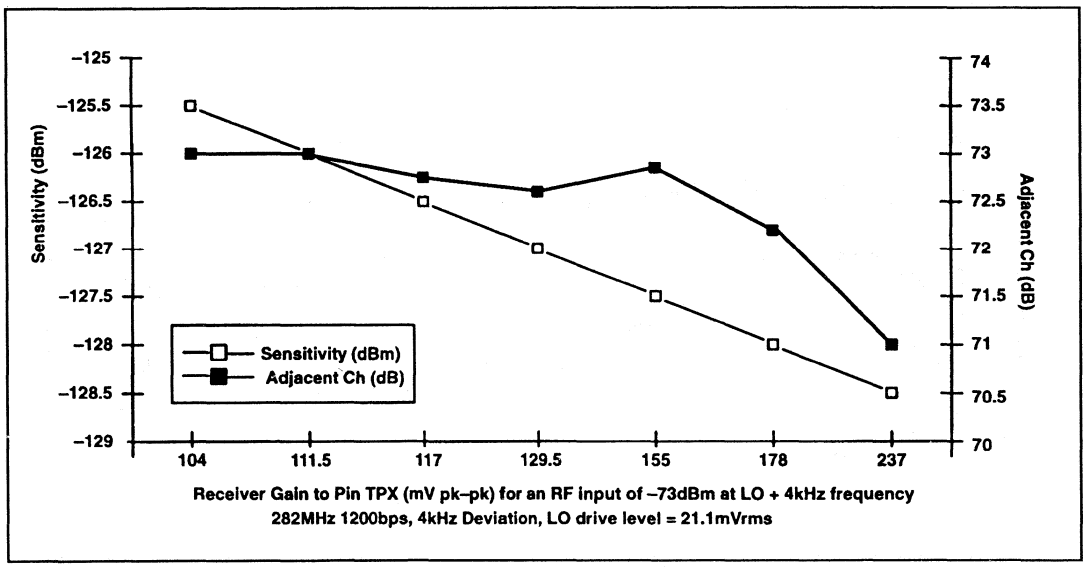


Fig.13 Sensitivity, adjacent Channel vs Receiver Gain

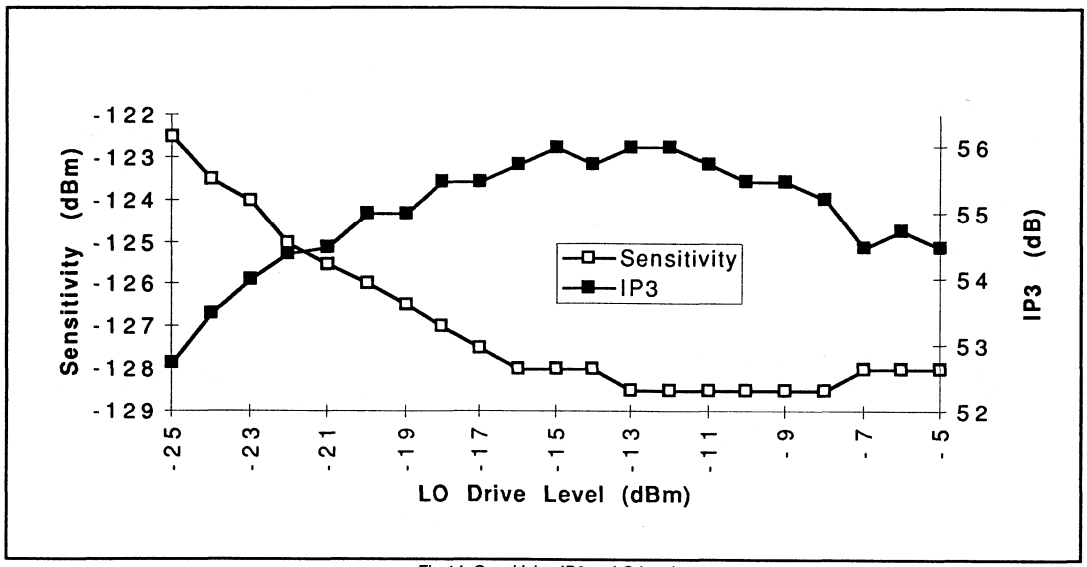


Fig.14 Sensitivity, IP3 vs LO level

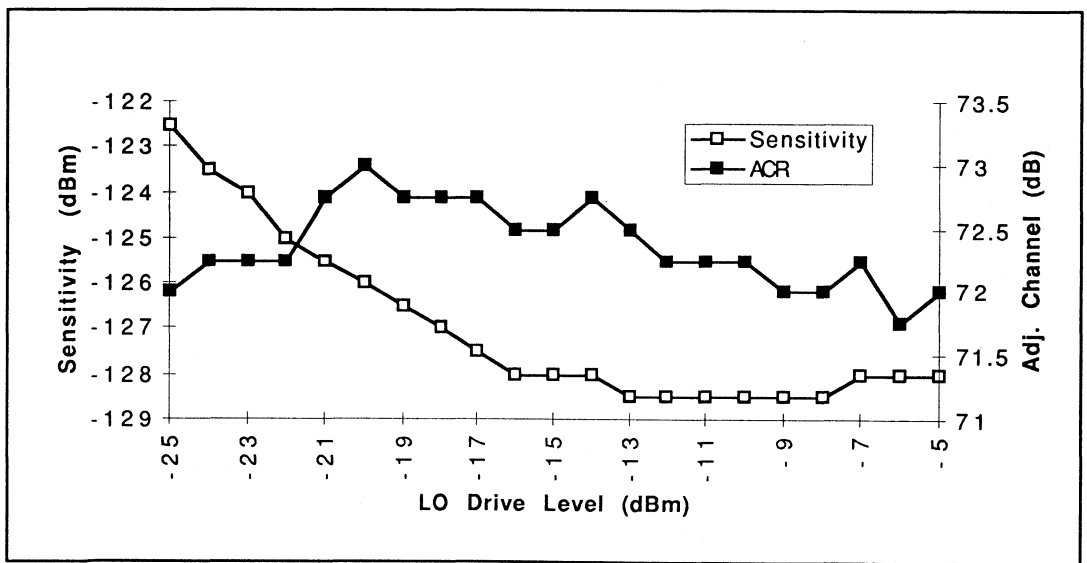


Fig.15 Sensitivity, Adjacent Channel vs LO level

SL6610

DIRECT CONVERSION FSK DATA RECEIVER

(Supersedes the October 1994 edition, DS4003 - 1.4)

This device is an advanced direct conversion receiver for operation up to 470MHz. The design is based on the SL6609A but is specifically designed for use in very small pagers i.e. credit card sized, where local oscillator re-radiation is a problem. This design has overcome this difficulty.

The device also includes a 1 volt regulator capable of sourcing up to 5mA, a battery flag and the facility of incorporating a more complex post detection filter off-chip. Both battery flag and data outputs have open collector outputs to ease their interface with other devices.

Adjacent channel rejection is provided using tuneable gyrator filters. To assist operation in the presence of large interfering signals both RF and audio AGC functions are provided.

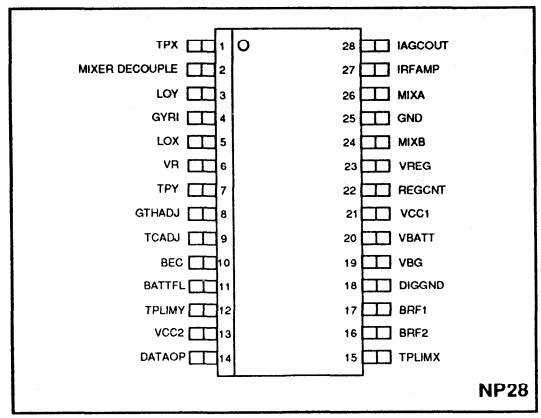


Fig.1 Pin connections

FEATURES

- Very low power operation - typ 3.0mW
- Superior sensitivity of -130dBm
- Operation at wide range of paging data rates 512, 1200, 2400 baud
- Small package offering SSOP
- Excellent performance of LO Rejection

APPLICATIONS

- Credit card pagers
- Watch pagers
- Small form factor pagers i.e. PCMCIA

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6V
Storage temperature	-55°C to +150°C
Operating temperature	-20°C to +70°C

ORDERING INFORMATION

SL6610 / KG / NPDS - SSOP devices in anti-static sticks
SL6610 / KG / NPDE - SSOP devices in tape and reel

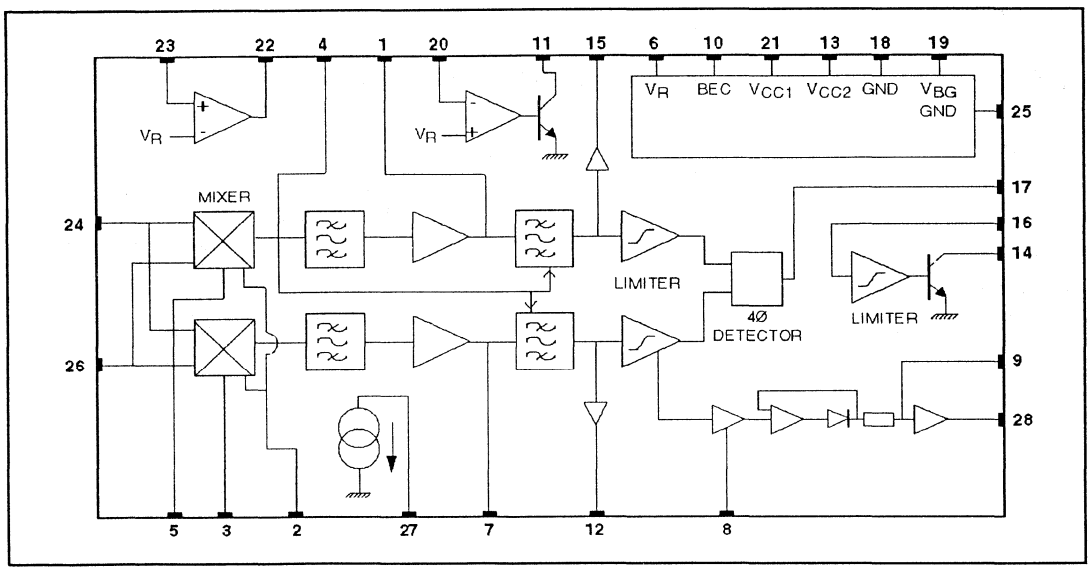


Fig.2 Block diagram of SL6610

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
Tamb = 25°C, VCC1 = 1.3V, VCC2 = 2.7V

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
VCC1 - Supply voltage	21	0.95	1.3	2.8	V	VCC1 $\leq$ VCC2 - 0.7 volts
VCC2 - Supply voltage	13	1.8	2.7	3.5	V	
ICC1 - Supply current	21,27,28		1.5	1.8	mA	Includes IRF. Does not include regulator supply. Audio AGC inactive
ICC2 - Supply current	11,13,14		550	700	µA	Batt flag & Data O/P high Pin 27 voltage: 0.3 - 1.3V
Power down ICC1	21,27,28			1	µA	
Power down ICC2	11,13,14			8	µA	
1 volt regulator	23	0.95	1.0	1.05	V	I Load = 3mA. Ext PNP. ß >= 100, V_{CE} = 0.1 volt
Band gap voltage reference	19	1.15	1.21	1.27	V	
Band gap current source	19			20	µA	
Voltage reference	6	0.93	1.0	1.07	V	
Voltage reference sink/source	6			10	µA	VCC1 > 1.1V
1 volt regulator load current		0.25	3	5	mA	
Turn on Time			5		ms	Stable data o/p when 3dB above sensitivity. C_{BG} and C_{VR} = 2.2µF
Turn off Time			1		ms	Fall to 10% of steady state current C_{BG} and C_{VR} = 2.2µF
Detector output current	17		+/-4		µA	
RF current source						
Current Source (IRF)	27	400	500	600	µA	Pin 27 voltage: 0.3 - 1.3V
Decoder						
Sensitivity		40			µVrms	Signal injected at TPX and TPY B.E.R. $\leq$ 1 in 30 5KHz deviation @ 1200 bits/sec BRF capacitor = 1nF
Output mark space ratio	14	7:9		9:7		
Data O/P Sink Current	14	100		500	µA	Output logic low
Data O/P Leakage Current	14			1.0	µA	Output logic high

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
Tamb = 25°C, VCC1 = 1.3V, VCC2 = 2.7V

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
Battery Economy						
Input logic high	10	(V_{CC2} - 0.3)			V	Powered Up
Input logic low	10			0.3	V	Powered Down
Input current	10		0.05	1	µA	Powered Up
Input current	10		6	8	µA	Powered down transient initial
Battery Flag Input						
Input current	20			1		µA
Battery Flag Output						
Battfl Sink Current	11	50		500	µA	(VBATT-VR) > 20mV
Battfl leakage current	11			1	µA	(VBATT-VR) < -20mV
Mixers						
Gain to "IF Test"		34		41	dB	LO inputs driven in parallel with 50mVRMS @ 50MHz.IF = 2kHz
RF input impedance	24, 26					See Figs.8a, 8b
LO input impedance	3, 5					See Fig.9
LO DC bias voltage	3, 5				V	Equal to Pin 21 (VCC1)
Audio AGC						
Max Audio AGC Sink Current	28	45	65	85	µA	

RECEIVER CHARACTERISTICS (GPS Demonstration board)

Measurement conditions unless stated V_{CC1} = 1.3V, V_{CC2} = 2.7V, LNA = 18dB Power Gain, 2dB Noise figure,
Carrier frequency 153MHz, BER 1 in 30, Tamb = 25°C
(TPx/TPy typically:- 160mV_{pp} ± 10% for - 73dBm RF input to the LNA)

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
Sensitivity		-130	-128	-125	dBm	1200 bps Δf = 4kHz LO = -18dBm
Intermodulation		52	56		dB	1200 bps Δf = 4kHz LO = -18dBm
Adjacent channel		68	73		dB	1200 bps Δf = 4kHz LO = -18dBm Channel spacing 25kHz
Centre frequency acceptance			+/-2.3		kHz	1200 bps Δf = 4kHz LO = -18dBm
Deviation acceptance			+/-2.2		kHz	1200 bps Δf = 4kHz LO = -18dBm

RECEIVER CHARACTERISTICS (GPS Demonstration board)

Measurement conditions unless stated V_{CC1} = 1.3V, V_{CC2} = 2.7V, LNA = 20dB Power Gain, 2dB Noise figure,
Carrier frequency 282MHz, BER 1 in 30, Tamb = 25°C
(TPx/TPy typically:- 160mV$_{pp}$ ±10% for - 73dBm RF input to the LNA)

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
Sensitivity		-130	-128 -125.5	-125 -122	dBm dBm	1200 bps Δf = 4kHz 2400 bps Δf = 4.5kHz LO = -15dBm
Intermodulation (IP3)		52 49	56 53.5		dB	1200 bps Δf = 4kHz 2400 bps Δf = 4.5kHz LO = -15dBm
Intermodulation (IP2)		47	52		dB	1200 bps Δf = 4kHz LO = -15dBm
Adjacent channel		67 64	72.5 69.5		dB	1200 bps Δf = 4kHz 2400 bps Δf = 4.5kHz LO = -15dBm Channel spacing 25kHz
Centre frequency acceptance		+/-1.9	+/-2.3 +/-2		kHz	1200 bps Δf = 4kHz 2400 bps Δf = 4.5kHz LO = -15dBm
Deviation acceptance			+/-2.2 +/-2		kHz	1200 bps Δf = 4kHz 2400 bps Δf = 4.5kHz LO = -15dBm

RECEIVER CHARACTERISTICS

Measurement conditions unless stated V_{CC1} = 1.3V, V_{CC2} = 2.7V, LNA = 22dB Power Gain, 2dB Noise figure,
Carrier frequency 470MHz, BER 1 in 30, Tamb = 25°C
(TPx/TPy typically:- 140mV$_{pp}$ ±10% for - 73dBm RF input to the LNA)

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
Sensitivity		-128	-126	-123	dBm	1200 bps Δf = 4kHz LO = -15dBm
Intermodulation		50	55.5		dB	1200 bps Δf = 4kHz LO = -15dBm
Adjacent channel		67	72.5		dB	1200 bps Δf = 4kHz LO = -15dBm Channel spacing 25kHz
Centre frequency acceptance			+/- 2.3		kHz	1200 bps Δf = 4kHz LO = -15dBm
Deviation acceptance			+/- 2.2		kHz	1200 bps Δf = 4kHz LO = -15dBm

RECEIVER CHARACTERISTICS (GPS Demonstration board)

Measurement conditions unless stated LNA = 18dB Power Gain, 2dB Noise figure,
Carrier frequency 282MHz, BER 1 in 30, Tamb = 0 to 45°C, Vcc2 = 2.7V, Vcc1 = 1.2V to 1.6V
(TPx/TPy typically:- 120mV$_{PP}$ ± 10% for - 73dBm RF input to the LNA)

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
Sensitivity (Desense from 25°C, Vcc1 = 1.3V)				1.5	dB	1200 bps Δf = 4kHz LO = -15dBm
Intermodulation (IP3)		53	58		dB	1200 bps Δf = 4kHz LO = -15dBm
Intermodulation (IP2)		47	53		dB	1200 bps Δf = 4kHz LO = -15dBm
Adjacent channel		66	72.5		dB kHz	1200 bps Δf = 4kHz LO = -15dBm Channel spacing 25kHz
Centre frequency acceptance		+/-1.8	+/-2.3		kHz	1200 bps Δf = 4kHz LO = -15dBm
Deviation acceptance			+/-2.2		kHz	1200 bps Δf = 4kHz LO = -15dBm
LO Rejection:- 0.5dB Sensitivity loss 3dB Sensitivity loss		 -59 -52	 -55 -48	 -44	 dBm dBm	 Level of local oscillator at the RF input to the LNA

OPERATION OF SL6610

The SL6610 is a Direct Converson Receiver designed for use up to 470MHz. It is available in a 28 pin SSOP package and it integrates all the facilities required for the conversion of an RF FSK signal to a base-band data signal.

Low Noise Amplifier

To achieve optimum performance it is necessary to incorporate a Low Noise RF Amplifier at the front end of the receiver. This is easily biased using the on chip voltage and current sources provided.

All voltages and current sources used for bias of the RF amplifier, receiver and mixers should be RF decoupled using suitable capacitors (see fig.4 for a suitable Low-Noise-Amplifier).

Local Oscillator

The Local Oscillator signal is applied to the device in phase quadrature. This can be achieved with the use of two RC networks operating at the -3dB/45° transfer characteristic, giving a full 90° phase differential between the LO ports of the device. Each LO port of the device also requires an equal level of drive from the Oscillator. (see Fig.5).

Gyrator Filters

The on chip filters include an adjustable gyrator filter. This may be adjusted with the use of an additional resistor between pin 4 and GND. This allows flexibility of filter characterstics and also allows for compensation for possible process variations.

Audio AGC

The Audio AGC fundamentally consists of a current sink which is controlled by the audio (baseband data) signal. It has three parameters that may be controlled by the user. These are the Attack (turn on) time, Decay (duration) time and Threshold level (see Fig.6 and 7). See Application note for details.

Regulator

The on chip regulator must be used in conjunction with a suitable PNP transistor to achieve regulation. As the transistor forms part of the regulator feedback loop the transistor should exhibit the following characteristics:-

$H_{FE} >= 100$ for $V_{CE} >= 0.1V$

Pin Number	Pin Name	Pin Description
1	TPX	X channel pre-gyrator filter test-point. This can be used for input and output
2	MIX-DEC	Mixer bias de-couple pin
3	LOY	LO input channel Y
4	GYRI	Gyrator current adjust pin
5	LOX	LO input channel X
6	VR	VREF 1.0 V internal signal ground
7	TPY	Y channel pre-gyrator filter test point, input or output
8	GTHADJ	Audio AGC gain and threshold adjust. RSSI signal indicator
9	TCADJ	Audio AGC time constant adjust
10	BEC	Battery economy control
11	BATTFL	Battery flag output
12	TPLIMY	Y channel limiter (post gyrator filter) test point, output only
13	VCC2	Supply connection
14	DATAOP	Data output pin
15	TPLIMX	X channel limiter (post gyrator filter) test point, output only
16	BRF2	Bit rate filter 2, input to data output stage
17	BRF1	Bit rate filter 1, output from detector
18	DIG GND	Digital ground
19	VBG	Bandgap voltage output
20	VBATT	Battery flag input voltage
21	VCC1	Supply connection
22	REGCNT	1V regulator control external PNP drive
23	VREG	1V regulator output voltage
24	MIXB	Mixer input B
25	GND	Ground
26	MIXA	Mixer input A
27	IRFAMP	Current source for external LNA. Value of current output will decrease at high mixer input signal levels due to RF AGC
28	IAGCOUT	Audio AGC output current

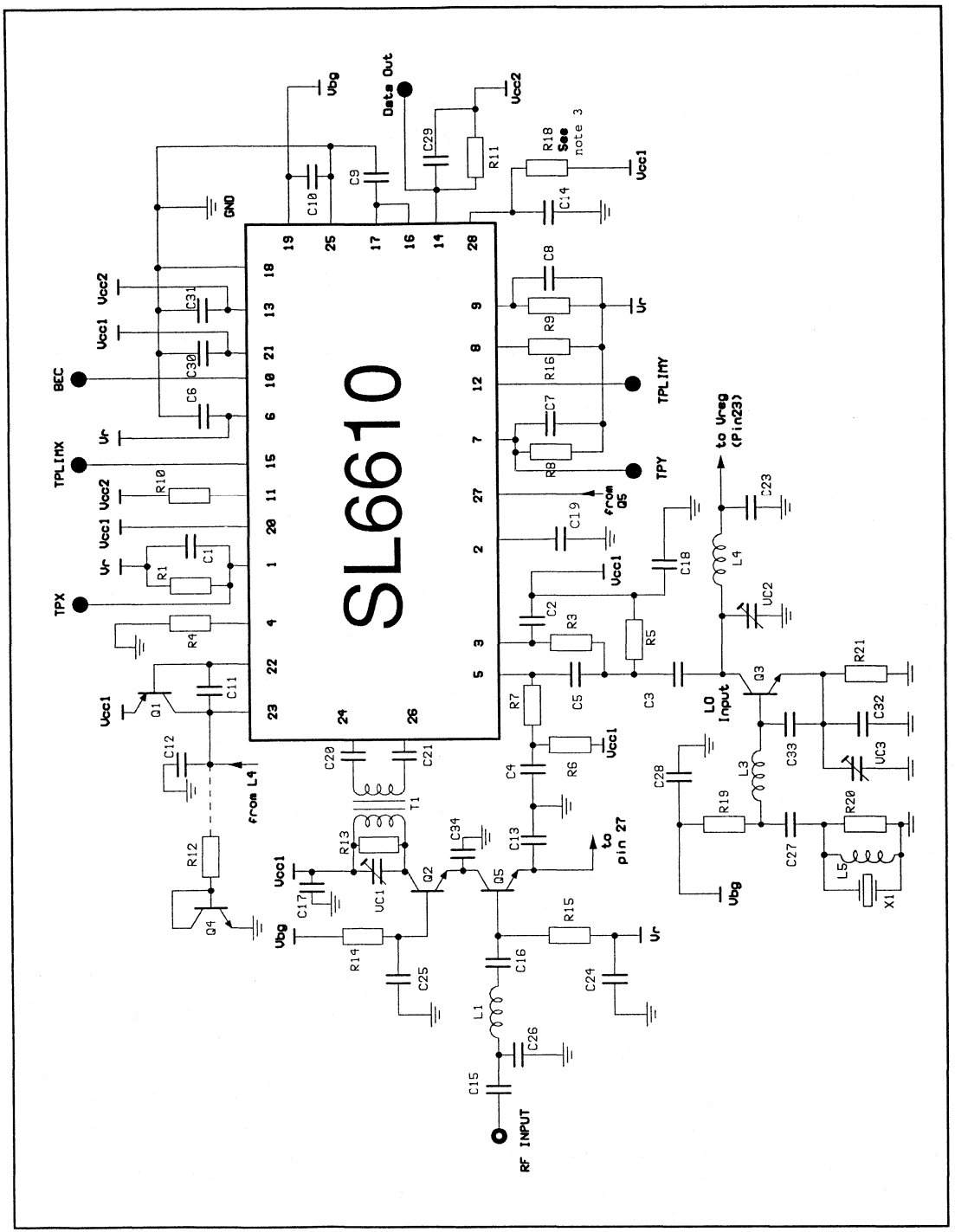


Fig.3 Application circuit board

COMPONENTS LIST FOR APPLICATION BOARD At 282MHz, 25kHz Channel Spacing.

(LO Circuit in Fig.3)

Resistors

R1	open circuit
R2	not used
R3	100
R4	100k
R5	1k
R6	1k
R7	100
R8	open circuit
R9	220k
R10	1M
R11	100k (6)
R12	not used
R13	1k5(1)
R14	4k7
R15	4k7
R16	33k
R17	not used
R18	0R (3)
R19	10k
R20	620
R21	1k
R22	open circuit

Capacitors

C1	1n
C2	2p7
C3	4p7
C4	1n
C5	2p7
C6	2u2
C7	1n
C8	100n
C9	1n (2)
C10	2u2
C11	100n
C12	1n
C13	1n
C14	1n
C15	1n
C16	1n
C17	1n
C17a	1n
C18	1n
C19	100n
C20	1n
C21	1n
C22	not used
C23	1n
C24	1n
C25	1n
C26	6p8
C27	1n
C28	1n
C29	100p
C30	2u2
C31	2u2
C32	4p7
C33	4p7
C34	3p3
C35	not used
VC1	1-10p
VC2	1-10p
VC3	1-10p

Inductors

L1	68n (4)
L2	not used (3)
L3	470n
L4	39n
L5	680n

Active Components

Q1	FMMT589
Q2	2SC5065 (Toshiba)
Q3	BFT25A (Philips)
Q4	not used
Q5	2SC5065 (Toshiba)
D1	Panasonic MA862 (5)

Misc

T1	30nH 1:1 Coilcraft M1686-A
Xtal	5th Overtone 94.075MHz

Notes

1. The values of R13 is determined by the set-up procedure. See Application Note.

2. The value of C9 is determined by the output data rate. Use 2nF for 512bps, 1nF for 1200bps and 470pF for 2400bps.

3. L2 is used in the Audio AGC circuit (see Fig. 6). For the characteristics of the Audio AGC current source see Fig.7. If the audio AGC is not required then the current source (Pin 28) may be disabled by connecting Pin 9 (TCADJ) to VR (Pin 6) and by connecting Pin 28 (IAGCOUT) to Vcc1, (R18). The voltage at Pin 8 may still be used as an RSSI. R9, C8, C14, C19, R17 and D1 may then be omitted. See Fig.6 for AGC component values.

4. L1 and C26 form the low noise matching network for the RF amplifier. The values given are for the RF amplifier specified in the Applications Circuit with no Audio AGC connected. i.e. R17 and D1 omitted.

5. Suggested diode for use with the Audio AGC circuit (see Fig.6) (D1 is not included on the general demonstration circuit).

6. The value of R11 is dependent on the data output load. R11 should allow sufficient current to drive the data output load.

COMPONENTS LIST FOR APPLICATION BOARD At 470MHz, 25kHz Channel Spacing.
(LO circuit is 50Ω network as in Fig.5 - crystal oscillator not specified)

Resistors

R1	open circuit
R2	not used
R3	100
R4	100k
R5	100
R6	100
R7	100
R8	open circuit
R9	220k
R10	1M
R11	100k (2)
R12	300 (3)
R13	3k9 (1)
R14	4k7
R15	4k7
R16	33k
R17	open circuit (4)
R18	0R (4)
R22	open circuit

Capacitors

C1	1n
C2	3.3pF
C3	1n
C4	1n
C5	3.9pF
C6	2u2
C7	1n
C8	100n
C9	1n (2)
C10	2u2
C11	100n
C12	1n
C13	1n
C14	1n
C15	1n
C16	1n
C17	1n
C18	1n
C19	100n
C20	1n
C21	1n
C22	not used
C23	not used
C24	1n
C25	1n
C26	open circuit
C27	not used
C28	not used
C29	100p
C30	2u2
C31	2u2
C34	1p5
VC1	1-3pF

Inductors

L1	47nH (5)
L2	not used (3)
T1	16nH 2 Turn 1:1 (Coilcraft) Q4123-A

Active Components

Q1	Zetex FMMT589
Q2	Philips BFT25A
Q3	Not Used
Q4	Philips BFT25A(3)
Q5	Philips BFT25A
D1	Panasonic MA862(6)

Notes

1. The values of R13 is determined by the set-up procedure. See Application Note.

2. The value of "C9" is determined by the output data rate. Use 2nF for 512bps, 1nF for 1200bps and 470pF for 2400bps.

3. R12 & Q4 form a dummy load for the regulator. Permitted load currents for the regulator are 250μA to 5mA. The 1V regulator (output Pin 23) can be switched off by connecting Pin 23 directly to VCC2. Q1, Q4, R12 and C12 must then be omitted

4. L2 is used in the Audio AGC circuit (see Fig.6). For the characteristics of the Audio AGC current source see figure 7. If the Audio AGC is not required then the current source (Pin 28) may be disabled by connecting Pin 9 (TCADJ) to VR (Pin 6) and by connecting Pin 28 (IAGCOUT) to Vcc1, (R18). The voltage at Pin 8 may still be used as an RSSI. R9, C8, C14, C19, R17 and D1 may then be omitted.

5. L1 and C26 form the low noise matching network for the RF amplifier. The values given are for the RF amplifier specified in the Applications Circuit with no Audio AGC connected. i.e. R17 and D1 omitted.

6. Suggested diode for use with the Audio AGC circuit (D1 is not included on the general demonstration circuit).

7. The value of R11 is dependent on the data output load. R11 should allow sufficient current to drive the data output load.

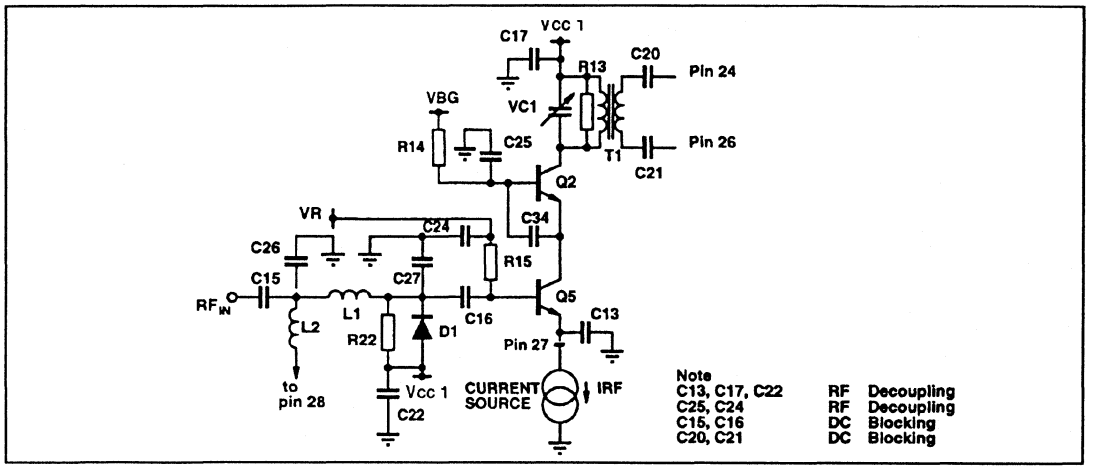


Fig.4 RF amplifier

RF Amplifier Components Values

Resistors		Capacitors		
R14, R15	4k7	C13, C15	1nF	Active components
R13	see note 1	C16, C17	1nF	D1 MA862 (Panasonic)
R22	47k	C20, C21	1nF see note 2	
		C24, C25	1nF	
		L2	820nH	

Notes:

(1) The value of R13 is determined by the set up procedure (See "Set up for optimum performance").

(2) C20 and C21 are purely for deomonstration purposes. Pin 24 and Pin 26 may be DC coupled provided that no DC voltage is applied to the mixer inputs.

Frequency Dependent Components

	153MHz	280MHz	450MHz
C26	not used	6.8p	not used
C27	not used	not used	not used
L1	150nH	68nH	39nH
C34	3p3	2p2	1p5
T1	100nH	30nH	16nH
	Coilcraft N2261-A	Coilcraft M1686-A	Coilcraft Q4123-A
VC1	1-10pF	1-10pF	1-3pF
Q4, Q5	Toshiba 2SC5065	Toshiba 2SC5065	Philips BFT25A

(See also Lo drive Network)

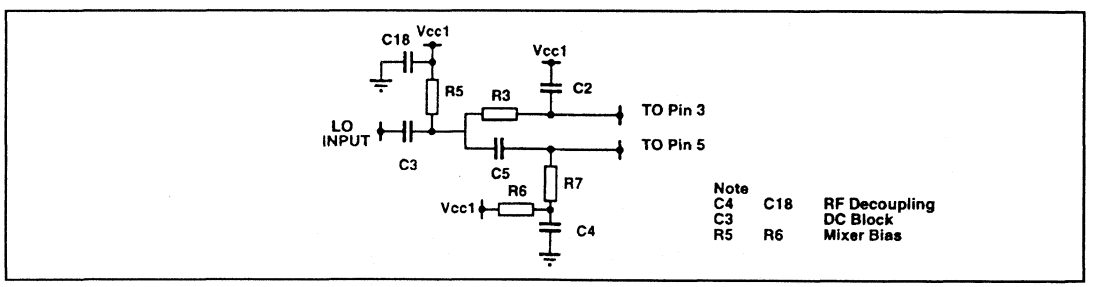


Fig.5 Local oscillator drive network

LO Drive Network Component Values

50Ohm input impedance (External LO injection)

	153MHz	280MHz	450MHz
C2	10p	5p6	3p3
C5	10p	5p6	3p9

C3, C4, C18 = 1n

R3, R5, R6, R7 = 100Ohms

Higher Input Impedance (crystal oscillator input)

	153MHz	280MHz	450MHz
C3	Set by load allowable on crystal oscillator (typical 4p7)		
C2	10p	5p6	3p3
C5	10p	5p6	3p9
R3	100	100	100
R7	100	100	100

R5, R6 = 1k

C4, C18 = 1n

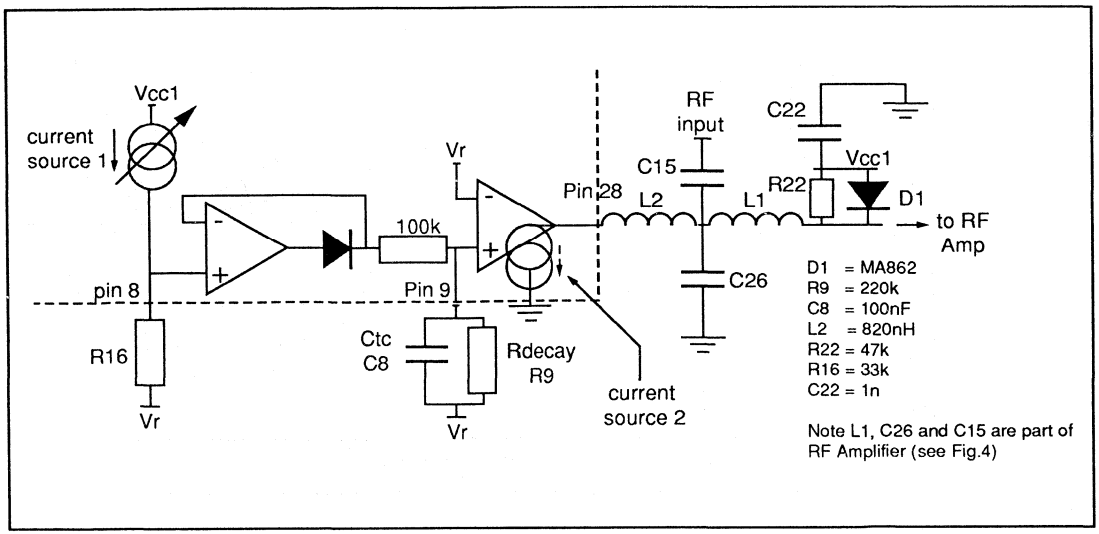


Fig.6 AGC Schematic

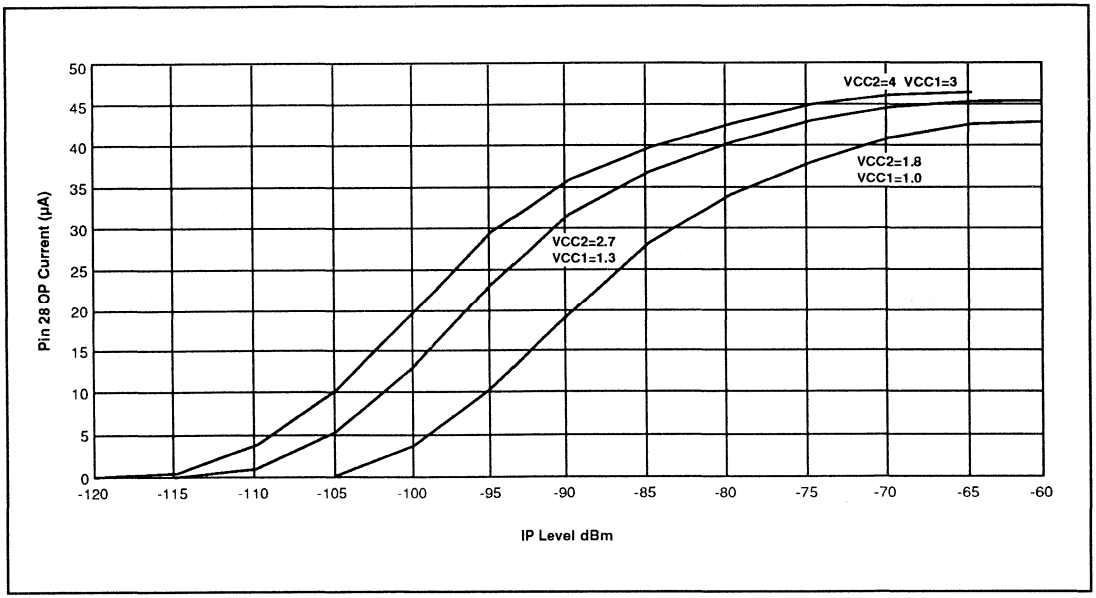


Fig.7 Audio AGC current vs. IP power at 25°C

S11

FREQ	MAG	ANG
50.000	0.969	-7.20
100.000	0.958	-14.45
150.000	0.942	-20.59
200.000	0.917	-26.40
250.000	0.893	-33.26
300.000	0.858	-39.84
350.000	0.832	-44.78
400.000	0.806	-49.01
450.000	0.781	-54.00
500.000	0.755	-59.53
550.000	0.743	-64-35
600.000	0.725	-68.43
650.000	0.703	-73.01
700.000	0.680	-78.74
750.000	0.666	-83.76
800.000	0.653	-87.48
850.000	0.636	-91.32
900.000	0.615	-97.17
950.000	0.604	-102.84
1000.00	0.600	-105.23

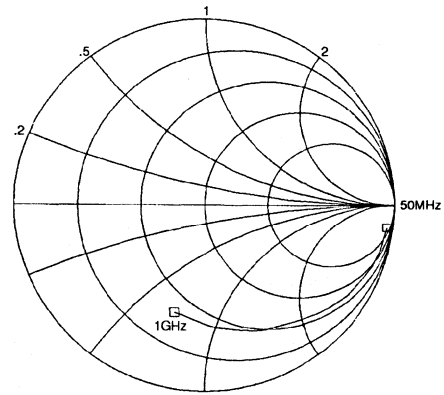


Fig.8a SL6609A Mixer A input S-Parameters

S11

FREQ	MAG	ANG
50.000	0.970	-7.06
100.000	0.960	-13.83
150.000	0.945	-19.90
200.000	0.919	-25.70
250.000	0.902	-32.18
300.000	0.872	-38.03
350.000	0.850	-43.07
400.000	0.825	-48.27
450.000	0.803	-53.58
500.000	0.776	-58.49
550.000	0.760	-63.08
600.000	0.739	-67.98
650.000	0.717	-72.63
700.000	0.698	-76.96
750.000	0.683	-81.09
800.000	0.666	-85.49
850.000	0.659	-89.51
900.000	0.647	-93.90
950.000	0.637	-98.42
1000.00	0.634	-102.40

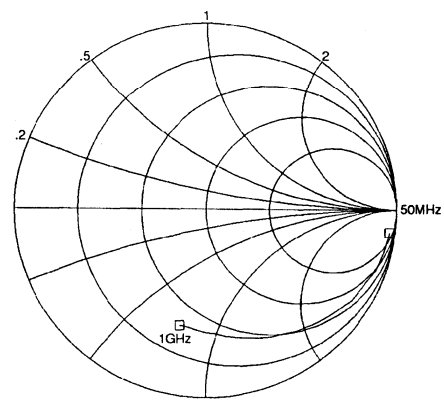


Fig.8b SL6609A Mixer B input S-Parameters

S11

FREQ	MAG	ANG
50.000	0.993	-4.17
100.000	0.995	-8.43
150.000	0.997	-12.88
200.000	0.997	-17.57
250.000	0.996	-22.63
300.000	0.986	-28.16
350.000	0.965	-33.87
400.000	0.936	-39.17
450.000	0.902	-43.88
500.000	0.872	-48.54
550.000	0.838	-52.81
600.000	0.804	-56.60
650.000	0.798	-59.47
700.000	0.810	-65.19
750.000	0.784	-71.49
800.000	0.779	-75.97
850.000	0.790	-82.54
900.000	0.788	-91.16
950.000	0.768	-100.20
1000.00	0.743	-108.52

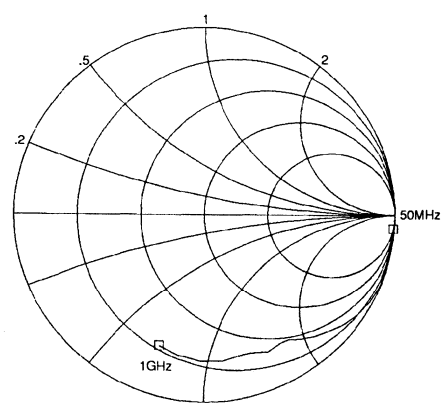


Fig.9 SL6609A LO X,Y inputs S-Parameters

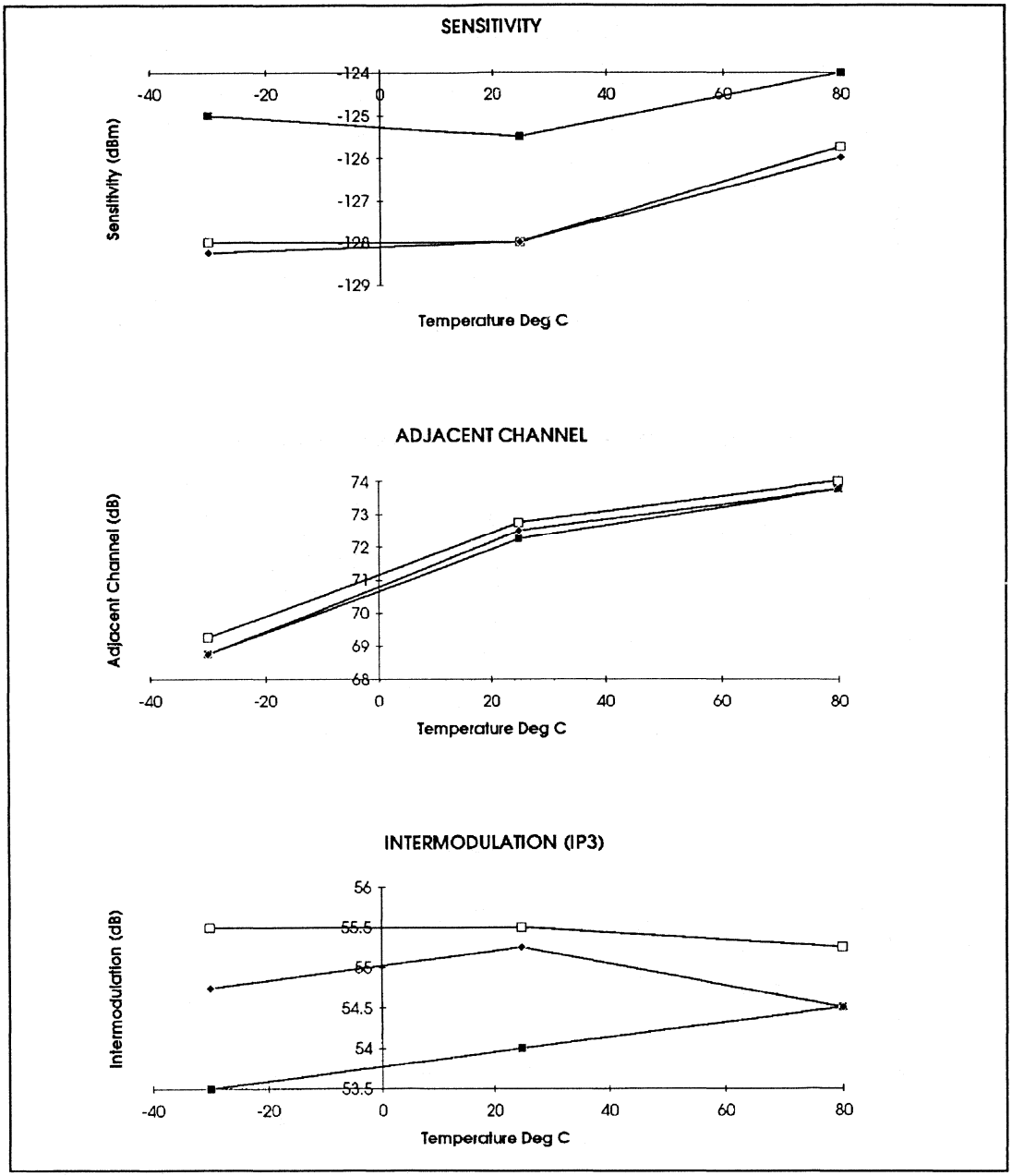
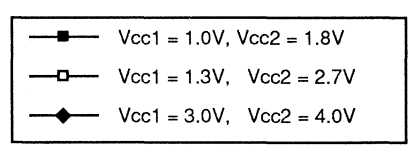


Fig.10a AC parameters vs. supply and temperature

Conditions:- 282MHz GPS demonstration board i.e. 20dB LNA, 2dB noise figure, carrier frequency 282MHz, 1200bps baud rate, 4kHz deviation frequency, BER 1 in 30.



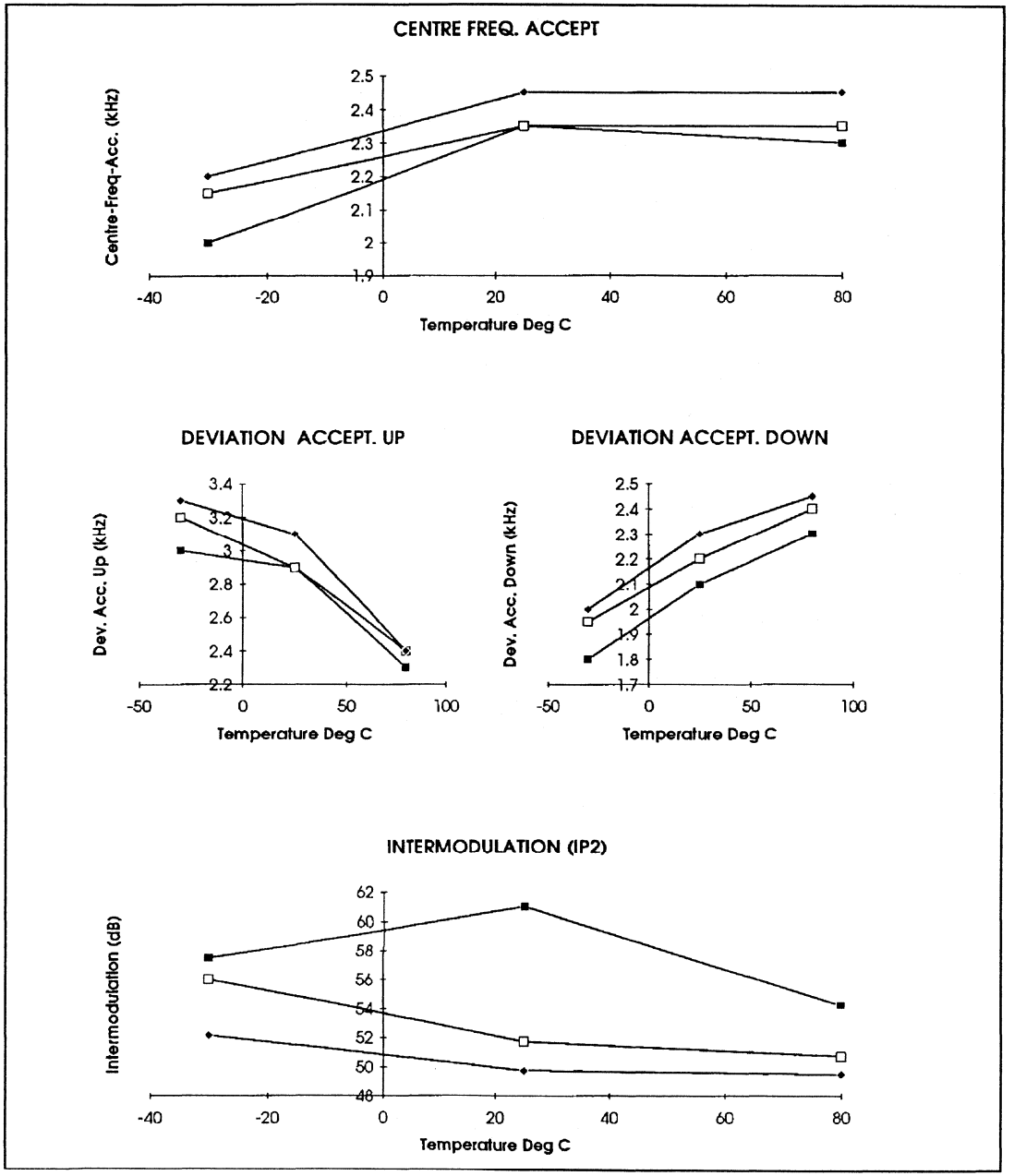
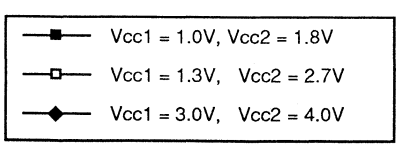


Fig. 10b AC parameters vs. supply and temperature

Conditions:- 282MHz GPS demonstration board i.e. 20dB LNA, 2dB noise figure, carrier frequency 282MHz, 1200bps baud rate, 4kHz deviation frequency, BER 1 in 30.



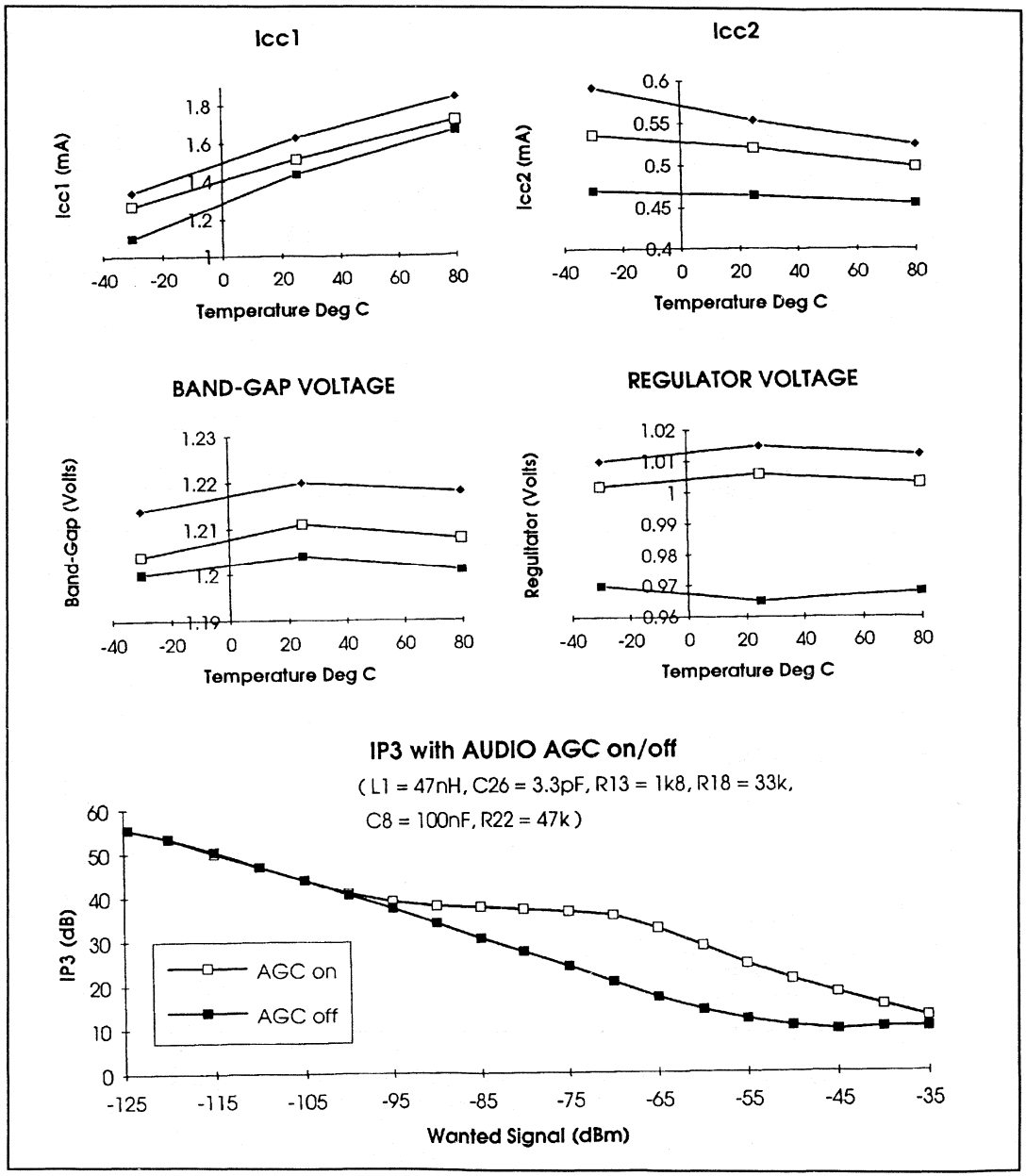


Fig.11 DC parameters vs. supply and temperature (IP3 vs audio AGC both on and off)

Conditions:- **ICC1 includes 500µA LNA current but does not include the regulator supply (audio AGC inactive). ICC2 measured with BATT FLAG and DATA O/P HIGH, Fc = 282MHz.**

Note 1- **IP3 is level above wanted needed to reduce receiver to 1 in 30 B.E.R.**

- Vcc1 = 0.98V, Vcc2 = 1.78V
- Vcc1 = 1.3V, Vcc2 = 2.7V
- Vcc1 = 3.0V, Vcc2 = 4.0V

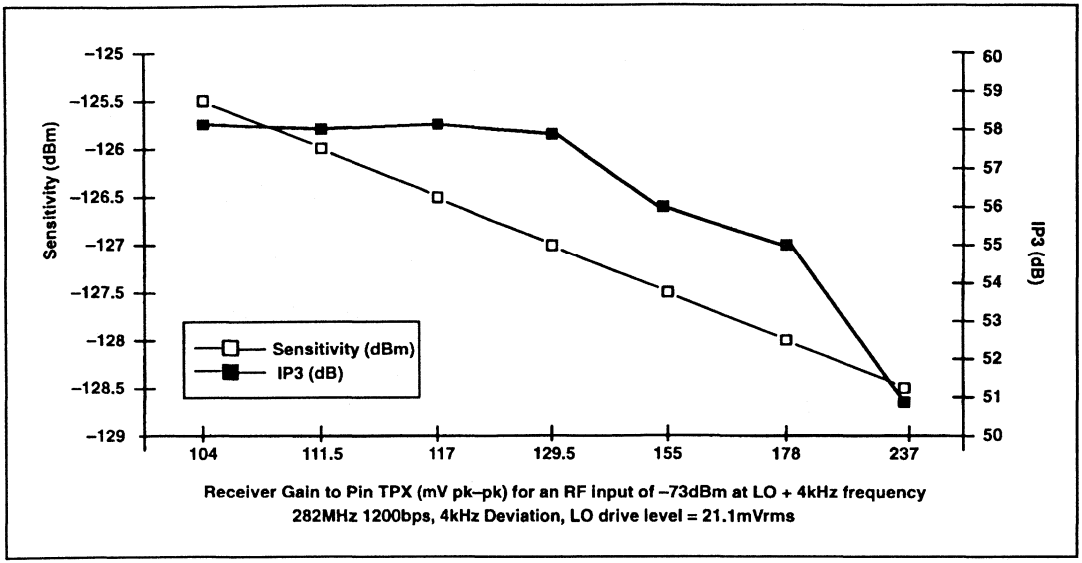


Fig.12 Sensitivity, IP3 vs Receiver Gain

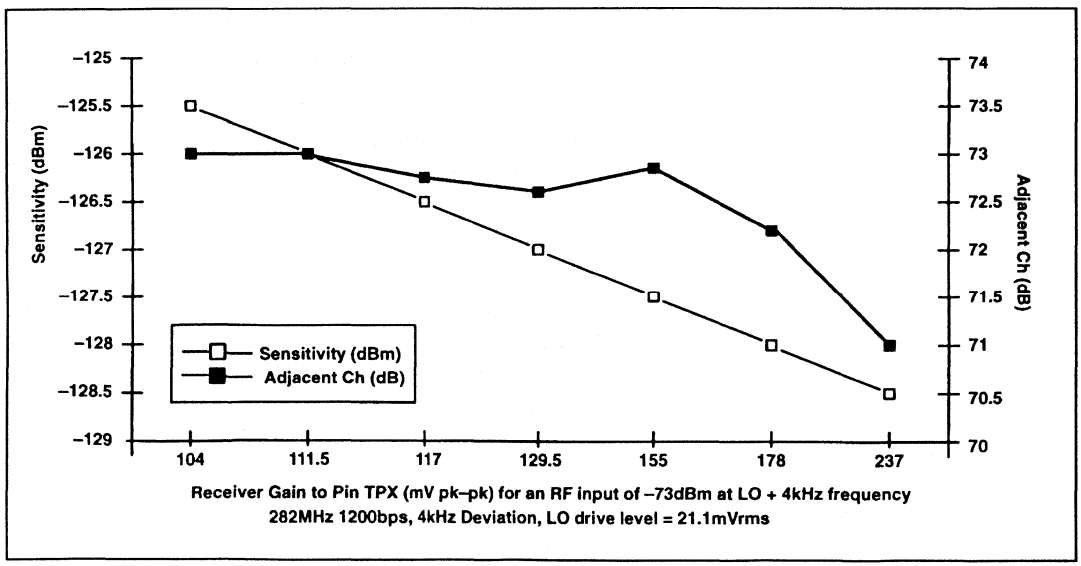


Fig.13 Sensitivity, adjacent Channel vs Receiver Gain

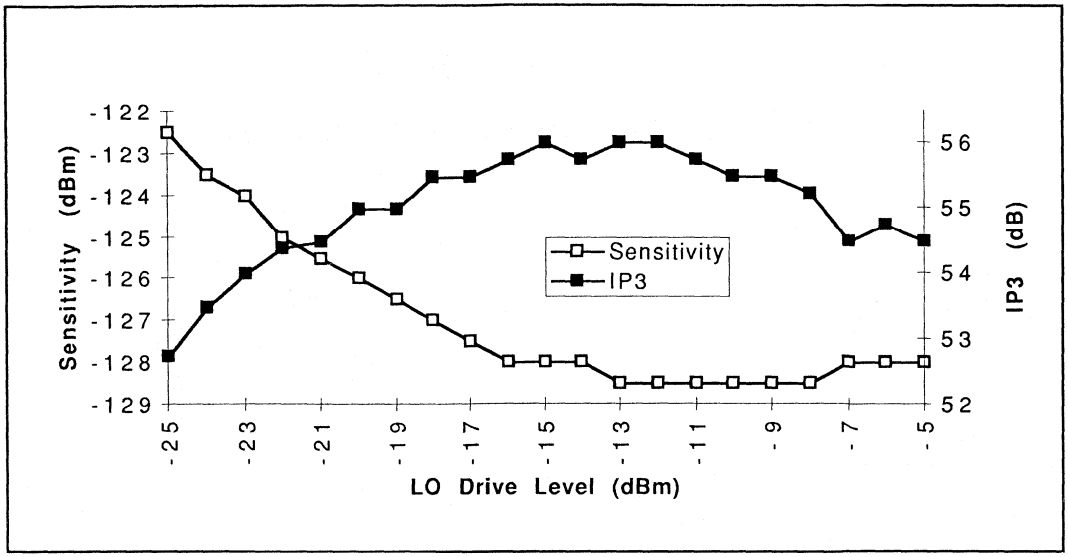


Fig.14 Sensitivity, IP3 vs LO level

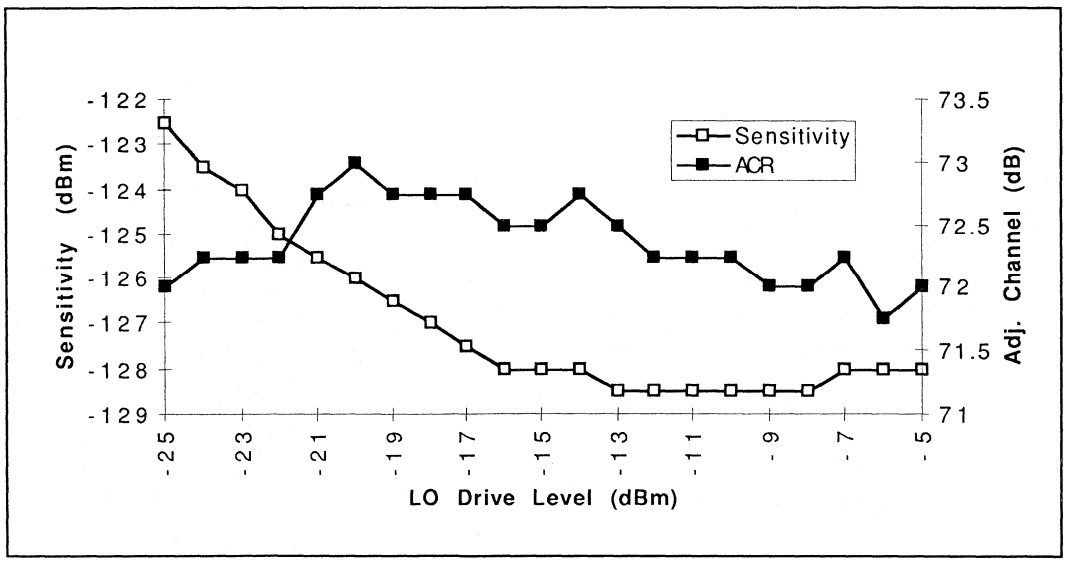


Fig.15 Sensitivity, Adjacent Channel vs LO level

SL6619

DIRECT CONVERSION FSK DATA RECEIVER

(Supersedes the July 1995 Edition D.S. 3853 – 2.3)

The SL6619 is an advanced Direct Conversion FSK Data Receiver for operation up to 450MHz. The device integrates all functions to convert a binary FSK modulated RF signal into a demodulated data stream.

Adjacent Channel Rejection is provided using tuneable gyrator filters. RF and Audio AGC functions assist operation when large interfering signals are present and an Automatic Frequency Control (AFC) function is provided to extend Centre Frequency Acceptance.

FEATURES

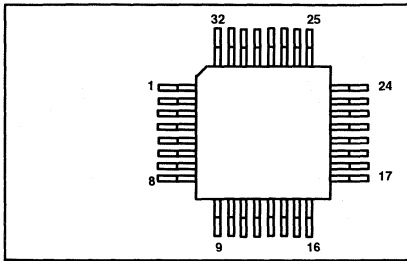
- Very low power operation from single cell
- Superior sensitivity
- Operation at 512, 1200 and 2400 baud
- On–chip 1Volt regulator
- 1mm height miniature package offering
- Automatic frequency control function
- Programmable post detection filter
- AGC detection circuitry
- Powerdown function
- Battery strength indicator

APPLICATIONS

- Pagers: including Credit card, PCMCIA and Watch pagers.
- Low data rate receivers e.g. Security Systems

ABSOLUTE MAXIMUM RATINGS

Supply voltage	4.0V
Storage temperature	–55°C to +150°C
Operating temperature	–20°C to +70°C



PIN	NAME	PIN	NAME
1	IRF	17	TPQ
2	GND	18	VREF
3	MIXIP A	19	AFC OP
4	MIX DEC	20	BEC
5	MIXIP B	21	DATA OP
6	REG CNT	22	VCC2
7	VREG	23	BATT FLAG
8	TPI	24	AFC1
9	I1	25	AFC2
10	I2	26	BRF CNT
11	VCC1	27	BRF1
12	LOIP I	28	VBATT
13	GYRI	29	TP LIM I
14	LOIP Q	30	IAGC OP
15	Q1	31	TC ADJ
16	Q2	32	GTH ADJ

Fig. 1 Pin connections

ORDERING INFORMATION

SL6619/KG/TP1N – 1mm TQFP device dry packed supplied in trays.
SL6619/KG/TP1Q – 1mm TQFP devices dry packed supplied in tape and reel.

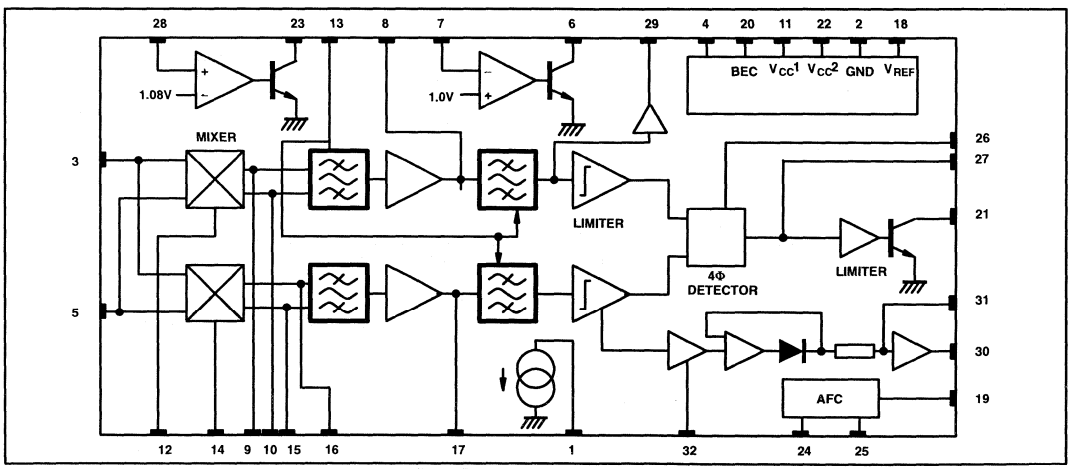


Fig. 2 Block diagram of SL6619

GEC PLESSEY
SEMICONDUCTORS

SL6649-1

200MHz DIRECT CONVERSION FSK DATA RECEIVER

(Supersedes edition in August 1994 Personal Communications IC Handbook)

The SL6649-1 is a low power direct conversion radio receiver for the reception of frequency shift keyed transmissions. It features the capability of 'power down' for battery conservation.

The device also includes a low battery flag indicator.

FEATURES

- Very Low Power Operation - typ. 3.7mW
- Single Cell Operation with External Inverter
- Complete Radio Receiver in One Package
- Operation up to 200MHz
- 100nV Typical Sensitivity
- Operates up to 1200 BPS
- On Chip Tunable Active Filters
- Minimum External Component Count
- Low Power Down Current Typical 5µA

APPLICATIONS

- Low Power Radio Data Receiver
- Wristwatch Credit Card Pager
- Radio Paging
- Ultrasonic Direction Indication
- Security Systems
- Remote Control Systems

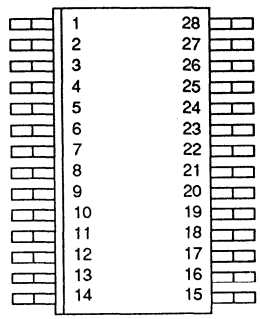
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6V
Storage Temperature	-55°C to +150°C
Operating Temperature	-20°C to +70°C

ORDERING INFORMATION

SL6649-I/KG/MPES - Small outline (MP28) supplied in tubes

SL6649-1/KG/MPEF - Small outline (MP28) supplied in tape & reel



MP28

PIN	DESCRIPTION	PIN	DESCRIPTION
1	GND	28	CHANNEL B TEST.
2	BATTERY ECON	27	LO INPUT CHANNEL B
3	GYRATOR CURRT ADJ	26	LO INPUT CHANNEL A
4	REF VOLTAGE	25	$V_{cc}1$ (MIXER)
5	BANDGAP REF VOLT	24	MIXER I/P A
6	$V_{cc}2$	23	MIXER I/P B
7	BIT RATE FILTER	22	CHANNEL A TEST
8	DATA OUTPUT	21	LO CURRENT SOURCE
9	GND	20	RFA II (EMIT) RF DEC
10	NC	19	RFA II (BASE) RF INPUT
11	NC	18	RF DEC
12	NC	17	RF O/P
13	BATT FLAG INPUT	16	COLPITTS OSC O/P DISABLE
14	BATT FLAG OUTPUT	15	NC

N.B. It is advisable to connect NC pins to ground.

Figure 1: Pin Connections - Top View

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated).
T_{amb} = 25°C, $V_{CC}1$ = 2.5V, $V_{CC}2$ = 3.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Voltage $V_{CC}1$	25	V_R	1.3	2.8	V	$V_{CC}1 \leq (V_{CC}2)-0.7$
Supply Voltage $V_{CC}2$	6,16	1.8	2.3	3.5	V	
Supply Current $I_{CC}1$	17, 25, 26, 27		1.6	2.0	mA	(I_{RF}) Included
Supply Current $I_{CC}2$	6,16		0.65	0.80	mA	
Power Down $I_{CC}1$	17, 21, 25, 26, 27		5	12	µA	Batt Econ Low
Power Down $I_{CC}2$	6,16		3	12	µA	Batt Econ Low
Bandgap Reference	5	1.15	1.22	1.35	V	
Voltage Reference	4	0.93	1.0	1.13	V	
RF Amplifier						
Supply Current (I_{RF})	17	430	535	640	µA	
Power Down	17				µA	Included in Power Down $I_{CC}1$
Mixers						
Gain to "IF Test"		32		38	dB	L.O. inputs driven in parallel with 50mV RMS @ 50MHz. IF = 2kHz
Oscillator						
Current Source	21	215	270	330	µA	
Power Down	21				µA	Included in Power Down $I_{CC}1$
Decoder						
Sensitivity				40	µVrms	Signal injected at "IF TEST" B.E.R. ≤1 in 30 5kHz deviation @ 500 bits/sec BRF capacitor = 1nF
Output Mark Space Ratio	8	7:9		9:7		
Output Logic High	8	85			$\%V_{CC}2$	
Output Logic Low				15	$\%V_{CC}2$	
Battery Economy						
Input Logic High	2	$(V_{CC}2)-0.3$			V	Powered Up
Input Logic Low	2			0.3	V	Powered Down
Input Current			0.05	1	µA	
Battery Flag						
Output High Level	14	85			$\%V_{CC}2$	Battery Low R_L > 1MΩ
Output Low Level	14			15	$\%V_{CC}2$	Battery High R_L > 1 MΩ
Flag trig Level	13	V_R-25mV		V_R+25mV	V	Voltage Reference (V_R) pin 4
Colpitts Oscillator						
Frequency		15			kHz	R=90K, pin 3 to GND
				15	kHz	R=360K, pin 3 to GND

TYPICAL ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed by design.
T_{amb} = 25°C, $V_{CC}1$ = 2.5V, $V_{CC}2$ = 3.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
RF Amplifier						
Noise Figure			5.5		dB	RS = 50Ω
Power Gain			14		dB	
Input Impedance	19					See Fig. 8
Mixer						
RF Input Impedance	23, 24					See Figs. 9 (a) and (b)
LO Input Impedance	26, 27					See Fig. 10
LO DC Bias Voltage	26, 27				V	Equal to pin 25
Detector						
Output Current	7		±4		μA	
Colpitts Oscillator						
Frequency	16		15		kHz	R = 270K, Pin 3 to GND
Output Voltage	16		20		mVp-p	R_L >> 1MΩ N.B. Refer to Channel Filter Fig. 4

RECEIVER CHARACTERISTICS (GPS DEMONSTRATION BOARD)

Measurement conditions (unless otherwise stated): Applications circuit diagram Fig.6; $V_{CC}1$ = 1.3V; $V_{CC}2$ = 2.3V; T_{amb} = 25°C; Colpitts oscillator resistor = 270kΩ; mixer input A and B phase balance = 180°; local oscillator input A and B phase balance = 90°. Measurement methods as described by CEPT Res 2 specification. F_{IN} = 153MHz (512 baud).

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Terminal Sensitivity Tone only 4/5 call reception		-127	-124	dBm	Δf = 4.5kHz, R_S = 50Ω
Deviation Acceptance		±2.5		kHz	3dB De-Sensitisation. $F_{IN} = F_{LO}$
Centre Frequency Acceptance	±2.0	±2.5		kHz	Δf = 4.5kHz
Adjacent Channel Rejection	65	70		dB	Δf = 4.5kHz Channel Spacing 25kHz
Adjacent + 1 Channel Rejection	65	70		dB	External capacitors on test
Third Order Intermod adj-1 + adj-2	52	53		dB	pins A and B.

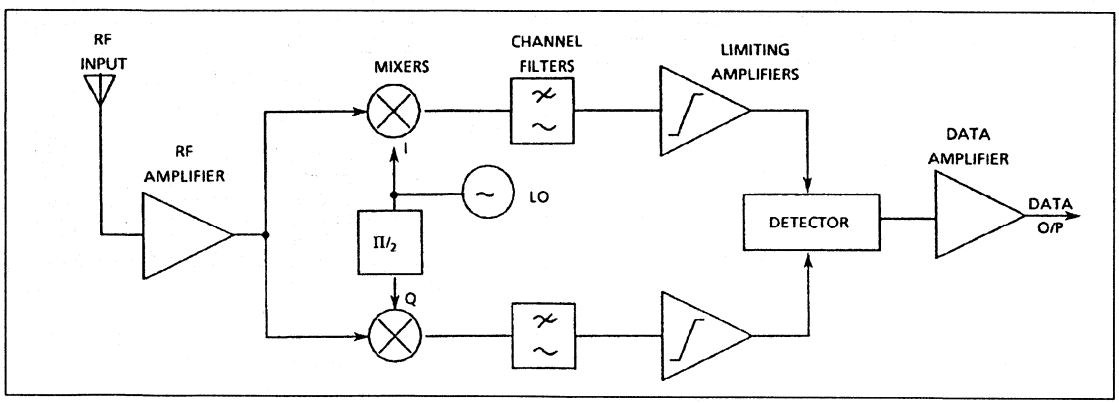


Figure 2: Block Diagram of SL6649-1 Direct Conversion Receiver

PRINCIPLE OF OPERATION

The incoming signal is split into two parts and frequency converted to baseband. The two paths are produced in phase quadrature (see Fig 2) and detected in a phase detector which provides a digital output. The quadrature network must be in the local oscillator path.

At a data rate of 512 baud and a deviation frequency of 4.5kHz, the input to the system has a demodulation index of 18. This gives a spectrum as in Fig 3. f_1 and f_0 represent the 'steady state' frequencies (i.e. modulated with continuous '1' and '0' respectively). The spectrum in Fig 3 is for reversals (a 0-1-0-1-0-1 etc. pattern) at the system bit rate; f_C is the nominal carrier frequency).

When the LO is at the nominal carrier frequency, then a continuous '0' or '1' will produce an audio frequency, at the output of the mixers corresponding to the difference between f_0 and f_C or f_1 and f_C. If the LO is precisely at fc, then the resultant output signal will be at the same frequency regardless of the data state; nevertheless, the relative phases of the two paths will reverse between '0' and '1' states. By applying the amplified outputs of the mixers to a phase discriminator, the digital data is reproduced.

TUNING THE CHANNEL FILTERS

The adjacent channel rejection performance of the SL6649-1 receiver is determined by the channel filters. To obtain optimum adjacent channel rejection, the channel filters' cut off frequency should be set to 8kHz. The process tolerances are such that the cut off frequency cannot be accurately defined, hence the channel filters must be tuned. However the receiver characteristics on the previous page can be achieved with a fixed 270kΩ resistor between pin 3 and GND.

Tuning is performed by adjusting the current in the gyrator circuits. This changes the values of the gyrator's equivalent inductance. The cut off frequency is tuned to 8kHz. To accurately define the cut off of the channel filters, a gyrator based Colpitts oscillator circuit has been included on the SL6649-1. The Colpitts oscillator and channel filters use the same type of architecture, hence there is a direct correlation between oscillator frequency and cut off frequency. By knowing the Colpitts oscillator frequency the channel filter cut off frequency can be estimated from Figure 4.

Once the channel filters have been tuned it may be necessary to disable the Colpitts oscillator. The Colpitts oscillator is disabled by connecting the Colpitts oscillator output/disable pin (pin # 16) to $V_{CC}2$. This is needed since the Colpitts oscillator may impair the performance of the receiver.

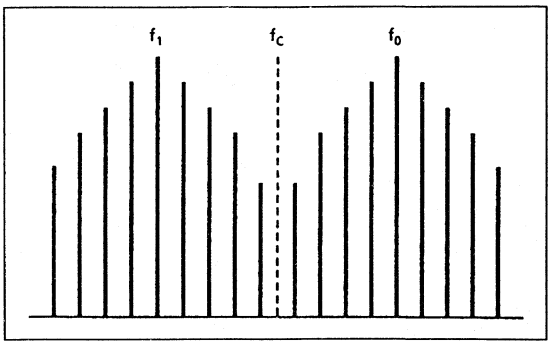


Figure 3: Spectrum Diagram

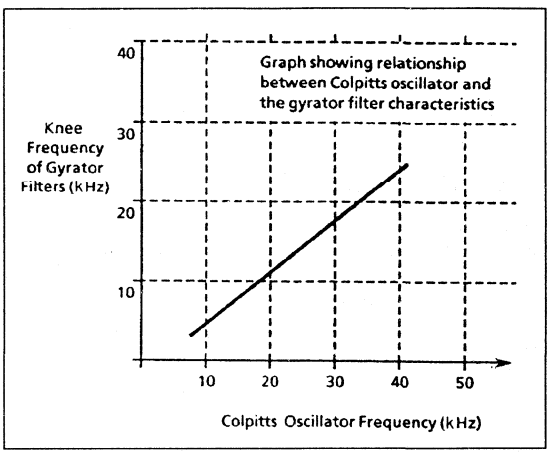


Figure 4

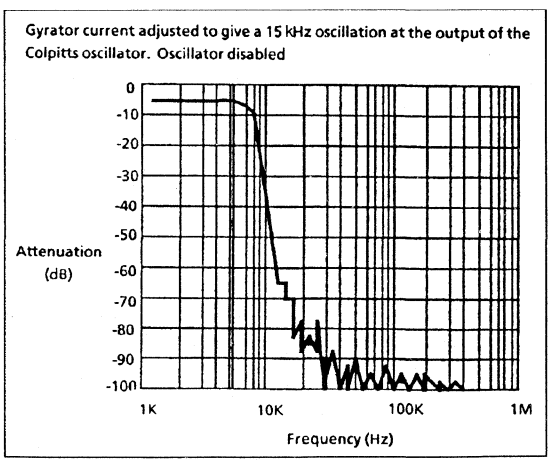


Figure 5: Channel Filter Response

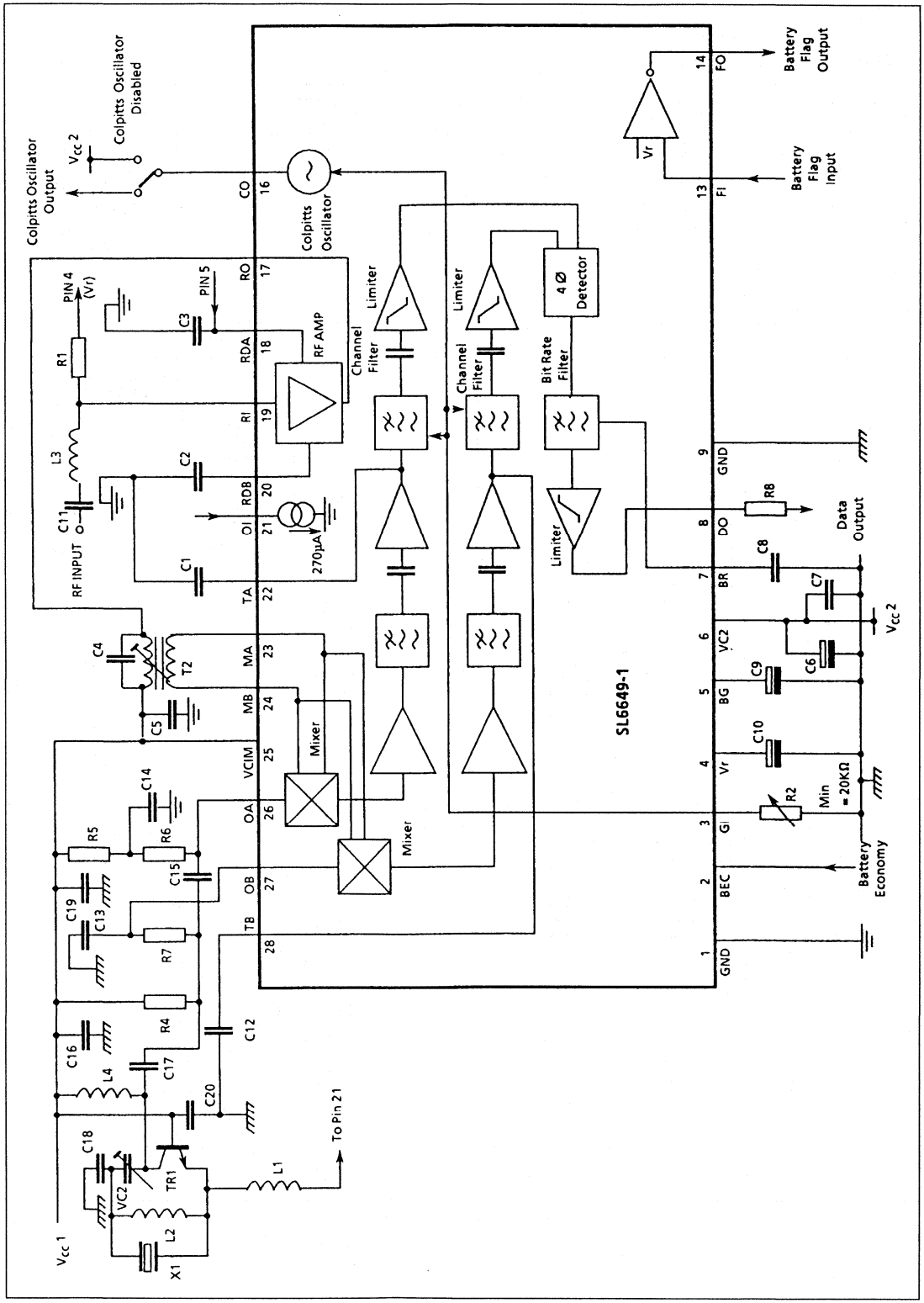


Figure 6: Block Diagram and Applications Circuit (for component values see next page)

COMPONENTS LIST FOR FIGURE 6

Capacitors				Resistors		Inductors		Transformers		Miscellaneous	
C1	1nF	C11	1nF	R1	2.2kΩ	L1	10µH	T1	1:1 Transformer Primary/Secondary Inductance=200nH	IC1	SL6649-1
C2	1nF	C12	1nF	R2	500kΩ Variable	L2	220nH			TR1	SOT-23 Transistor with $f\tau \geq 1.3$GHz (EG. ZETEX BFS 17)
C3	1nF	C13	10pF	R4	100Ω	L3	150nH			X1	153MHz 7th overtone crystal
C4	5.6pF	C14	1nF	R5	100Ω	L4	100nH			VC2	1.5-10pF
C5	1nF	C15	10pF	R6	100Ω						
C6	2.2µF	C16	1nF	R7	100Ω						
C7	1nF	C17	5.6pF	R8	100KΩ						
C8	1nF	C18	4.7pF								
C9	2.2µF	C19	1nF								
C10	2.2µF	C20	1nF								

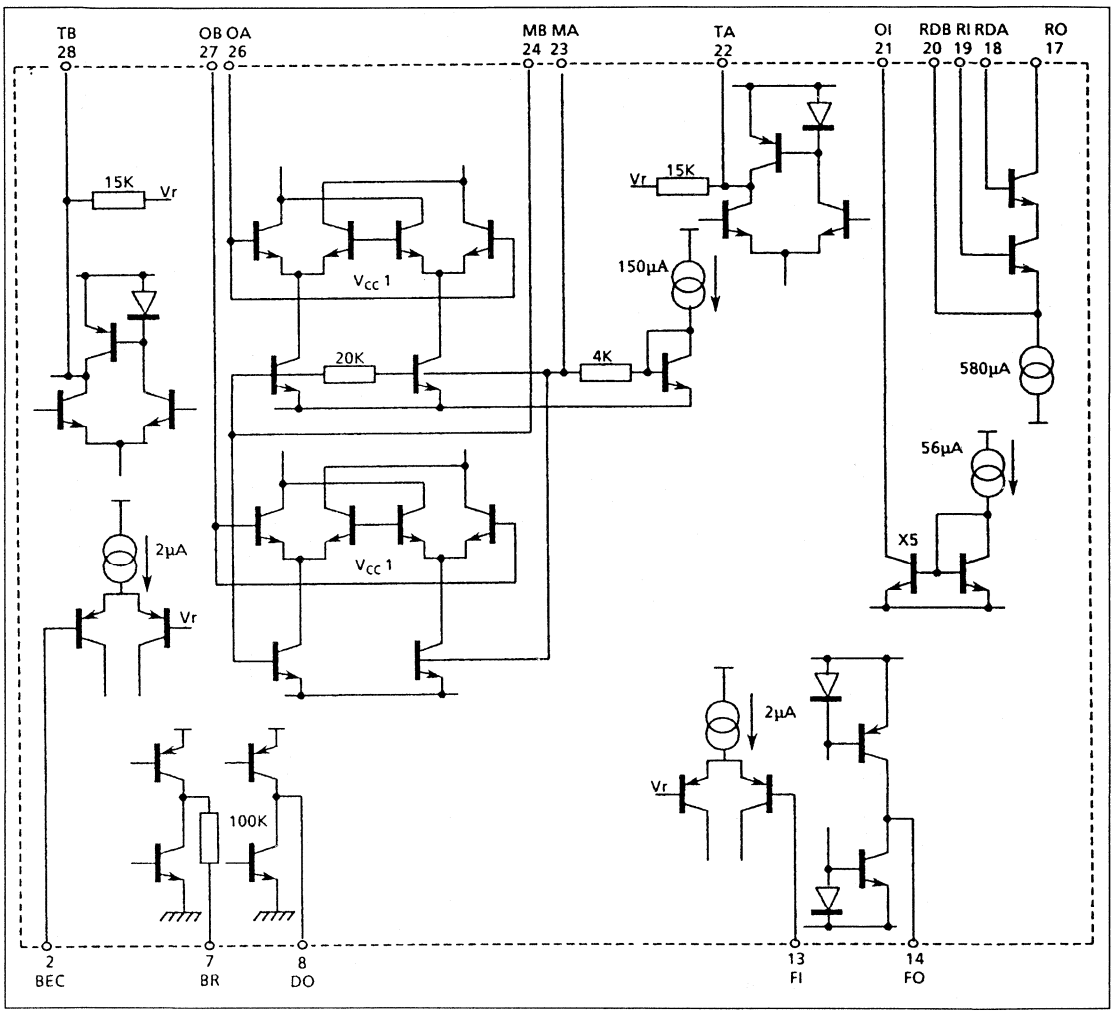
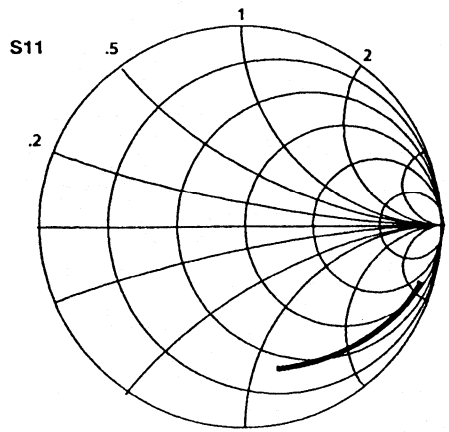
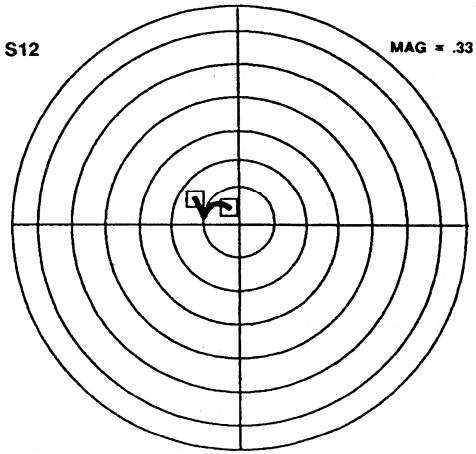
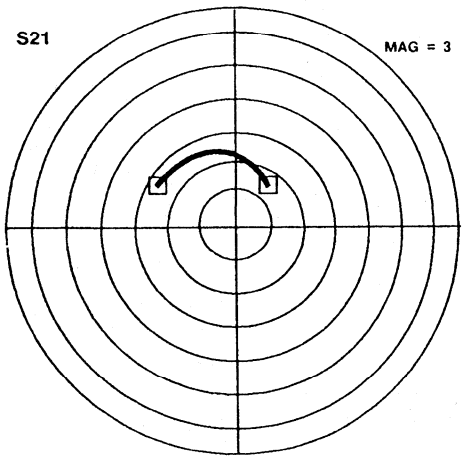
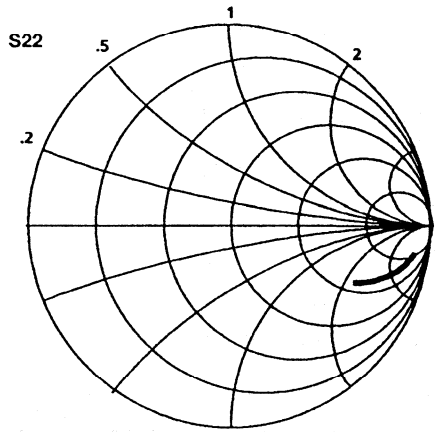


Figure 7: Pinning Diagram of the SL6649-1









FREQ	S11		S12		S22		S21	
MHz	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.
100.000	0.963	-15.971	0.016	120.281	1.036	-3.440	1.460	157.948
150.000	0.949	-21.603	0.017	121.732	0.991	-5.524	1.390	142.732
200.000	0.934	-27.247	0.017	123.174	0.946	-7.608	1.321	127.508
250.000	0.906	-33.835	0.021	124.612	0.938	-10.156	1.261	115.531
300.000	0.876	-40.519	0.025	126.042	0.934	-12.744	1.201	103.830
350.000	0.846	-45.789	0.029	139.335	0.925	-14.380	1.132	95.446
400.000	0.816	-50.979	0.032	153.381	0.915	-15.955	1.061	87.270
450.000	0.781	-58.616	0.039	163.051	0.872	-18.015	0.986	78.111
500.000	0.746	-66.363	0.045	172.537	0.827	-20.094	0.910	68.910
550.000	0.700	-72.624	0.062	165.197	0.771	-19.691	0.854	65.157
600.000	0.655	-78.856	0.079	157.518	0.716	-19.231	0.798	61.518

Figure 8: RF Amplifier

☐ S11

FREQ.	MAG.	ANG.
100.000	0.943	-14.921
150.000	0.929	-21.059
200.000	0.914	-27.208
250.000	0.904	-35.234
300.000	0.895	-43.439
350.000	0.866	-52.138
400.000	0.836	-60.882
450.000	0.796	-68.177
500.000	0.756	-75.417
550.000	0.726	-82.654
600.000	0.696	-89.883

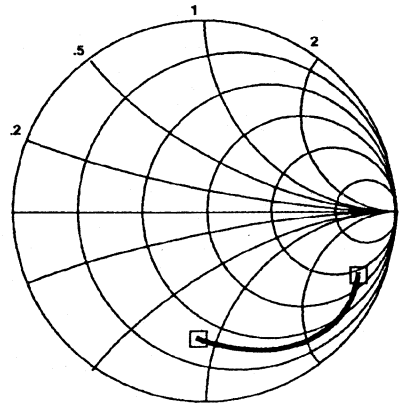


Figure 9a: SL6649-1 Mixer RF input pin 23

☐ S11

FREQ.	MAG.	ANG.
100.000	0.963	-10.019
150.000	0.953	-15.143
200.000	0.944	-20.277
250.000	0.930	-20.764
300.000	0.915	-20.853
350.000	0.891	-30.479
400.000	0.866	-40.734
450.000	0.846	-46.135
500.000	0.826	-51.344
550.000	0.806	-57.057
600.000	0.786	-62.785

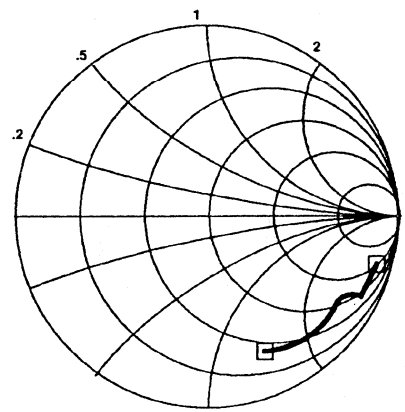


Figure 9b: SL6649-1 Mixer RF input pin 24

☐ S11

FREQ.	MAG.	ANG.
100.000	0.993	-11.020
150.000	0.983	-16.144
200.000	0.974	-21.277
250.000	0.960	-27.820
300.000	0.945	-34.499
350.000	0.954	-39.765
400.000	0.946	-44.952
450.000	0.927	-52.586
500.000	0.907	-60.331
550.000	0.877	-67.086
600.000	0.847	-73.819

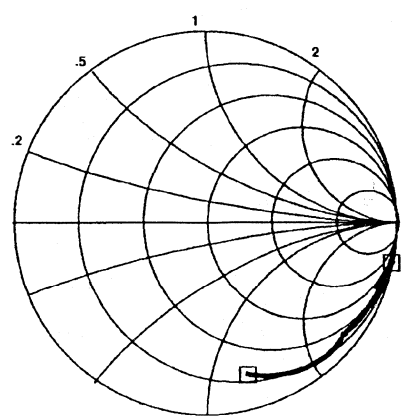


Figure 10: SL6649-1 Mixer LO input pins 26 and 27

METHOD FOR THE MEASUREMENT OF SENSITIVITY ON THE SL6649-1 RECEIVER

The method used by GEC Plessey Semiconductors in the measurement of terminal sensitivity is essentially the same as that described in the CEPT Res 2 Specification.

This method requires the following equipment:

1. A signal generator e.g. HP8640
2. A pocsag encoder
3. A pocsag decoder e.g. MV6639
4. An SL6649-1 Demo Board.
5. An interference free low impedance P.S.U. ($V_{CC}1$ and $V_{CC}2$ must be separate supplies and there must be at least 0.7V difference between them). Recommended supply configurations are shown in Fig. 13.

The test equipment and D.U.T. are set up as shown in Figure 11.

The R.F. frequency is set to the nominal L.O. frequency of the receiver and the peak deviation is set to 4.5kHz.

Care must be taken to avoid long power supply leads and any ground loops. Any interference from the decoder will be reduced by the insertion of a high value resistor R1 (100KΩ) between the receiver data output and the decoder input.

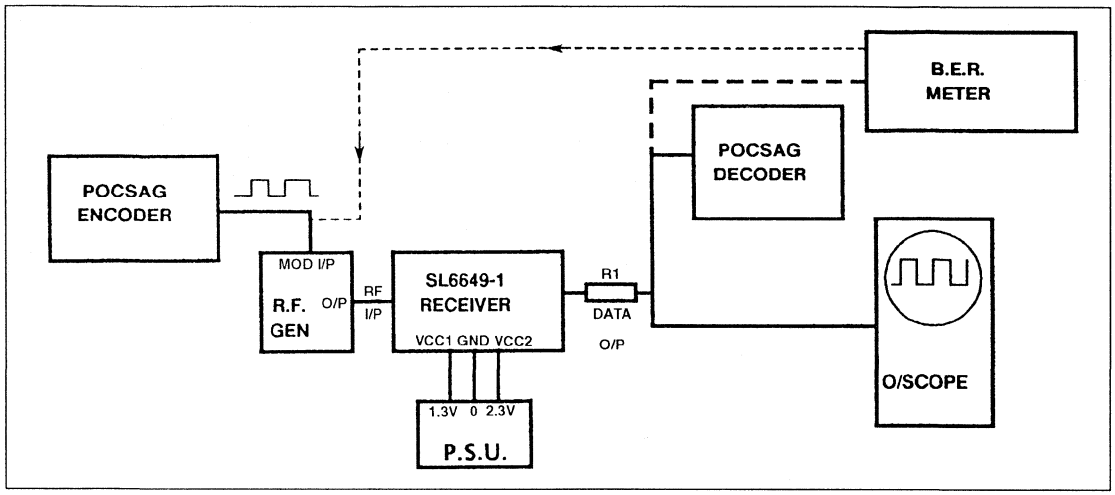


Figure 11: Test System

The generator output level is reduced successively until the decoder responds just 4 out of 5 times to the encoder signal. This output level is then recorded as the sensitivity threshold of the receiver.

We find that this threshold correlates to a bit error rate of 1 in 30. The data output waveforms for an input level which produces a B.E.R. of 1 in 30 and for input levels 2dB above and below this level, are shown below (square wave input). It can be seen that the edge jitter increases dramatically at signal levels below the sensitivity threshold of -127dBm. Typical waveforms that can be seen on an oscilloscope around the sensitivity threshold level are shown in Figure 12.

NB. In performing the sensitivity measurement great care should be taken in preventing coupling between test leads.

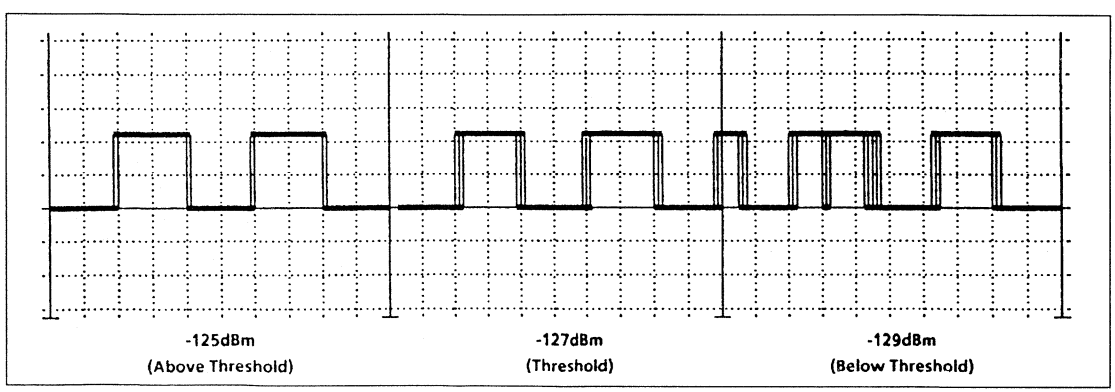


Figure 12: Waveform at Data O/P

PIN	MNEMONIC	FUNCTION
1	GND	Ground
2	BEC	Battery Economy
3	GI	Gyrator Current Adjust
4	Vr	Reference Voltage
5	BG	Bandgap Reference Voltage
6	Vc2	V_{CC} 2
7	BR	Bit rate Filter
8	DO	Data Output
9	GND	Ground
10		UNC
11		UNC
12		UNC
13	FI	Battery Flag Input
14	FO	Battery Flag Output

PIN	MNEMONIC	FUNCTION
15		UNC
16	CO	Colpitts Oscillator Output/Disable
17	RO	RFA I (collector) RF Output
18	RDA	RFA I (base) RF Decouple
19	RI	RFA II (base) RF Input
20	RDB	RFA II (emitter) RF Decouple
21	OI	LO Current Source
22	TA	Channel A Test
23	MA	Mixer I/P B
24	MB	Mixer I/P A
25	VCIM	V_{CC}1 (mixer)
26	OA	LO Input Channel A
27	OB	LO Input Channel B
28	TB	Channel B Test

POWER SUPPLIES

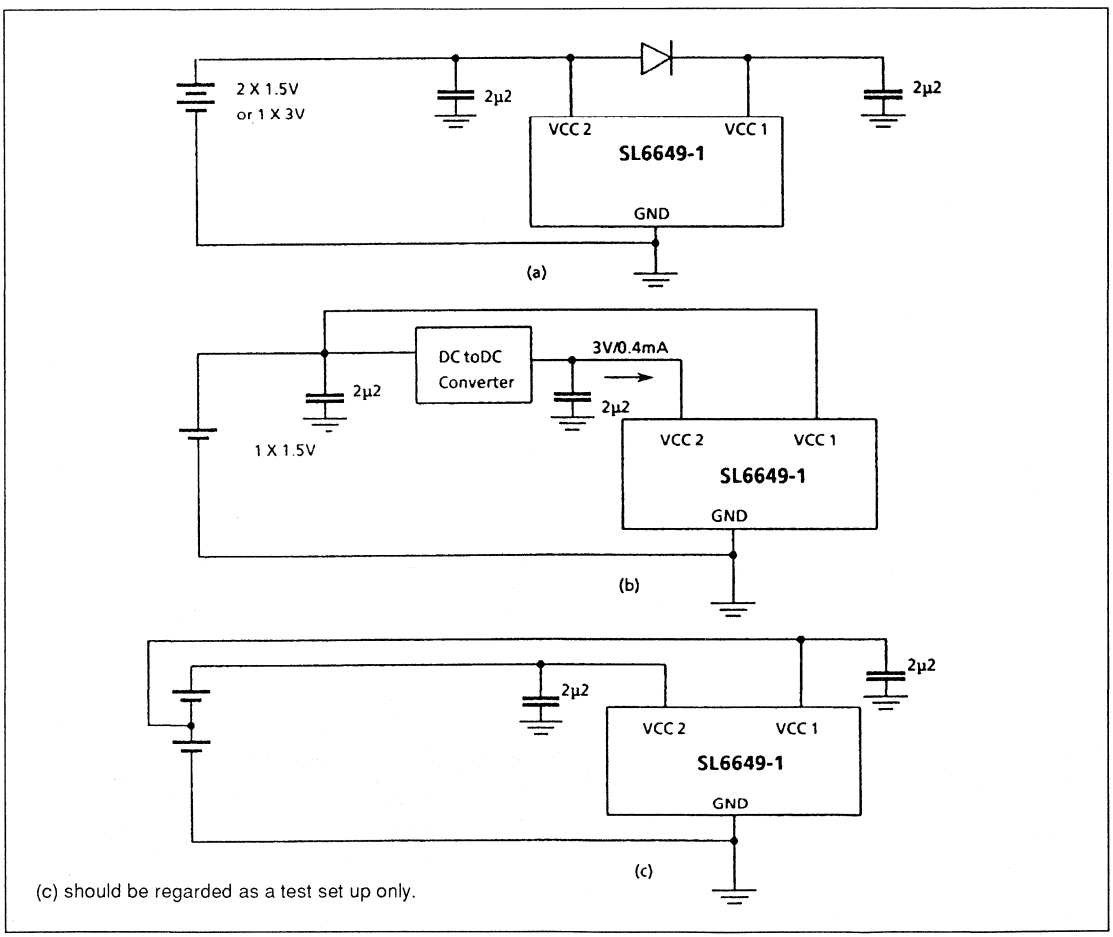


Figure 13(a): SL6649-1 Power Supply Options

PAGER APPLICATION EXAMPLE

A typical 1 volt pager system suitable as a wrist watch application is shown in Figure 13 (b). Only 3 integrated circuits are required to perform all the functions of a tone only pager. These are SL6649-1 direct conversion radio receiver and the MV6639 POCSAG decoder plus a 1 volt E²PROM (eg. Seiko Epson SPM28C51).

The SL6649-1 receives and demodulates the data, and monitors the battery voltage. The interface between the decoder and receiver consists of only 3 connections excluding the supplies.

The MV6639 performs all the functions required for a POCSAG decoder for tone only and/or pager messaging at 512 or 1200 baud. A 32kHz watch crystal is used as the reference frequency for the decoder.

The decoder voltage doubler output $V_{CC}2$ is available to power not only the receiver, but an alternative higher voltage E²PROM and microprocessor/LCD driver for a full tone and message pager.

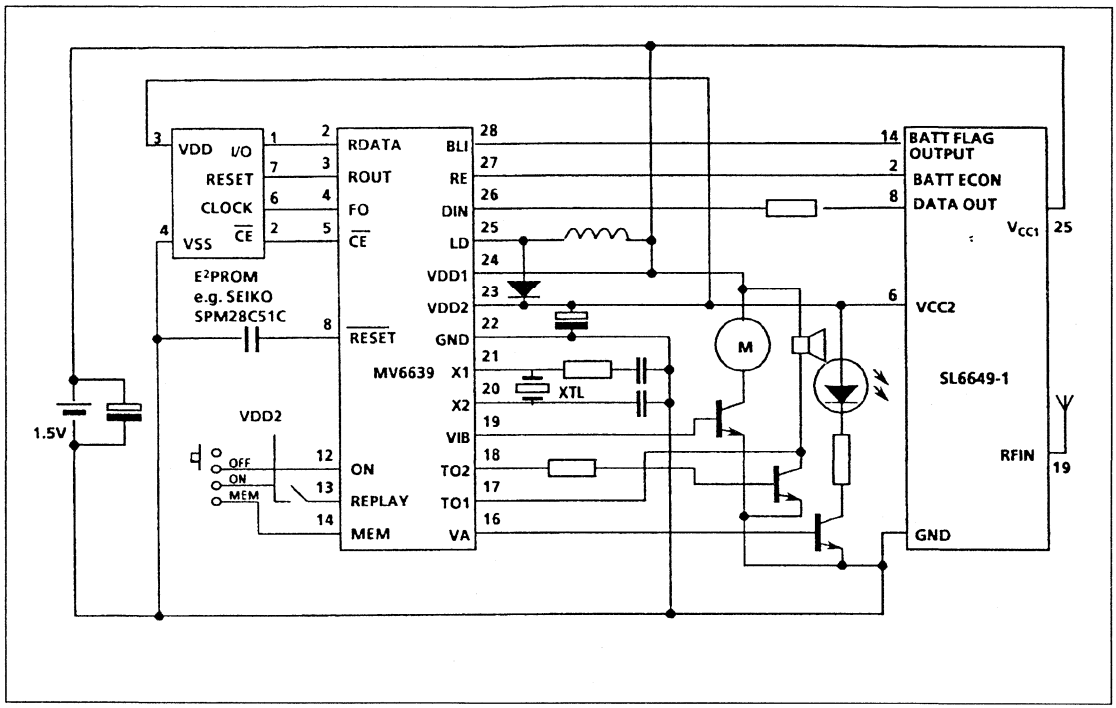


Figure 13(b): Tone Pager Applications Example Showing Interface with SL6649-1 Receiver

OPERATION AT OTHER FREQUENCIES AND DATA RATES

The values given in the components list for figure 6 are appropriate for frequencies nominally around 153MHz. In order to use the receiver at other frequencies it is necessary to change the capacitor C4 which is resonant with the transformer T1, and L2 and L4 in the oscillator circuit.

It is also necessary to change the values of capacitors C13 and C15 such that the reactance of these is equal to 100Ω at the required frequency.

It is of course necessary to use a crystal of the required frequency and stability. In order to use the receiver at higher data rates it is only necessary to reduce the value of C8, for example, at 1200bps, C8=470pf.

A demonstration board has been designed specifically to demonstrate terminal sensitivity. It is possible to connect an antenna to the board with suitable matching but no guarantee can be given regarding field strength sensitivity. However, with a suitably designed combination of PCB and antenna, a sensitivity of 5μV/M should be attainable.

Section 4

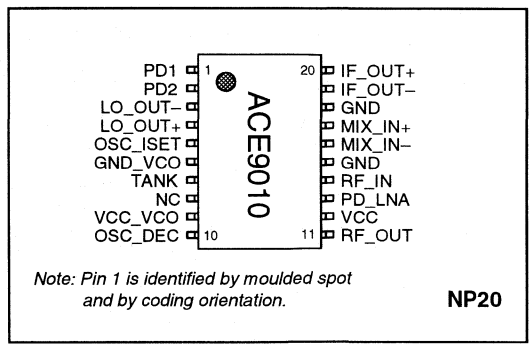
Analog Cellular Components

ACE9010

R.F. FRONT END WITH VCO

ACE9010 is a combined LNA, Mixer and VCO for use in the receive path of cellular telephones. High frequency front end functions previously realised in discrete components are integrated into one device. The design is optimised for low power whilst retaining high intercept performance and low noise operation.

Power saving modes are included for battery economy.



Note: Pin 1 is identified by moulded spot and by coding orientation.

NP20

Fig.1 Pin connections - top view

FEATURES

- Low Power and Low Voltage (3·6 to 5·0 V) Operation
- Power Down Modes
- Low Noise Figure - LNA 1.6 dB typical
- 1GHz VCO, Buffer, and Mixer
- Part of the ACE Integrated Cellular Phone Chipset
- Small Outline 20 pin SSOP Package

APPLICATIONS

- AMPS and TACS Cellular Telephones
- GSM and IS54 Digital Cellular Telephones
- Radio Systems

ORDERING INFORMATION

SSOP 20 lead package, code NP20

ACE9010/KG/NP1S - devices shipped in tubes

ACE9010/KG/NP1T - devices shipped on tape

RELATED PRODUCTS

ACE9010 is part of the following chipset:

- ACE9020 Receiver and Transmitter interface
- ACE9030 Radio Interface and Twin Synthesiser
- ACE9040 Audio Processor
- ACE9050 System Controller and Data Modem

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6 V
Storage temperature	- 65 °C to + 150 °C
Operating temperature	- 30 °C to + 85 °C
Voltage at any pin	- 0.3 V to V_{cc} + 0.3 V

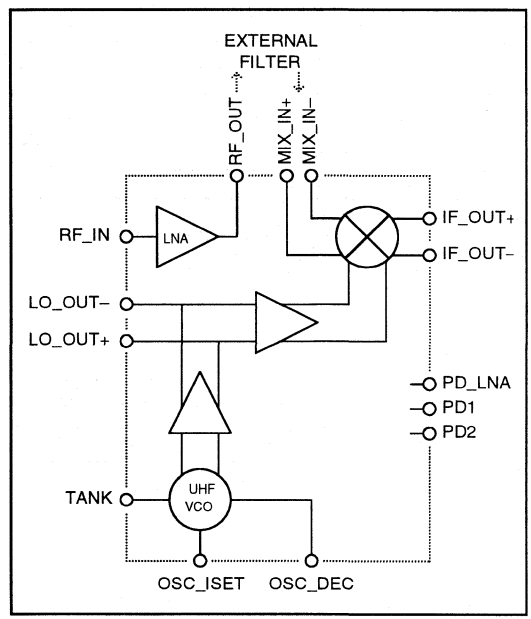


Fig. 2 ACE9010 simplified block digram

PIN CONNECTIONS

Pin No.	Name	Type	Description
1	PD1	I	Power down control input 1
2	PD2	I	Power down control input 2
3	LO_OUT–	I(O)	VCO differential buffer output (LO1 mixer input with VCO powered down)
4	LO_OUT+	I(O)	VCO differential buffer output (LO1 mixer input with VCO powered down)
5	OSC_ISET	I	VCO current set, oscillator emitter, typ. 220 Ω in series with 47 nH to GND
6	GND_VCO	I	VCO ground
7	TANK	I	Oscillator external resonator & varactor circuit connection
8	nc	-	No connection
9	VCC_VCO	Supply	VCO V_{CC} supply (leave open to power VCO down)
10	OSC_DEC	-	VCO decoupling, typ. 12 nF to GND_VCO
11	RF_OUT	O	LNA RF open collector output.
12	VCC	Supply	V_{CC} supply for LNA and mixer
13	PD_LNA	I	LNA power down
14	RF_IN	I	LNA input
15	GND	Supply	Ground
16	MIX_IN–	I	Differential mixer input (with pin 17)
17	MIX_IN+	I	Differential mixer input (with pin 16)
18	GND	Supply	Ground
19	IF_OUT–	O	Mixer I.F. differential output (with pin 20)
20	IF_OUT+	O	Mixer I.F. differential output (with pin 19)

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 30 °C to + 85 °C, V_{CC} = 3·75 ± 0·15 V or 4·85 ± 0·15 V, f_{RF} = 869 to 950 MHz, f_{LO} = 914 to 995 MHz, IF = 45 MHz, Interstage filter loss = 3 dB.

Parameter	Min.	Typ.	Max.	Unit	Conditions
LNA and MIXER					
Supply current			11	mA	
Conversion power gain	17			dB	See note 1
Noise Figure - LNA only		1.6	2.3	dB	
Noise Figure - Total		3.5	4	dB	See note 1
1 dB input compression	–18			dBm	See note 2
VCO					
Supply current		9	12	mA	
Output level		– 5		dBm	
Phase noise, Δf = 25 kHz			– 109	dBc/Hz	
Phase noise, Δf = 45 MHz			– 155	dBc/Hz	

Notes:
1. Includes LNA and Mixer plus interstage filter with 3 dB loss
2. Jamming signal at 45 MHz below f_{RF}

VCO OPTIONS

In normal operation the VCO will internally drive the mixer and also drive the outputs LO_OUT– and LO_OUT+ to provide the local oscillator signal to the ACE9020 prescaler and upconverter. It is possible to use an external VCO if preferred, by disconnecting VCC_VCO (pin 9) to power down the VCO and to then drive in on pins LO_OUT– and LO_OUT+.

Power Down Modes

PD2	PD1	PD_LNA	Mode
0	0	x	Sleep
0	1	1	VCO powered on
1	x	1	Receive -All circuitry on
1	x	0	LNA powered off

ACE9020

RECEIVER AND TRANSMITTER INTERFACE

ACE9020 is a VHF oscillator, up-converter and prescaler. It is used in a radio architecture where a UHF synthesiser makes the channel selection and a second synthesiser generates a fixed transmit offset.

A VCO signal from ACE9010 at UHF drives a buffer in ACE9020 to feed an on-chip prescaler and transmit up-converter. The prescaler is a dual two-modulus divider and drives the main synthesiser input of the ACE9030. The SSB up-converter suppresses the unwanted transmit sideband.

The VHF oscillator is buffered to drive the auxiliary synthesiser input of the ACE9030 and is locked to the offset frequency. This frequency is modulated by varying the resonant frequency of the external tank circuit. Both this oscillator and the UHF VCO drive the up-converting mixer to generate the transmit signal.

Various power saving modes for battery economy are included. These allow the transmit sections to be shut down during stand-by and the whole chip can be shut down during sleep mode. The circuit techniques used have been chosen to minimise external components and at the same time give very high performance.

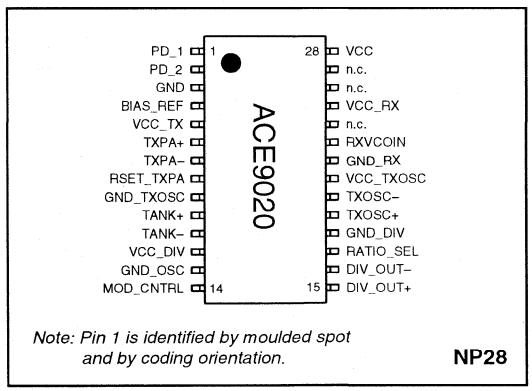


Fig.1 Pin connections - top view

FEATURES

- Low Power Low Voltage (3·6 to 5·0 V) Operation
- Power Down Modes
- Differential Signals to Minimise Cross-talk
- Auxiliary Oscillator with Transmit Up-converter
- Prescaler for Main Synthesiser
- Part of the ACE Integrated Cellular Phone Chipset
- Small Outline 28 pin Package

APPLICATIONS

- AMPS and TACS Cellular Telephone
- Two-Way Radio Systems

RELATED PRODUCTS

ACE9020 is part of the following chipset:

- ACE9010 R.F. Front End with VCO
- ACE9030 Radio Interface and Twin Synthesiser
- ACE9040 Audio Processor
- ACE9050 System Controller and Data Modem

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6 V
Storage temperature	- 65 °C to + 150 °C
Operating temperature	- 30 °C to + 85 °C
Voltage at any pin	- 0.3 V to V_{CC} + 0.3 V

ORDERING INFORMATION

SSOP 28 lead package, code NP28

ACE9020/KG/NP1S - devices shipped in tubes

ACE9020/KG/NP1T - devices shipped on tape

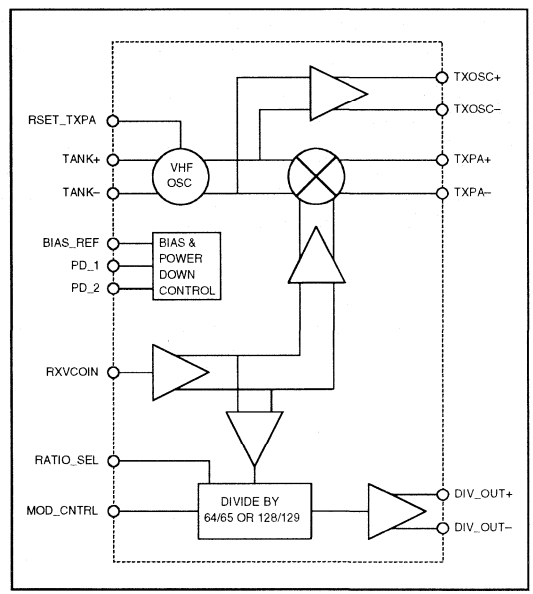


Fig. 2 ACE9020 simplified block digram

PIN CONNECTIONS

Pin No.	Name	Type	Description
1	PD_1	I	Power down control input 1
2	PD_2	I	Power down control input 2
3	GND	Supply	Ground
4	BIAS_REF	I	Reference current for bias control
5	VCC_TX	Supply	Transmit section supply voltage
6	TXPA+	O	Transmit up-converter open collector output
7	TXPA-	O	Transmit up-converter open collector output
8	RSET_TXPA	I	Reference current for transmit power amplifier output
9	GND_TXOSC	Supply	Ground
10	TANK+	I	Transmit oscillator tank circuit
11	TANK-	I	Transmit oscillator tank circuit
12	VCC_DIV	Supply	Divider section supply voltage
13	GND_OSC	Supply	Ground
14	MOD_CNTRL	I	Modulus control input
15	DIV_OUT+	O	Divider output positive
16	DIV_OUT-	O	Divider output negative
17	RATIO_SEL	I	Ratio select
18	GND_DIV	Supply	Ground divider section
19	TXOSC+	O	Transmit oscillator monitor output positive
20	TXOSC-	O	Transmit oscillator monitor output negative
21	VCC_TXOSC	Supply	Transmit oscillator supply voltage
22	GND_RX	Supply	Ground
23	RXVCOIN	I	Input buffer for 1 GHz VCO signal from ACE9010
24	n.c.	-	No connection
25	VCC_RX	Supply	Receiver section supply voltage
26	n.c.	-	No connection
27	n.c.	-	No connection
28	VCC	Supply	ON/OFF logic supply voltage

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 30 °C to + 85 °C, V_{CC} = 3·75 ± 0·15 V or 4·85 ± 0·15 V

POWER SUPPLY CURRENT

Condition	PD_1	PD_2	Min	Typ	Max	Unit
Power Down	0	0		0·08	0·11	mA
Standby	0	1		6	8	mA
Transmit set up [1]	1	1		36	51	mA
Full Duplex	1	0		48	63	mA

Notes:

1. This interim state powers up the Auxiliary VCO before enabling the transmit output buffer.

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 30 °C to + 85 °C, V_{CC} = 3·75 ± 0·15 V or 4·85 ± 0·15 V

A.C.PARAMETERS

TXOSC OUTPUT SIGNAL

Parameter	Min	Typ	Max	Unit
Differential output level	500			mV p-p
TXOSC frequency	70	90 or 122·25	140	MHz
Sensitivity to supply		60		kHz/V
Spurii above 700 MHz			– 40	dBc
Tank inductor, for 90 MHz		100		nH
Tank inductor, for 122·25 MHz		68		nH
Tank circuit Q	40			
Power up time			25	µs

TXPA OUTPUT SIGNAL

Parameter	Min	Typ	Max	Unit
Power into 50 Ω	0	2	4	dBm
Noise at f_{TX} ± 45 MHz			– 145	dBc/Hz
Noise at f_{TX} ± 25 kHz			– 100	dBc/Hz
Harmonic contents			– 20	dBc
Spurious at $f_{RXVCO} + f_{AUX}$			– 10	dBc
Spurii at $f_{RXVCO} \pm 2f_{AUX}$			– 30	dBc
Spurii at $f_{RXVCO} \pm 3f_{AUX}$			– 25	dBc
Spurious contents within f_{TX} + 45 MHz ± 15 kHz except at $2f_{RXVCO} - 9f_{AUX}$			– 105	dBc
Spurious content at $2f_{RXVCO} - 9f_{AUX}$			– 60	dBc
Other spurii in band 800 to 940 MHz			– 70	dBc
Other spurii, except at $f_{RXVCO} + f_{AUX}$			– 30	dBc
Power up time			25	µs
Residual modulation			– 40	dB

RXVCOIN INPUT SIGNAL

Parameter	Min	Typ	Max	Unit
Signal power	– 7		0	dBm
Input impedance		100		Ω
Frequency to dividers	800		1100	MHz
Frequency to all else	910		1040	MHz
Noise at f_{RXVCO} ± 45 MHz			– 155	dBc
Noise at f_{RXVCO} ± 25 kHz			– 117	dBc

DIVIDER

Parameter	Min	Typ	Max	Unit
MOD_CNTRL HIGH level	$V_{CC}/2 + 0·3$		$V_{CC}/2 + 1·1$	V
MOD_CNTRL LOW level	$V_{CC}/2 - 1·1$		$V_{CC}/2 - 0·3$	V
DIV_OUT+, & –:				
Level	500	600		mV p-p
Edge time	10		15	ns
MOD_CNTRL:				
Set-up time	20			ns
Hold time			1	ns

DESCRIPTION

The primary purposes of the ACE9020 are to generate the transmit frequency by mixing the receiver local oscillator frequency with an auxiliary synthesiser, to add modulation to this transmit signal, and to provide a prescaler for the receiver synthesiser. In order to save battery power the various sections can be shut down when not in use.

The circuit operation can be explained with reference to the basic application diagram.

The transmit oscillator TXOSC drives the auxiliary synthesiser inputs on the ACE9030 and so is phase locked to the required offset frequency, f_{AUX}, equal to the sum of the channel duplex separation and the receiver first intermediate frequency. A typical application will use an auxiliary frequency of 90MHz. The modulation is added by varying this oscillator frequency by the use of a varactor diode in the tank circuit.

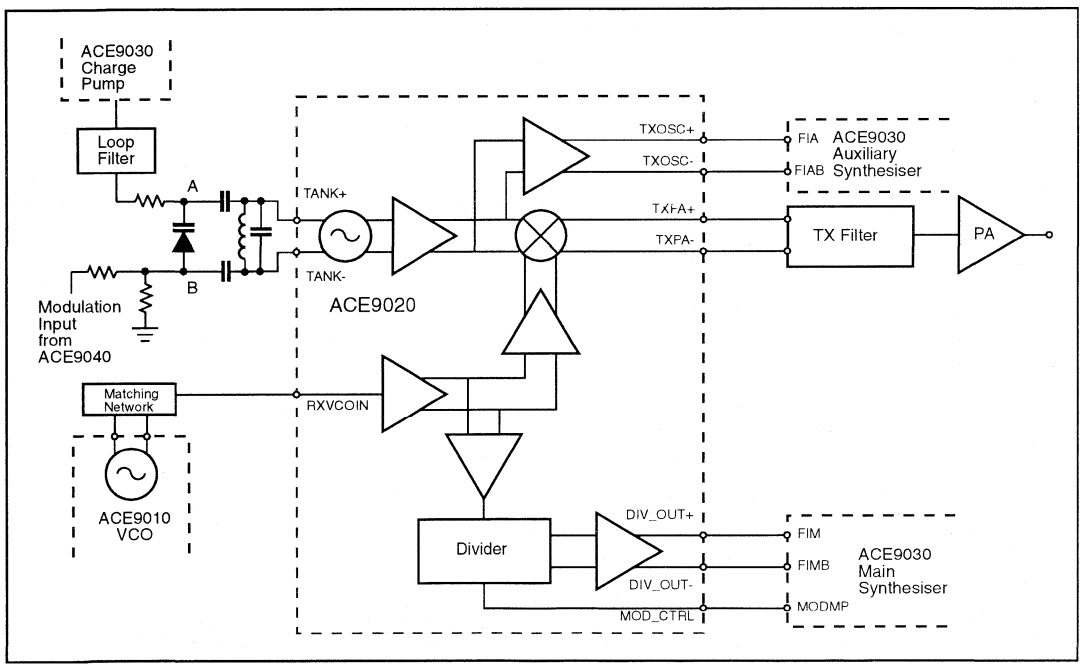
The receiver VCO in the ACE9010 drives the pin RXVCOIN, which is buffered to drive the transmitter mixer, a prescaler and the RX_LO output buffer. Separate buffering is used to ensure that prescaler noise does not affect the mixer. This prescaler drives the main synthesiser inputs on the ACE9030 to be phase locked to the required local oscillator frequency f_{RXVCO} for the channel to be received and is operated as a two modulus divider, controlled by MOD_CNTRL and with the pair of ratios selected by RATIO_SEL:

	RATIO_SEL @ LOW	RATIO_SEL @ HIGH
MOD_CNTRL = LOW	÷129	÷65
MOD_CNTRL = HIGH	÷128	÷64

The mixer generates the transmit frequency f_{TX} as the difference $f_{RXVCO} - f_{AUX}$ and is designed to give a low noise floor.

The power down inputs PD1,2 are controlled by digital outputs from ACE9030.

APPLICATION DIAGRAM



ACE9030

RADIO INTERFACE AND TWIN SYNTHESISER

ACE9030 is a combined radio interface circuit and twin synthesiser, intended for use in a cellular telephone.

The radio interface section contains circuits to monitor and control levels such as transmit power in the telephone, circuits to demodulate the frequency modulated signal to audio, and a crystal oscillator with a frequency multiplier.

The Main synthesiser has Normal and Fractional-N modes both with optional Speed-up to select the desired channel. The Auxiliary synthesiser is used for the transmit-receive offset and for modulation.

Both sections are controlled by a serial bus and have software selected power saving modes for battery economy. The circuit techniques used have been chosen to minimise external components and at the same time give very high performance.

FEATURES

- Low Power Low Voltage (3·6 to 5·0 V) Operation
- Serial Bus Controlled Power Down Modes
- Simple Programming Format
- Reference Crystal Oscillator
- Frequency Multiplier for LO2 Signal
- 8·064 MHz Output for External Microcontroller
- Main Synthesiser with Fractional-N Option
- Auxiliary Synthesiser
- Main Synthesiser Speed-up Options
- FM Discriminator for 450 kHz or 455 kHz I.F. Signal
- Radio System Monitor Inputs and Control Outputs
- Part of the ACE Integrated Cellular Phone Chipset
- TQFP 64 pin 0·4 mm and 0·5 mm Pitch Packages

RELATED PRODUCTS

ACE9030 is part of the following chipset:

- ACE9010 R.F. Front End with VCO
- ACE9020 Receiver and Transmitter Interface
- ACE9040 Audio Processor
- ACE9050 System Controller and Data Modem

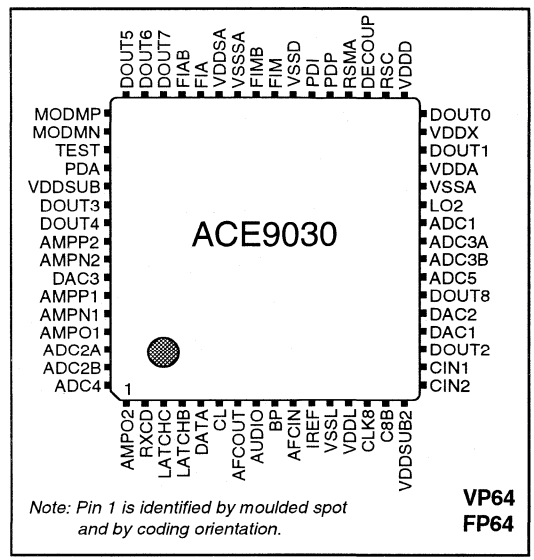


Fig.1 Pin connections - top view

APPLICATIONS

- AMPS and TACS Cellular Telephone
- Two-way Radio Systems

ORDERING INFORMATION

Industrial temperature range
TQFP 64 lead 10 x 10 mm, 0·5 mm pitch (FP64)
ACE9030/IG/FP1R - devices shipped in trays
ACE9030/PR/FP1R - pre-production
TQFP 64 lead 7 x 7 mm, 0·4 mm pitch (VP64)
ACE9030/IG/FP2R - devices shipped in trays
ACE9030/PR/FP2R - pre-production

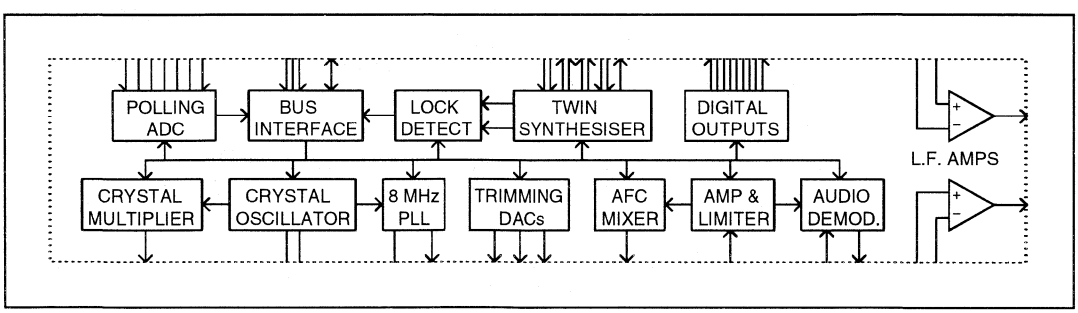


Fig. 2 ACE9030 Simplified Block Diagram

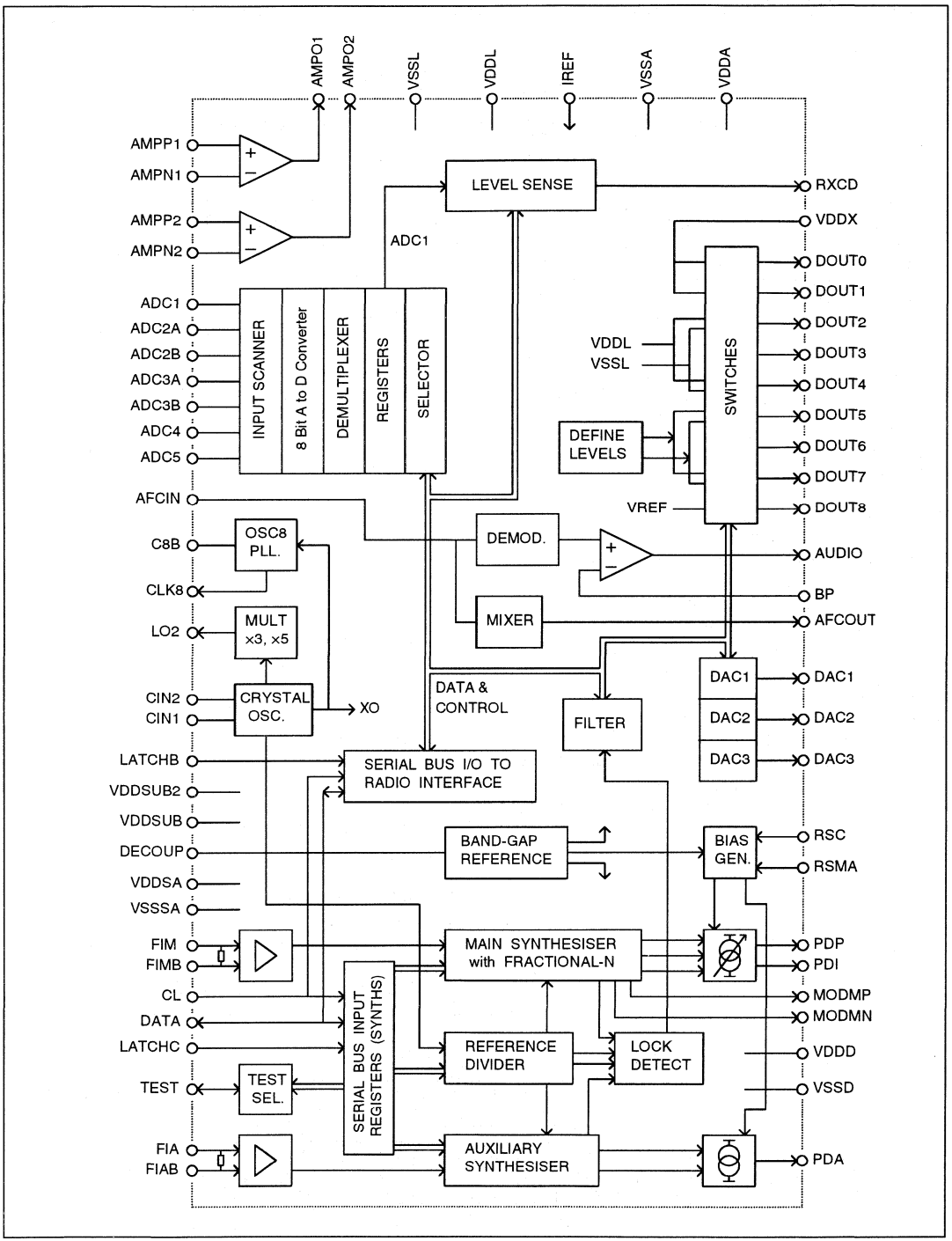


Fig.3 ACE9030 Block diagram

PIN DESCRIPTIONS

The relevant supplies (V_{DD}) and grounds (V_{SS}) for each circuit function are listed. The ESD protection diodes and clamps sometimes use different V_{DD}'s and V_{SS}'s. It is advised that all V_{DD}'s and all V_{SS}'s are always used.

Pin No.	Name	Description	VDD	VSS
1	AMPO2	LF amplifier 2 output.	VDDA	VSSA
2	RXCD	Receive carrier detect (ADC1 comparator) output.	VDDL	VSSL
3	LATCHC	Synthesiser programme enable input.	VDDL	VSSL
4	LATCHB	Radio interface programme enable input.	VDDL	VSSL
5	DATA	Serial data; programming input, results output.	VDDL	VSSL
6	CL	Clock input for programming bus and for I.F. sampling.	VDDL	VSSL
7	AFCOUT	Output from AFC amplifier after sampling.	VDDL	VSSL
8	AUDIO	Output from f.m. discriminator after filtering.	VDDA	VSSA
9	BP	Feedback input to audio bandpass filter.	VDDA	VSSA
10	AFCIN	Input to AFC amplifier and f.m. discriminator.	VDDL	VSSL
11	IREF	Bias current input for radio interface, connect setting resistor to ground.	–	VSSA
12	VSSL	Ground for radio interface logic.	–	–
13	VDDL	Power supply to radio interface logic.	–	–
14	CLK8	Output clock at 8·064 MHz, locked to crystal.	VDDL	VSSL
15	C8B	8·064 MHz oscillator charge pump output and control voltage input.	VDDA	VSSA
16	VDDSUB2	Second connection for clean positive supply to bias substrate.	VDDA	VSSA
17	CIN2	Connection for crystal oscillator.	VDDL	VSSL
18	CIN1	Connection for crystal oscillator.	VDDL	VSSL
19	DOUT2	Digital control output 2.	VDDL	VSSL
20	DAC1	Analog control output 1.	VDDA	VSSA
21	DAC2	Analog control output 2.	VDDA	VSSA
22	DOUT8	Digital control output 8.	VDDA	VSSA
23	ADC5	Analog to digital converter input 5.	VDDA	VSSA
24	ADC3B	Analog to digital converter input 3B.	VDDA	VSSA
25	ADC3A	Analog to digital converter input 3A.	VDDA	VSSA
26	ADC1	Analog to digital converter input 1.	VDDA	VSSA
27	LO2	Output from crystal frequency multiplier.	VDDA	VSSA
28	VSSA	Ground for radio interface analog parts.	–	–
29	VDDA	Power supply to radio interface analog parts.	–	–
30	DOUT1	Digital control output 1.	VDDX	–
31	VDDX	Power supply to DOUT1 and DOUT2 switches.	–	–
32	DOUT0	Digital control output 0.	VDDX	–
33	VDDD	Power supply to synthesisers, except input buffers and the bandgap.	–	–
34	RSC	Fractional-N compensation bias current, resistor to ground.	–	VSSSA
35	DECOUP	Bandgap reference decoupling capacitor connection.	VDDSA	VSSSA
36	RSMA	Bias current for synthesiser charge pumps, resistor to ground.	–	VSSSA
37	PDP	Main synthesiser proportional charge pump output.	VDDD	VSSD
38	PDI	Main synthesiser integral charge pump output.	VDDD	VSSD
39	VSSD	Ground for synthesisers, except input buffers and the bandgap.	–	–
40	FIM	Main synthesiser positive input from prescaler.	VDDSA	VSSSA
41	FIMB	Main synthesiser negative input from prescaler.	VDDSA	VSSSA
42	VSSSA	Ground for FIM and FIA input buffers and the bandgap.	–	–
43	VDDSA	Power for FIM and FIA input buffers and the bandgap.	–	–
44	FIA	Auxiliary synthesiser positive input from VCO.	VDDSA	VSSSA
45	FIAB	Auxiliary synthesiser negative input from VCO.	VDDSA	VSSSA
46	DOUT7	Digital control output 7.	VDDD	VSSD
47	DOUT6	Digital control output 6.	VDDD	VSSD
48	DOUT5	Digital control output 5.	VDDD	VSSD
49	MODMP	Modulus control output to prescaler - positive sense.	VDDD	VSSD
50	MODMN	Modulus control output to prescaler - negative sense.	VDDD	VSSD
51	TEST	Test input and output for synthesisers.	VDDD	VSSD
52	PDA	Auxiliary synthesiser charge pump output.	VDDD	VSSD
53	VDDSUB	Clean positive supply to bias substrate.	–	–
54	DOUT3	Digital control output 3.	VDDL	VSSL
55	DOUT4	Digital control output 4.	VDDL	VSSL
56	AMPP2	LF amplifier 2 positive input.	VDDA	VSSA
57	AMPN2	LF amplifier 2 negative input.	VDDA	VSSA
58	DAC3	Analog control output 3.	VDDL	VSSL
59	AMPP1	LF amplifier 1 positive input.	VDDA	VSSA
60	AMPN1	LF amplifier 1 negative input.	VDDA	VSSA
61	AMPO1	LF amplifier 1 output.	VDDA	VSSA
62	ADC2A	Analog to digital converter input 2A.	VDDA	VSSA
63	ADC2B	Analog to digital converter input 2B.	VDDA	VSSA
64	ADC4	Analog to digital converter input 4.	VDDA	VSSA

ABSOLUTE MAXIMUM RATINGS

Supply voltage from ground (any V_{DD} to any V_{SS})	−0·3 V to +6·0 V
Supply voltage difference (any V_{DD} to any other V_{DD})	−0·3 V to +0·3 V
Input voltage (any input pin to its local V_{SS} and V_{DD})	V_{SS} −0·3 V to V_{DD} +0·3 V
Output voltage (any output pin to its local V_{SS} and V_{DD})	V_{SS} −0·3 V to V_{DD} +0·3 V
Storage temperature	−55 °C to +150 °C
Operating temperature	−40 °C to +85 °C

These are not the operating conditions, but are the absolute limits which if exceeded even momentarily may cause permanent damage. To ensure sustained correct operation the device should be used within the limits given under Electrical Characteristics.

To avoid any possibility of latch-up the substrate connections V_{DDSUB} and V_{DDSUB2} must be the most positive of all V_{DD}'s at all times including during power on and off ramping. As the current taken through these V_{DD}'s is significantly less than through the other V_{DD}'s this requirement can be easily met by directly connecting all V_{DD} pins to a common point on the circuit board but with the decoupling capacitors distributed to minimise cross-talk caused by common mode currents. If low value series resistors are to be included in the V_{DD} connections, with decoupling capacitors by the ACE9030 pins to further reduce interference, the V_{DDSUB} and V_{DDSUB2} pins should not have such a resistor in order to guarantee that their voltage is not slowed down at power-on. Power switches to DOUT0 and DOUT1 are supplied from V_{DDX} and are specified for a total current of up to 40 mA so any resistor in the V_{DDX} connection must be very low, around 1Ω, in order to avoid excessive voltage drop; it is recommended that this supply has no series resistor. These two methods are shown in circuit diagrams, figures 4 and 5. In both circuits the main V_{DD} must also have good decoupling.

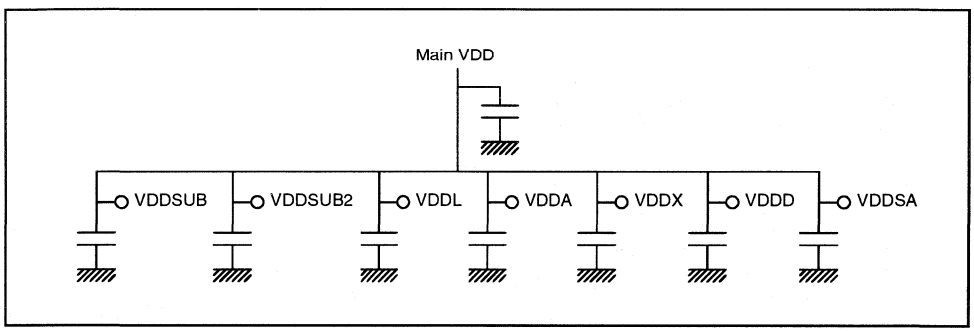


Fig.4 Typical VDD local decoupling networks without series resistors

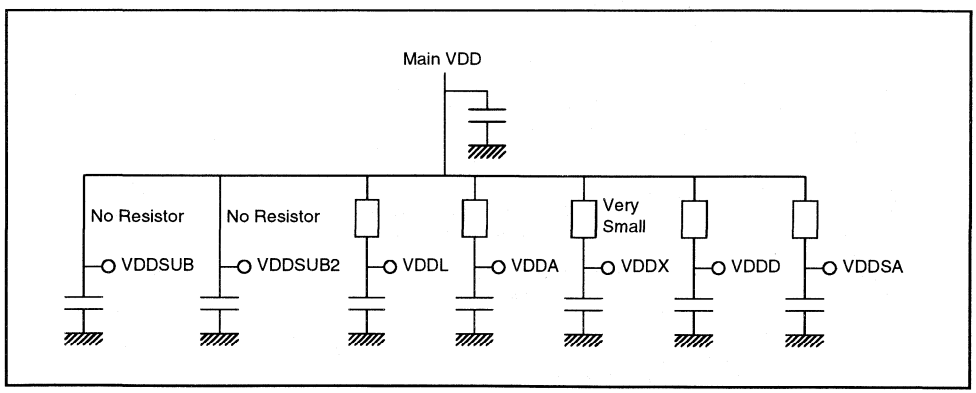


Fig.5 Typical VDD local decoupling networks with series resistors

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 40 °C to + 85 °C, all V_{DD} = + 3·6 to + 5·0 V, GND ref. = V_{SS}, any V_{DD} to any other V_{DD} = – 0·1 to + 0·1 V

D.C. Characteristics

Parameter	Min.	Typ.	Max.	Unit	Conditions
Power supply					
Supply current, Radio Interface: I_{DDA} + I_{DDL}					
Sleep mode			2·5	mA	XO, OSC8 on
Fully operating (excluding I_{DDX})			7	mA	(see Note 1)
Supply current, Synthesisers: I_{DDD} + I_{DDSA} + I_{DDSUB}					f_{REF} = 15 MHz
Main and Auxiliary ON		3		mA	f_{MAIN} = 16 MHz
Main ON and Auxiliary in Standby		2		mA	f_{AUX} = 90 MHz
Main in Standby and Auxiliary ON		2		mA	(see Note 2)
Main and Auxiliary in Standby, with Bandgap off.		10		µA	
Input and output signals					
Logic input HIGH (LATCHC, LATCHB, DATA, CL, and TEST)	0·7 x V_{DD}		V_{DD} + 0·3	V	
Logic input LOW (LATCHC, LATCHB, DATA, CL, and TEST)	– 0·3		+ 0·8	V	
Input capacitance (signal pins)			10	pF	Pin voltage
Input leakage (signal pins)			1	µA	V_{SS} to V_{DD}
Logic output HIGH (RXCD, DATA, AFCOUT, TEST and DOUT2, 3 and 4)	V_{DD} – 0·5			V	External load: 20 kΩ & 30 pF
Logic output LOW (RXCD, DATA, AFCOUT, TEST and DOUT2, 3 and 4)			0·4	V	
Output ON level, DOUT0 and DOUT1	V_{DDX} – 0·2			V	I_{OH} = 20 mA.
Output HIGH level, DOUT5, 6 and 7	2·3		2·9	V	I_{OH} = 80 µA
Output LOW level, DOUT5, 6 and 7			0·3	V	I_{OL} = ± 10 µA
Trimmed output level ON, DOUT8	3·35		3·55	V	I_{OH} = 20 to 400 µA.
Level difference, DOUT8 ON – ADC reference	– 10		+ 10	mV	
Output level OFF, DOUT8			TBD	-	
MODMP, MODMN output HIGH	V_{DD}/2 + 0·35		V_{DD}/2 + 1·0	V	I_{OH} = 10 µA
MODMP, MODMN output LOW	V_{DD}/2 – 1·0		V_{DD}/2 – 0·35	V	I_{OL} = – 10 µA
Input Schmitt Hysteresis, pins CL, LATCHB, LATCHC, DATA.	0·4			V	
Analog circuits bias resistor on I_{REF}		68		kΩ	V_{DD} @ 3·75 V
		100		kΩ	V_{DD} @ 4·85 V

Notes

1. The sleep current is specified with the crystal oscillator (XO) and the OSC8 oscillator and PLL running as these are normally needed to provide the clock to the system controller. It is possible to switch off these two blocks by use of commands on the serial bus to reduce the sleep current to an even smaller value but the system must then provide a clock to the controller from some other source.

2. The terms f_{REF}, f_{MAIN}, and f_{AUX} refer to the frequencies of the Reference inputs (Crystal oscillator, pins CIN1 and CIN2), the Main synthesiser inputs (pins FIM and FIMB) and the Auxiliary synthesiser inputs (pins FIA and FIAB) respectively. The ON supply currents given apply when the loops are locked - during channel change the charge pump current is additional.

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 40 °C to + 85 °C, all V_{DD} = + 3·6 to + 5·0 V, GND ref. = V_{SS}, any V_{DD} to any other V_{DD} = – 0·1 to + 0·1 V

D.C. Characteristics (continued)

Parameter	Min.	Typ.	Max.	Unit	Conditions
Synthesiser charge pump current					
Current setting resistor R_{SMA}	19	39	78	kΩ	Note 3
Current setting resistor R_{SC}	19	39	78	kΩ	Note 3
External capacitance on pin R_{SMA}			5	pF	Ensures stable
External capacitance on pin R_{SC}			5	pF	bias current.
Bias current I_{RSMA} (nominally 1·25V / R_{SMA})	28·8	32	35·2	µA	R_{SMA} = 39 kΩ
Bias current I_{RSC} (nominally 1·25V / R_{SC})	28·8	32	35·2	µA	R_{SC} = 39 kΩ
Iprop(0) scaling accuracy, pin PDP	–10		+10	%	@ 200 µA. Note 4
Iprop(1) scaling accuracy, pin PDP	–10		+10	%	@ 800 µA. Note 4
Iint scaling accuracy, pin PDI	–10		+10	%	@ 4 mA. Note 4
Icomp(0) scaling accuracy, pin PDP	–10		+10	%	@ ACC × 0·2 µA Note 4
Icomp(1) scaling accuracy, pin PDP	–10		+10	%	@ ACC × 0·8 µA Note 4
Icomp(2) scaling accuracy, pin PDI	–10		+10	%	@ ACC × 4 µA Note 4
Iauxil scaling accuracy, pin PDA	–5		+5	%	@ 256 µA. Note 4
Auxiliary Charge Pump, Up or Down I_{AUX} current variation	–10		+10	%	Note 5
Main Charge Pumps, Up or Down I_{MAIN} or $I_{INTEGRAL}$ current variation	–10		+10	%	Note 6
Iprop(0) or Iprop(1) setting from PDP pin			1·0	mA	
Iint setting from PDI pin			5	mA	
Icomp(0) or Icomp(1) setting from PDP pin			12	µA	
Icomp(2) setting from PDI pin			180	µA	
Iauxil setting from PDA pin			512	µA	

Notes

3. The circuit is defined with resistors R_{SMA} and R_{SC} connected from pins RSMA and RSC to V_{SSSA} but in most practical applications all V_{SS} pins will be connected to a ground plane so R_{SMA} and R_{SC} should then also be connected to this ground plane.

4. The charge pump currents are specified to this accuracy when the relevant output pin is at a potential of $V_{DD}/2$ and with R_{SMA} = 39 kΩ, CN = 200, L= 1, K = 5, R_{SC} = 19 kΩ. The nominal value is set by external resistors and by programming registers, as defined in Table 6. Tolerances in the internal Bandgap voltage and bias circuits are within the limits given for I_{RSMA} and I_{RSC}, the scaling accuracy of the multiplying DAC's is within these limits given for Iprop(0), Iprop(1), Iint, Icomp(0), Icomp(1), Icomp(2), and auxil.

5. The Auxiliary charge pump output voltage is referred to as V_{PDA} and the output current I_{AUX} is the Up or Down current measured when $V_{PDA} = V_{DD}/2$.
   The conditions for the variation limits for the Up current are:
   either I_{AUX} = 128 or 256 µA and $0 < V_{PDA} < V_{DD} - 0{\cdot}5$ V
   or I_{AUX} = 512 µA and $0 < V_{PDA} < V_{DD} - 0{\cdot}65$ V
   The conditions for the variation limits for the Down current are:
   either I_{AUX} = 128 or 256 µA and $0{\cdot}5 \text{ V} < V_{PDA} < V_{DD}$
   or I_{AUX} = 512 µA and $0{\cdot}65 \text{ V} < V_{PDA} < V_{DD}$

6. The Main charge pump output voltage at pin PDP is referred to as V_{PDP} and at pin PDI as V_{PDI}. The output currents I_{MAIN} and $I_{INTEGRAL}$ are the up or down current Iprop(0), Iprop(1) or Iint measured when V_{PDP} or $V_{DPI} = V_{DD}/2$.
   The conditions for the variation limits for the Up current are :
   I_{MAIN} = 100 to 1000 µA or $I_{INTEGRAL}$ = 1 to 5 mA and $0 < V_{PDP} < V_{DD} - 0{\cdot}45$ V
   The conditions for the variation limits for the Down current are:
   I_{MAIN} = 100 to 1000 µA or $I_{INTEGRAL}$ = 1 to 5 mA and $0{\cdot}45 \text{ V} < V_{PDP} < V_{DD}$

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 40 °C to + 85 °C, all V_{DD} = + 3·6 to + 5·0 V, GND ref. = V_{SS}, any V_{DD} to any other V_{DD} = – 0·1 to + 0·1 V

A.C. Characteristics

Parameter	Min.	Typ.	Max.	Unit	Conditions
CONTROL BUS					
Clock rate CL input		1008		kHz	
Clock duty cycle CL input	40	50	60	%	
t_{DS}, input data set-up time	80			ns	See Fig. 7
t_{DH}, input data hold time	80			ns	See Fig. 7
t_{CWL}, t_{CWH}, CL input pulse width (to bus logic)	400		600	ns	See Fig. 7
t_{CL}, delay time, clock to latch	440			ns	See Fig. 7
t_{LW}, latch pulse high time	230			ns	See Fig. 7
t_{LH}, delay time, latch to clock	220			ns	See Fig. 7
t_{DSO}, output data set-up time	80			ns	See Fig. 8
t_{DHO}, output data hold time	80			ns	See Fig. 8
t_{ZS}, DATA line available to ACE9030	80		1200	ns	See Fig. 8
t_{ZH}, DATA line released by ACE9030	80		1200	ns	See Fig. 8
t_{CD}, delay from received message to transmitted response	4		4	cycles of CL	See Figs. 8 and 10
Rise and Fall times, all digital inputs:			50	ns	
DIGITAL OUTPUTS					
DOUT0 and 1 On time to V_{DD} – 0·2 V			100	µs	100 nF load and from
DOUT0 and 1 Off time to > 1 MΩ			100	µs	LATCHB rising edge
DOUT5, 6 and 7 rise and fall times			10	µs	30 pF load and to
DOUT8 rise and fall time			10	µs	D.C. specification
A to D CONVERTER					
Lowest transition, 0000 0000 to 0000 0001	0·07	0·15	0·23	V	Bandgap multiplier
Highest transition, 1111 1110 to 1111 1111	3·35	3·45	3·55	V	correctly trimmed
ADC conversion time (20 cycles of CL)		20		µs	CL = 1008 kHz
Input scanning rate (CL ÷ 40)		25·2		kHz	CL = 1008 kHz
Integral Non-linearity	– 1		+ 1	LSB	
Differential Non-linearity	– 0·5		+ 0·5	LSB	
Power supply sensitivity			1	Bit/V	Noise at 0 to 10 kHz
CRYSTAL OSCILLATOR					
Start-up time of crystal oscillator		5		ms	
Crystal effective series resistance (ESR)			25	Ω	To ensure start-up
Power dissipation in crystal		100	150	µW	
D to A CONVERTERS					
Full scale output level, DAC1, DAC2 & DAC3	3·35	3·45	3·55	V	Bandgap multiplier
Zero scale output level, DAC1	1·0		1·2	V	trimmed to nominal
Zero scale output level, DAC2 & DAC3	0·3		0·5	V	reference voltage
Integral Non-linearity	– 1		+ 1	LSB	
Differential Non-linearity	– 0·5		+ 0·5	LSB	
Output wideband and clock noise: 50 Hz to 1·1 MHz, flat integration 50 Hz to 3400 Hz with 750 µs de-emphasis			 0·5 0·1	 mV_{rms} mV_{rms}	
Power supply rejection ratio	20			dB	50 Hz to 25 kHz.
Settling time to within 10% of end of step (DAC3 with external 15 kΩ resistor)			5	µs	DAC1 and DAC2 not in Sleep mode, 10 pF load
Output load capacitance, DAC1 and DAC2			100	nF	
Output load capacitance, DAC3			30	pF	To guarantee stability
Internal series resistor, DAC1 and DAC2	7	15	40	kΩ	
DAC3 output current, sink or source	1·0			mA	

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 40 °C to + 85 °C, all V_{DD} = + 3·6 to + 5·0 V, GND ref. = V_{SS}, any V_{DD} to any other V_{DD} = – 0·1 to + 0·1 V

A.C. Characteristics (continued)

Parameter	Min.	Typ.	Max.	Unit	Conditions
LOW FREQUENCY AMPLIFIERS (1 and 2)					
Voltage Gain	1200	2800		V/V	
Input Offset		5	10	mV	
Open loop input resistance		1		MΩ	
Open loop output resistance		8		kΩ	
Unity Gain bandwidth		2		MHz	
Input bias current, inverting input			200	nA	
Power supply rejection at 100 kHz	35			dB	
Output voltage maximum, linear operation	V_{DDA} – 0·2			V	
Output voltage maximum, as a comparator	V_{DDA} – 0·1			V	
Output voltage minimum level, linear operation			0·2	V	
Output voltage minimum level, as a comparator			0·1	V	
Common mode input range	V_{SSA}		V_{DDA}	V	
Output slew rate	1			V/µs	
Output load capacitance			30	pF	
8 MHz OSCILLATOR and PLL					
OSC8 centre frequency		8·064		MHz	Control offset value at 000000 = $0A_{HEX}$
OSC8 VCO sensitivity		20		MHz/V	Control range value at 011110 = 21_{HEX}
OSC8 charge pump output current		50		µA	
CLK8 output load, resistive: capacitive:	15 15	25 25	100 30	kΩ pF	
CLK8 output amplitude	0·8	1·5	2·4	V_{pk-pk}	
CLK8 total output jitter (as f.m. deviation)			4	kHz	200 Hz to 8 kHz.
Start-up time at power-on, to default settings			15	ms	With a loop filter as described in fig. 17
Lock time to within 100 ppm, after reprogramming set-ups			15	ms	
AFCIN F.M. DISCRIMINATOR and AFC					
AFCIN input signal level	0·05		2·5	V_{pk-pk}	
AFCIN input impedance, resistive: capacitive:	50		 10	kΩ pF	
Input frequency	400		500	kHz	
Input signal to integrated noise ratio	10			dB	I.F. ± 15 kHz.
Input Schmitt window (threshold difference)	10	20	30	mV	
AUDIO signal SINAD, psophometric, note 7	45			dB	1 kHz tone at 3 kHz peak deviation on AFCIN input at I.F.
AUDIO signal hum and noise, note 7			– 46	dB	
AUDIO output signal level, note 7	480	640		mV_{ms}	
AFCOUT load			30	pF	
AFCOUT duty cycle	40		60	%	
AFCOUT rise and fall times			75	ns	

Note

7. AUDIO signal quality is measured with feedback components as shown in figure 18 and with 500 mV peak to peak input to AFCIN. Discriminator gain is set with D = 3 and M = 40 and V_{DD} = 3·75 V and a crystal at 14·85 MHz. SINAD is defined as the ratio of wanted signal to all unwanted output, measured simultaneously with filters. The hum and noise figure is defined as the ratio of output power at AUDIO when AFCIN is not driven to the output power when AFCIN is driven as specified above.

ELECTRICAL CHARACTERISTICS

These characteristics apply over these ranges of conditions (unless otherwise stated):

T_{AMB} = – 40 °C to + 85 °C, all V_{DD} = + 3·6 to + 5·0 V, GND ref. = V_{SS}, any V_{DD} to any other V_{DD} = – 0·1 to + 0·1 V

A.C. Characteristics (continued)

Parameter	Min.	Typ.	Max.	Unit	Conditions
LO2 Multiplier					
Amplitude	47		120	mV_{rms}	Circuit as in fig. 15,
Reference frequency content of output		– 10		dBc	with RD = 3·9 kΩ and
2nd, 4th, or 5th harmonic content of output		– 20		dBc	V_{DD} = 3·75 V. Load is
6th and higher harmonics in output		– 30		dBc	3·7 pF and 1 kΩ.
SYNTHESISERS					
Reference divider					
Reference divider input frequency	5		30	MHz	
Drive level into CIN1 from external oscillator	400			mV_{pk-pk}	With crystal oscillator powered down
CIN1 input capacitance			10	pF	
CIN1 input resistance	10			kΩ	
Auxiliary synthesiser					
FIA input frequency	10		135	MHz	May be a sinewave
Rise and fall times of inputs			10	ns	
Timing Skew between FIA and FIAB			± 2 or ± 10%	ns signal period	See Fig. 6 Both maxima must be met
FIA, FIAB differential signal level with both sides driven	180 100			mV_{pk-pk} mV_{pk-pk}	Each input, 5 to 50 & 99 to 135 MHz Each input, 50 to 99 MHz
FIA single input drive level with FIAB decoupled to V_{SS}	360 200			mV_{pk-pk} mV_{pk-pk}	One input, 5 to 50 & 99 to 135 MHz One input, 50 to 99 MHz
FIA, FIAB common mode range	V_{DD} – 1·7		V_{DD} – 0·7	V	
FIA, FIAB input capacitance			10	pF	
FIA, FIAB differential input resistance	10			kΩ	Note 8
Auxiliary Synthesiser comparison frequency			2	MHz	
Main Synthesiser					
FIM input frequency	4		20	MHz	
Rise and fall times of inputs			10	ns	
FIM - FIMB Timing Skew			± 2 or ± 10%	ns signal period	See Fig. 6 Both maxima must be met
FIM, FIMB differential signal level with both sides driven.	100			mV_{pk-pk}	Each input, 4 to 20 MHz
FIM single input drive level with FIMB decoupled to V_{SS}	200			mV_{pk-pk}	One input, 4 to 20 MHz
FIM, FIMB common mode range	V_{DD} – 1·7		V_{DD} – 0·7	V	
FIM, FIMB input capacitance			10	pF	
FIM, FIMB differential input resistance	10			kΩ	Note 8
Delay FIM rising to MODMP/MODMN changing			30	ns	
Main Synthesiser comparison frequency			2	MHz	

Note

8. To simplify single ended drive there is a resistor between FIA and FIAB and another between FIM and FIMB. In this mode the inputs should drive FIA or FIM with D.C. coupling and the other inputs FIAB and FIMB should be decoupled to ground by external capacitors.

TIMING WAVEFORMS

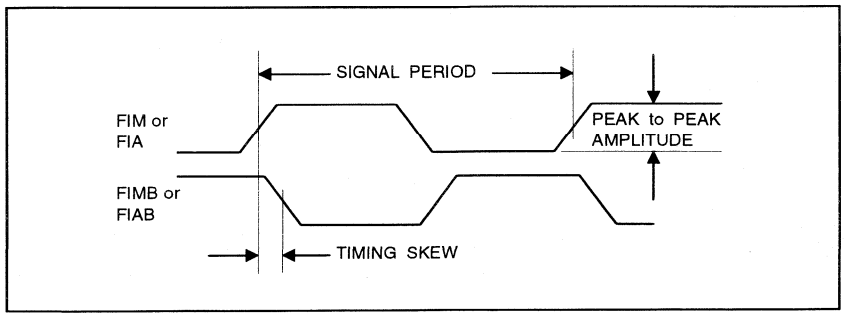


Fig. 6 Synthesiser Inputs

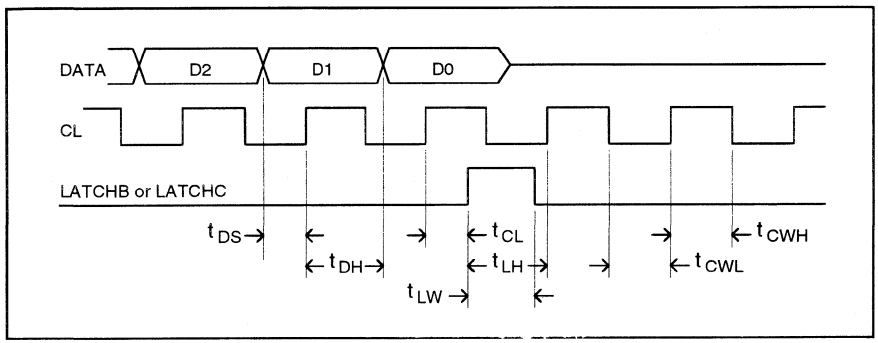


Fig. 7 Control Bus input timing

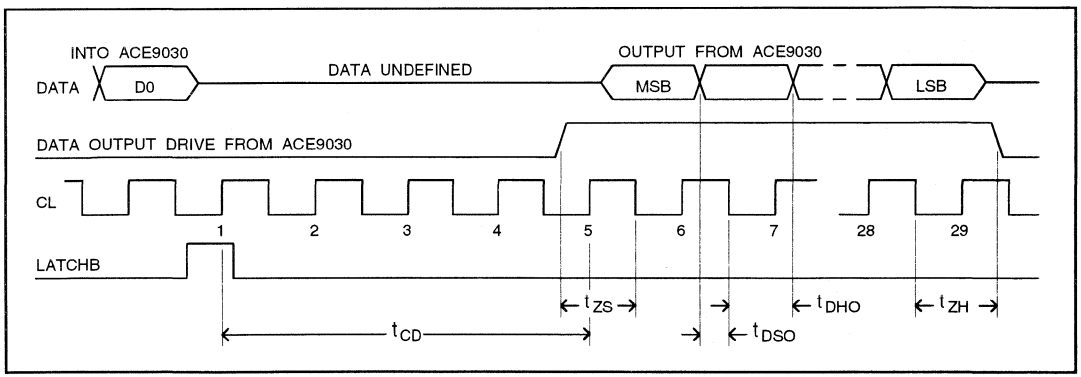


Fig. 8 Control Bus output timing

FUNCTIONAL DESCRIPTION - CONTROL BUS

The functions of the ACE9030 fall into two separate groups, the Radio Interface and the Synthesisers.

The common control bus splits the input strings differently for these two sections so this bus operation is described first as an introduction to the available features.

All functions are controlled by a serial bus; DATA is a bi-directional data line, to input all control data and to output the results of measurements in the Radio Interface section, CL is the clock, and LATCHB and LATCHC are the latch signals at the end of each control word for either the Radio Interface or the Synthesiser section respectively.

CL is a continuously running clock at typically 1·008 MHz, and all incoming and output data are latched on rising edges of this clock. The controller should clock data in and out on falling clock edges. For bus control purposes the frequency of CL may be widely varied and this clock does not need to be continuous, however, the sampled I.F. signal AFCOUT, the Polling ADC, and the Lock Detect Filter also use CL as the sampling clock. In systems where any of these are required the clock CL is constrained to be 1·008 MHz and to be continuous.

To ensure clean initialisation the clock CL should give at least 8 cycles before the power-up command and similarly to set the control logic to known states there should be 8 cycles of CL after a power-down command.

During normal operation there should be at least 30 cycles of CL between latch pulses, 24 for the data bits (see figures 9,10 & 11) plus 6 extra. This minimum becomes 36 cycles if the extended synthesiser programming command (A2) is used.

Radio Interface Bus - Receive

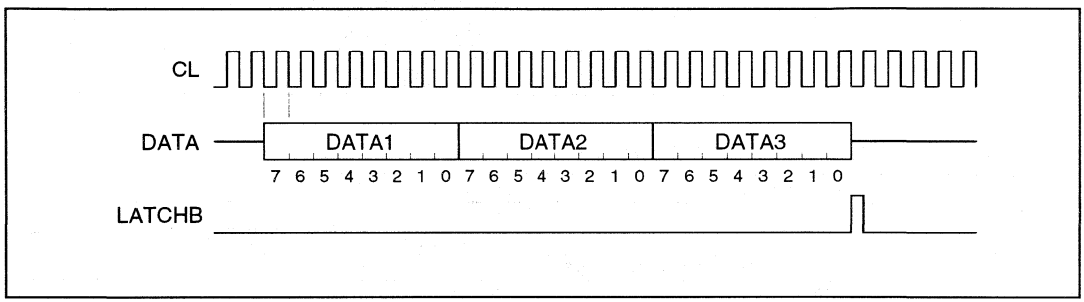


Fig.9 Radio Interface receive bus timing

The received data is split into three bytes, where DATA1 normally contains a value to be loaded into a destination set by DATA2 and DATA3. When a command does not need to put any information into byte DATA1 a preamble xx1010xx is recommended to fill this byte. It is possible to set-up several features in one bus operation and to allow this the decoding only acts on single or selected bits; the others are given as "x" in the block descriptions. Two bits of DATA2 also set the type of command, with four options:

DATA2 bit 7	DATA2 bit 6	Type of Command	Comment
0	0	SLEEP	No reply
0	1	NORMAL	Send requested data
1	0	SET-UP	No reply
1	1	TEST	No reply

Sleep mode is selected to put the cellular terminal into a very low power state for when it is "Off" and neither waiting for, nor setting up a call. In Sleep only the crystal and 8·064 MHz oscillators, DAC1 and DAC2, the OSC8 phase locked loop, and the CLK8 output driver will be active, and are used to clock the microcontroller. To reduce the supply current to its minimum in Sleep the synthesisers must also be powered down, by a Word D message with DA and DM both set HIGH as described under **Synthesiser Bus - Receive Only**. During Sleep all set-up values are retained unless changed by a Set-up command. The exit from Sleep is by any Normal command.

Normal commands will end Sleep mode but are primarily used to change the operating mode of the cellular terminal or to request ADC data. The response to Normal commands is the only reason for the ACE9030 to drive the serial bus.

Set-up commands are used to adjust various operating parameters but can also initiate a logic restart if DATA3 bits 1 and 0 are both "1" so for routine changes of set-ups these bits should always be 00.

Test mode is included only for use during chip manufacture.

The Sleep Command - DATA2 bits 7, 6 = 00

DATA1	DATA2	DATA3
xx1010xx	00xxxxxx	xxxxxxxx

Summary of Normal Commands - DATA2 bits 7, 6 = 01

Normal commands are always a request for data; the ADC registers to be read are defined by Y1 and Y0 in DATA3. A normal command will also end Sleep mode.

BIT	EFFECT when at 0	EFFECT when at 1
DATA2:		
7	With DATA2:6 defines command type	-
6	-	With DATA2:7 defines command type
5	Discriminator powered down	Discriminator active.
4	-	Load Lock threshold register from DATA1:7-1
3	DAC3 powered down	DAC3 active
2	-	Load DOUT7-0 from DATA1:7-0
1	-	Load DAC3 from DATA1:7-0
0	Not used	Not used
DATA3:		
7	Not used	Not used
6	LO2 multiplier powered down	LO2 multiplier active
5	Set DOUT8 to OFF	Set DOUT8 to ON, to output the ADC reference voltage
4	-	Load ADC1 comparator from DATA1:7-0
3	-	Load DAC1 from DATA1:7-0
2	-	Load DAC2 from DATA1:7-0
1	Y1 Decode with DATA3:0 for Polling ADC register read	
0	Y0 Decode with DATA3:1 for Polling ADC register read	

Summary of Set-up Commands - DATA2 bits 7, 6 = 10

BIT	EFFECT when at 0	EFFECT when at 1
DATA2:		
7	-	With DATA2:6 defines command type
6	With DATA2:7 defines command type	-
5	Not used	Not used
4	-	Set OSC8 VCO range from DATA1:5-0
3	-	Set OSC8 VCO offset from DATA1:5-0
2	Select input A for ADC3	Select input B for ADC3
1	Select input A for ADC2	Select input B for ADC2
0	OSC8 off	OSC8 on
DATA3:		
7	Crystal oscillator off	Crystal oscillator on
6	Bandgap off - use external reference	Bandgap on
5	-	Set discriminator divisors from DATA1:7,6 and lock detect period from DATA1:5 and OSC8 divisors from DATA1:2-0
4	-	Set bandgap trim from DATA1:7-0
3	Not used	Not used
2	Not used	Not used
1	-	Do a restart if both DATA3 bits 1 and 0 are at 1
0	-	Do a restart if both DATA3 bits 1 and 0 are at 1

Radio Interface Bus - Transmit

The ACE9030 only drives the bus in response to a request for data by a Normal command as described above. To avoid any bus contention, there is a delay from the end of a data request to the start of the response, see figure 10. The data will start on the fifth rising edge of CL after the rising edge of LATCHB.

The output Preamble word begins with a fixed pattern 1 0 1 0 and then includes the source code number (Y1, Y0) for the Result words and the status of the Lock Detect from the synthesiser, all as described in the section Polling A to D Converter.

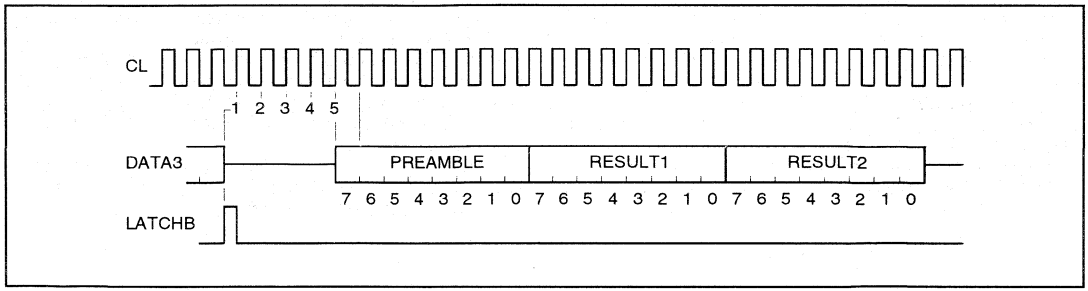


Fig.10 Radio Interface transmit bus timing

Synthesiser Bus - Receive Only

The overall format to control the synthesiser is basically the same as for the Radio Interface. There is an option of a 32 bit string to allow a channel change with loop gain control in only one message and also the width of the LATCHC pulse is used to set the duration of speed-up mode when changing channels.

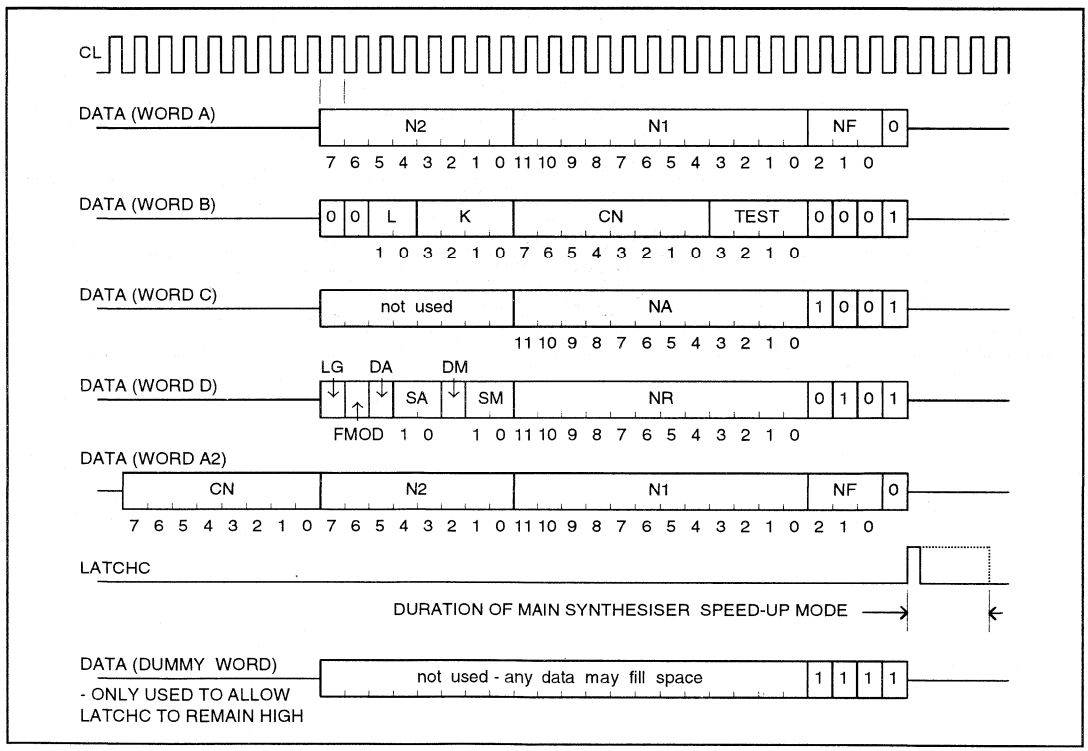


Fig.11 Synthesiser bus timing

Data is accepted by the circuit on the rising edge of LATCHC. Programmable divider ratios will be changed at their next re-load, at up to a whole comparison period after the LATCHC edge.

Normal channel changes require only word A but if it is necessary to maintain exactly uniform loop dynamics the parameter CN (see Main Synthesiser - Normal Mode) must also change. This can be achieved by either sending a word B for the CN parameter before word A for the frequency or alternatively the extended command A2 can be used to combine both in one long word. This A2 mode is not supported by the ACE9050 as it is not necessary for most cellular terminals.

After the power-on initialisation Word B is altered only for a channel change, so the new values are held until the following Word A or A2 has been written, when both words are used at the same time to ensure a clean change.

The LG bit in Word D sets whether A or A2 mode is to be used, 0 for A and 1 for A2.

Speed-up drive is active for the duration of the LATCHC pulse that loads the A or A2 word and if it is required the pulse will typically be hundreds of cycles of CL in duration.

In some applications the system performance can be improved by holding LATCHC at HIGH to minimise clock noise on the synthesisers. LATCHC also controls Speed-up mode and so to exit speed-up mode after a channel change the LATCHC must be driven LOW and then a dummy command can be added to get LATCHC back to HIGH. This dummy command should be a non-functional word formed by setting the last four bits to 1111 as in figure 11; the value or the number of the data bits before the four 1's are of no significance so the typical schemes are to send either a standard 24 bit message ending 1111 or a special 4 bit only message of 1111 and in both cases the LATCHC is kept HIGH until the next channel change.

The TEST bits in Word B must be set to 0000 for normal operation and the first two bits in Word B should be set to 00 to be sure of compatibility with future variants.

Summary of Synthesiser Programming

BIT STRING	Range of values	FUNCTION
N1	3 - 4095	Main synthesiser down count; prescaler at lower modulus.
N2	1 - 255	Main synthesiser up count; prescaler at higher modulus.
NF	0 - 7	Main synthesiser fractional increment numerator.
TEST	0000	This state must be selected in every Word B for normal operation. TEST pin will be held LOW to screen adjacent PDA pin. Other test modes are for use during chip manufacture only.
CN	0 - 255	Main charge pump current scaling coefficient.
K	0 - 15	Integral charge pump speed-up mode multiplying factor.
L	0 - 3	Proportional charge pump speed-up mode exponent, giving × 2, × 4, × 8 or × 16 current.
NA	3 - 4095	Auxiliary synthesiser VCO divider ratio.
NR	8 - 4095	Reference divider ratio.
SM	0 - 3	Main synthesiser comparison frequency select.
DM	0, 1	Main synthesiser in standby mode if DM set HIGH.
SA	0 - 3	Auxiliary synthesiser comparison frequency select.
DA	0, 1	Auxiliary synthesiser in standby mode if DA set HIGH.
FMOD	0, 1	Fractional-N denominator, $^1/_5$'s when at "0" or $^1/_8$'s when at "1".
LG	0, 1	Control bus mode select - Word A if LOW or Word A2 if HIGH.

FUNCTIONAL DESCRIPTION - BLOCKS IN THE RADIO INTERFACE

Power-On Reset Generator

To ensure a tidy start-up there is an internal power-on detector to initialise various registers.

This initialisation leaves the Radio Interface in Sleep mode with the crystal and 8·064 MHz oscillators running. The 8·064 MHz PLL will be set up for a 15·36 MHz crystal as a default to ensure the microprocessor is not clocked too fast during the start up sequence. Any Normal command can be used to change to active operation.

A software Restart command can be sent to force the Radio Interface to the power-on reset state. This command is:

DATA1	DATA2	DATA3
xxxxxxxx	10xxxxxx	xxxxxx11

Digital Outputs

The nine digital outputs, DOUT8 to DOUT0, are used to control the status or function of radio subsections external to the ACE9030 and are controlled by a Normal type command with a logic "1" setting the output to HIGH or ON and a logic "0" giving LOW or OFF.

Outputs DOUT0 and DOUT1 are power switches from V_{DDX} to supply Front-End circuits. Both are forced to OFF in Sleep mode.

Outputs DOUT2 to DOUT4 are logic level outputs to control various functions in the cellphone. DOUT2 and DOUT3 are forced to HIGH and DOUT4 is forced to high impedance in Sleep mode.

Outputs DOUT5 to DOUT7 are low current outputs with reduced voltage swing to control power down in the ACE9010 and ACE9020. All three are forced to LOW in Sleep mode.

Output DOUT8 can be driven by the buffered Band-gap based ADC reference voltage and is included for test and setting-up purposes, as well as for driving a temperature sensing thermistor read through one of the ADC channels. DOUT8 is forced to high impedance in Sleep mode.

The control formats are Normal commands:

DATA1	DATA2	DATA3
$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$	01xxx1xx	xxxxxxxx

where DATA1 bits 7 to 0 control DOUT7 to DOUT0 respectively when enabled by DATA2 bit 2, and:

DATA1	DATA2	DATA3
xxxxxxxx	01xxxxxx	xx D_5 xxxxx

where DATA3 bit 5 controls DOUT8 directly.

Lock Detect Filter

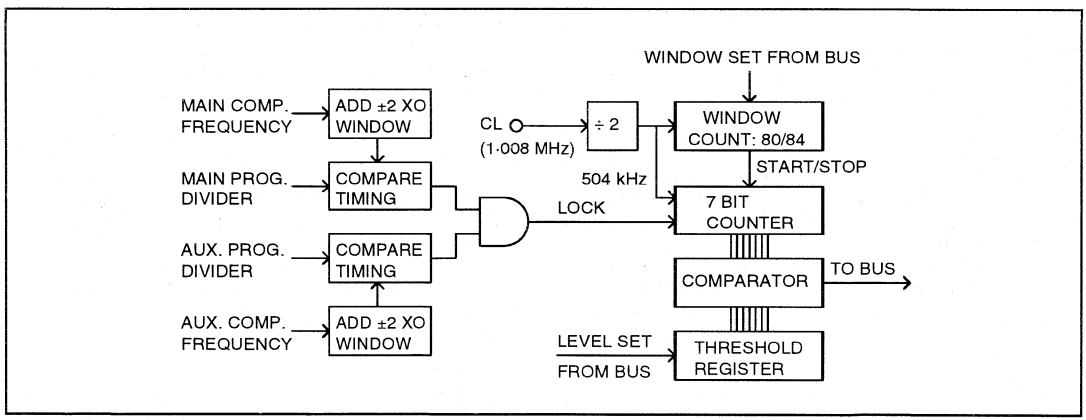


Fig. 12 Lock Detect Block Diagram

The Lock Detect Filter processes the phase errors in both synthesisers to give a clean signal to put onto the bus as a single bit added to the ADC read response.

In the synthesiser section of the ACE9030 the time differences between the active edges of the outputs of the programmable dividers and of the reference divider are compared with a window of two cycles of the reference clock, XO, from the crystal oscillator. If a loop has a time difference, or phase error, larger than this window then that loop is deemed unlocked and its lock signal is held low for a whole comparison period, giving a Main Lock and an Auxiliary Lock signal. When both synthesisers are active the error signals are combined by an AND function to give the internal signal LOCK. If either synthesiser is powered down its lock is disregarded and if both are powered down the ACE9030 will always give LOCK at LOW, the unlocked state, to be output on the bus. This final signal LOCK is normally HIGH to indicate locked loops but will pulse low for one or more comparison periods when an active synthesiser is unlocked.

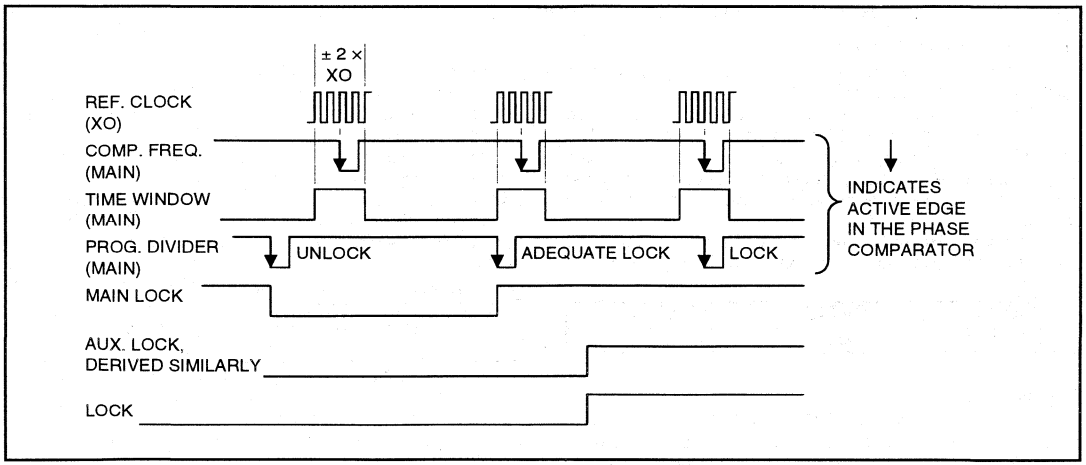


Fig. 13 Typical Lock Detect Waveforms

Pulses can occur on the LOCK signal at a rate up to the higher of the Main and Auxiliary comparison frequencies, and this is often either 12·5 kHz for NMT and ETACS (50 kHz if Fractional-N is used) or 30 kHz for AMPS so some extra filtering is needed to get a clean lock indicator.

LOCK is filtered by first sampling at 504 kHz (the bus clock CL divided by two) and then counting the number of HIGH samples in a pre-determined period. There are two selections available for this counting period, approximately 160 µs (2 periods of 12·5 kHz or 8 of 50 kHz) or approximately 167 µs (5 periods of 30 kHz) which are set by a second counter, also running at 504 kHz and with a fixed modulus of 80 or 84. LOCK is stable for each comparison period so the counts for each comparison frequency are always in blocks of 40 for 12·5 kHz, 10 for 50 kHz or 16 for 30 kHz.

The value in the LOCK sample counter is compared with a threshold previously set by another bus command, to determine if the loops are locked, the result is then output as the last bit in the pre-amble word in the response to a Normal command, before the ADC levels are given, as described in the section Polling A to D converter.

The filter period is selected by the following Set-up command where DATA1 bit D_5 sets the period to one of the two values to suit whichever cellular system is to be used:

DATA1	DATA2	DATA3
xx D_5 xxxxx	10xxxxxx	xx1xxx00

DATA1:5 = 0 sets 160 µs for NMT or ETACS (Window count = 80) and DATA1:5 = 1 sets 167 µs for AMPS (Window count = 84).

The threshold is set by a Normal command:

DATA1	DATA2	DATA3
D_7 D_6 D_5 D_4 D_3 D_2 D_1 x	01x1xxxx	xxxxxxxx

DATA1 bits D_7 to D_1 form a 7 bit binary number in the range 0 to 127, which is the threshold value to be loaded. The window period of 80 or 84 clock cycles sets the maximum count value that can be found; the effect of unlock is to reduce the actual count by at least one comparison period's worth of samples 40, 10, or 16 so a suitable threshold can easily be chosen. Assuming that the maximum sensitivity is required the threshold should be set at just above the maximum count (80 or 84) minus the effect of one unlock count (40, 10, or 16), to give suggested thresholds of at least 42 (for 12·5 kHz) or 72 (for 50 kHz) or 70 (for 30 kHz). In each case any convenient number between these suggestions and the maximum count may be used as the selection is not critical.

Polling A To D Converter

A five channel polling Analog to Digital Converter is used to monitor various analog levels, such as Received Signal Strength, Transmitter Power, Temperature and Battery Voltage. The 8 bit ADC has a nominal range of 0·15 V to 3·45 V for codes 00 to FF and is connected to each input channel, ADC1 to ADC5, in turn by the scanning logic. The results are put into individual registers for reading by the microcontroller. The successive approximation technique is used, with the bus clock CL controlling both the timing of the conversion and also the polling around the inputs. The voltage reference for the ADC is shared with the three DAC's and is derived from the bandgap voltage through a trimming multiplier which can be monitored on DOUT8 and is described in the section Band-Gap Reference. Some channels are scanned more frequently than others, with the pattern:

5, 1, 5, 2, 5, 1, 5, 3, 5, 1, 5, 4,

which repeats continuously. With clock CL at its normal 1008 kHz frequency, the scanning rates are 12·6 kHz for ADC5, 6·3 kHz for ADC1 and 2·1 kHz for ADC2, 3 and 4.

Channels 2 and 3 each have two options, 2A, 2B and 3A, 3B as pins to connect to alternative points to monitor. The selection is by a Set-up command:

DATA1	DATA2	DATA3
xxxxxxxx	10xxx D_2 D_1 x	xxxxxx00

where DATA2 bit D_2 selects ADC3B when HIGH or ADC3A when LOW for measurement by channel 3, and DATA2 bit D_1 selects ADC2B when HIGH or ADC2A when LOW for measurement by channel 2.

The ADC data in the five registers is read in response to a Normal command, with the two results to be output being selected by two bits of DATA3:

DATA1	DATA2	DATA3
xxxxxxxx	01xxxxxx	xxxxxxY_1Y_0

where Y_1 Y_0 are decoded to select:

Y_1	Y_0	Data requested
0	0	ADC5 & ADC1
0	1	ADC5 & ADC2A/B
1	0	ADC5 & ADC3A/B
1	1	ADC5 & ADC4

The requested data is then clocked out after a fixed delay, with a preamble followed by the two results:

PREAMBLE	RESULT 1	RESULT 2
1010 Y_1 Y_0 0 L	RRRRRRRR	RRRRRRRR

The Y_1 Y_0 code is output to confirm the data selection and is the same as in the Normal command that requested the data, detailed above, L is the Lock Detect status from the Lock Detect Filter, and the two results are in the order ADC5 in RESULT 1 and ADC1, 2, 3, or 4 in RESULT 2.

The level in the ADC1 register is continuously compared with a threshold number such that if ADC1 is above this threshold the output pin RXCD is driven HIGH and can be used to indicate the presence of a received carrier. The threshold is set by a Normal command on the bus, with the value in DATA1:

DATA1	DATA2	DATA3
DDDDDDDD	01xxxxxx	xxx1xxxx

IREF Bias Circuit

To set the operating current for several blocks in the Radio Interface there is a bias pin I_{REF} which should be connected to the ground plane (V_{SS} pins) via a resistor whose value depends on the supply voltage, 68 or 100 kΩ for 3·75 V or 4·85 V nominal V_{DD}. The current into this pin is then mirrored to the various functional blocks. To reduce the noise on this bias a capacitor can be added from the IREF pin preferably to the supply or alternatively to a good ground. A value of 82 nF offers a good compromise between noise rejection and power-up time.

D to A Converters

There are three 8-bit DAC's with buffered outputs in the ACE9030.

DAC1 and DAC2 have a high zero offset, a nominally 15 kΩ output series resistor, and are stable when driving up to a 100 nF load capacitance.

DAC3 has a low zero offset and no output resistor. In order to guarantee stability the capacitance of the load on DAC3 must be no more than 30 pF.

The output resistors on DAC1 and DAC2 are used to form part of a low pass filter and these DAC's are intended to be used to adjust the crystal frequency as given below under Crystal Oscillator.

The level for each DAC is set by a Normal command:

DATA1	DATA2	DATA3
DDDDDDDD	01xxxx D_1 x	xxxx D_3 D_2 xx

where the data in DATA1 is loaded into DAC1 if DATA3 bit D_3 is HIGH, into DAC2 if DATA3 bit D_2 is HIGH, or into DAC3 if DATA2 bit D_1 is HIGH.

DAC1 and DAC2 remain active during Sleep mode but the outputs are driven with reduced current capability; this will slightly reduce the accuracy and will significantly increase the settling time to any level change. DAC3 is powered down in Sleep mode.

To power down DAC3 outside of Sleep mode, a Normal command may be used:

DATA1	DATA2	DATA3
xxxxxxxx	01xx D_3 xxx	xxxxxxxx

where DAC3 is active if DATA2 bit D_3 is HIGH or powered down if DATA2 bit D_3 is LOW.

L.F. Amplifiers

Two identical low frequency amplifiers are provided; one has inputs AMPP1 and AMPN1 driving output AMPO1, the other has inputs AMPP2 and AMPN2 driving output AMPO2.

A typical use for AMP1 is as a linear amplifier to buffer the DAC3 output to drive the transmit power control in a software controlled loop with a power sensor input to ADC5.

AMP2 is typically used as a comparator to detect transmit power independent of the software as a system integrity check. The System Controller can then gate the presence of transmitter power on AMPO2 with the absence of received carrier on RXCD to detect a non-valid status and re-initialise the system.

Crystal Oscillator

A crystal oscillator maintaining circuit is provided on pins CIN1 and CIN2 for use with a crystal at typically 12·8, 14·85 or 15·36 MHz depending on the cellular system chosen. The circuit is designed for a crystal cut for a 20 pF load and with an ESR less than 25 Ω. To ensure reliable fast start times for this oscillator the bias current is increased significantly for the first 2047 cycles of oscillation after power-up, a restart command or after an oscillator ON command and then automatically changes to the lower normal level. The normal level has been chosen to still guarantee start-up if the circuit should be stopped by some external interference but to consume less power than the fast start mode.

The buffered internal output of this oscillator is used in several sections of the chip and is referred to as XO in this data sheet. This oscillator can be trimmed by using DAC1 and DAC2 to control varicap diodes and so to pull the frequency, the two DAC's may be used to give separate AFC and temperature compensation. A typical external circuit is shown in figure 14.

If preferred, an external oscillator can be used by driving into CIN1 with CIN2 left open circuit. To allow this external drive the internal oscillator should be shut down by using a Set-up command with DATA3 bit D_7 at LOW. The internal oscillator is switched on at power-up, at restart, and by a Set-up command with DATA3 bit D_7 at HIGH:

DATA1	DATA2	DATA3
xxxxxxxx	10xxxxxx	D_7 xxxxx00

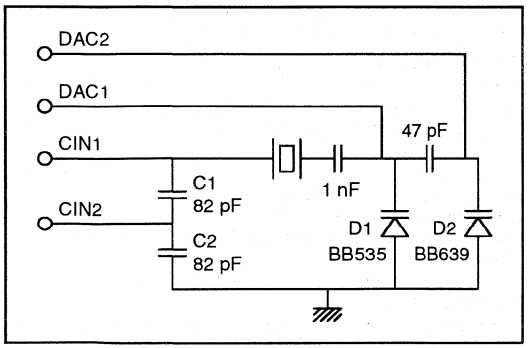


Fig. 14 Crystal Oscillator Trimming Circuit with Typical Component Values

Crystal Multiplier for LO2

To mix the first intermediate frequency signal down to the second IF a second local oscillator is needed. In the ACE9030 there is a crystal frequency multiplier to generate this signal by squaring the crystal oscillator waveform and selecting the desired harmonic. To multiply the crystal frequency by 3 or 5 output LO2 is driven at the reference frequency with a 1:1 mark space ratio. This ratio of 1:1 is chosen to minimise the even harmonics, especially the second and fourth. A tuned circuit will pick off the required harmonic. The value of the resistor RD depends on the output amplitude and on V_{DD}. Some suggested values based on simulations are given in table1.

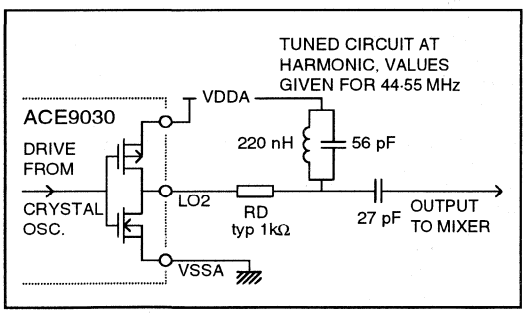


Fig. 15 Basic Circuit of the Crystal Multiplier

V_{DD} V	RD Ω	Output Amplitude min	Output Amplitude max
3·75	3·9 k	47 mVrms	120 mVrms
4·85	5·6 k	47 mVrms	115 mVrms
3·75	390	305 mVrms	406 mVrms
4·85	680	290 mVrms	432 mVrms

Table 1 Suggested RD values.

Typical frequencies generated by the multiplier are:

Crystal	Multiplier	LO2	1st I.F.	2nd I.F.
14·85 MHz	x 3	44·55 MHz	45·00 MHz	450 kHz
15·36 MHz	x 5	76·80 MHz	77·25 MHz	450 kHz

Typical performance for noise power measured in the adjacent channels,16 kHz wide at 25 kHz offset is – 80 dBc.

To power down the multiplier if it is not required, a Normal command can be used with DATA3 bit D6 set to LOW, to set the multiplier power on DATA3 bit D6 should be set to HIGH:

DATA1	DATA2	DATA3
xxxxxxxx	01xxxxxx	x D_6 xxxxxx

Band-Gap Reference

A band-gap voltage reference is used to set levels in the ADC, in the DAC's and the currents in the synthesiser charge pumps. This voltage is smoothed by an external decoupling capacitor on the DECOUP pin and to help improve low frequency filtering this pin has a high impedance drive.

The voltage derived for the ADC full range reference can be monitored through pin DOUT8. The Radio Interface DAC reference is nominally the same as the ADC reference and it can be monitored independantly of DOUT8 by setting DAC3 (the low output impedance DAC) to full scale.

To power down the band-gap reference to allow the use of an external reference voltage on pin DECOUP the following Set-up command can be used:

DATA1	DATA2	DATA3
xxxxxxxx	10 xxxxxx	x D_6 xxxx00

where the band-gap is powered down if DATA3 bit D6 is LOW or is active if DATA3 bit D6 is HIGH.

The band-gap voltage multiplier for the ADC and DAC reference (nominally 3·45 V) can be adjusted by a Set-up command to correct for production spreads:

DATA1	DATA2	DATA3
DDDDDDDD	10xxxxxx	xxx1xx00

where the value in DATA1, G_{BG} sets the gain from band-gap to output voltage according to the approximate equation:

$$\frac{V_{OUT}}{V_{BG}} = \frac{(430 \times G_{BG} + 355 \times 10^3)}{(145 \times 10^3)}$$

For a typical V_{BG} of 1·2 V the number is approximately 144 (= 90_{HEX}) and for a typical V_{BG} of 1·3 V the number is approximately 70 (= 46_{HEX}) and a suitable trimming pattern can be chosen.

8·064 MHz Oscillator

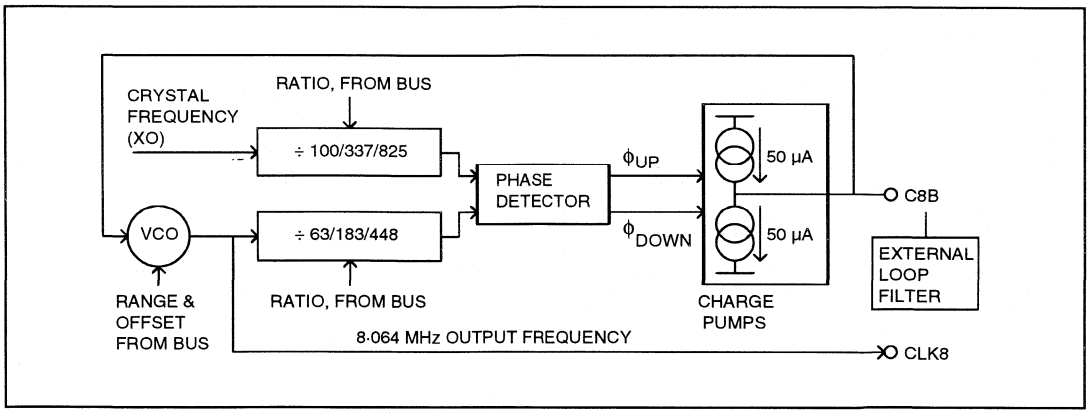


Fig. 16 OSC8 Block Diagram

An 8·064 MHz oscillator OSC8 is provided to drive the ACE9050 System Controller through pin CLK8. ACE9050 further drives the ACE9040 Audio Processor and the CL bus clock via a ÷ 8 divider. OSC8 is locked to the crystal oscillator by a phase locked loop with an external filter on pin C8B.

This loop can be programmed by a Set-up command to give the correct output frequency with any of the normally used crystals. Note that the same Set-up command uses DATA1 bit D_5 for the lock logic and bits D_7 and D_6 for the Discriminator programming:

DATA1	DATA2	DATA3
xxxxx D_2 D_1 D_0	10xxxxxx	xx1xxx00

where D_2 D_1 D_0 act as in table 2. At power-on reset the setting is D_2 D_1 D_0 = 110, the values for a 15·36 MHz crystal, so that the microcontroller is never clocked too fast with any of the crystals and can then send the Set-up message to set D_2 D_1 D_0 to the correct levels.

With a 14·85 MHz crystal it is not possible to both use a high comparison frequency and get the exact 8·064 MHz output, so two options are provided. The lower comparison frequency will give the output exactly correct but will need larger capacitors in the loop filter and the higher option allows smaller capacitors and can improve close-in phase noise by having a larger loop bandwidth, but gives a very small frequency error - this error should have no effect in a practical cellular terminal.

A Sleep command will not change the status of OSC8; if enabled it will remain active when put into Sleep mode and when returning to Normal mode. If the OSC8 oscillator is not required it can be switched off by a Set-up command:

DATA1	DATA2	DATA3
xxxxxxxx	10xxxxx D_0	xxxxxx00

where DATA2 bit D0 at LOW gives OSC8 OFF or DATA2 bit D_0 at HIGH gives OSC8 ON.

To allow for design and manufacturing tolerances the VCO can be trimmed by two set-up commands, each of which loads a 6 bit value in DATA1 into a control register. One sets frequency "Range" (effectively the VCO gain but also with an effect on the centre frequency):

DATA1	DATA2	DATA3
xx D_5 D_4 D_3 D_2 D_1 D_0	10x1xxxx	xxxxxx00

The other sets frequency "Offset" (effectively the VCO centre frequency but also with an effect on the gain):

DATA1	DATA2	DATA3
xx D_5 D_4 D_3 D_2 D_1 D_0	10xx1xxx	xxxxxx00

The default values loaded by the power-on reset are Offset = $0A_{HEX}$ and Range = 21_{HEX} and were chosen to help ensure that the output clock on CLK8 does not run faster than 8·064 MHz while better values are to be loaded. Experimental results suggest that these default values can often be left unchanged for normal operation.

The output of the phase comparator charge pump is on pin C8B so that an external loop filter can be connected. This loop filter then drives the VCO control voltage, also through

Command Data D2 D1 D0	Crystal frequency	Crystal divider	PLL comp. freq. (kHz)	OSC8 divider	Exact CLK8 output (MHz)	Error (ppm)
1 0 0	12·8 MHz	÷100	128	÷63	8·064	0
0 1 1	14·85 MHz	÷825	18	÷448	8·064	0
1 0 1	14·85 MHz	÷337	44·065281	÷183	8·0639466	–7
1 1 0*	15·36 MHz	÷120	128	÷63	8·064	0

* Power up default

Table 2

pin C8B to close the loop. An integration is needed to set the VCO onto the correct frequency and other components can then ensure loop stability. Enough filtering must be provided to give a clock output suitable for all of its uses - microprocessor clock, F.M. discriminator, and audio filtering. A typical loop filter is shown in figure 17.

The filter is shown connected to V_{DDA} as an A.C. ground to give better noise rejection than using V_{SS}. Typical component values for a comparison frequency of 18 kHz are R8F = 6·8 kΩ and C8F = 82 nF to give low comparison frequency spurs and R8F = 47 kΩ and C8F = 1·5 nF for higher loop bandwidth and less close in noise. In practical applications the loop filter should be designed to give the optimum balance between comparison sideband supression and close-in phase noise. The sideband energy is reduced by the frequency division that occurs in the ACE9050 and ACE9040 before the clocks act on ACE9040's sensitive switched capacitor filters.

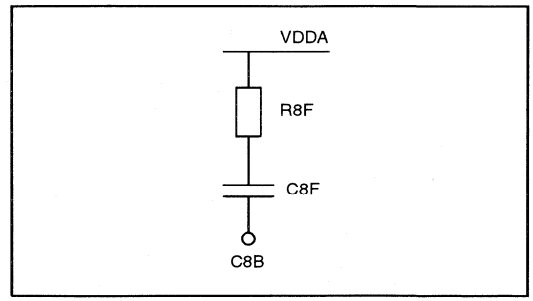


Fig. 17 Typical OSC8 Loop Filter

AFC Amplifier and Discriminator

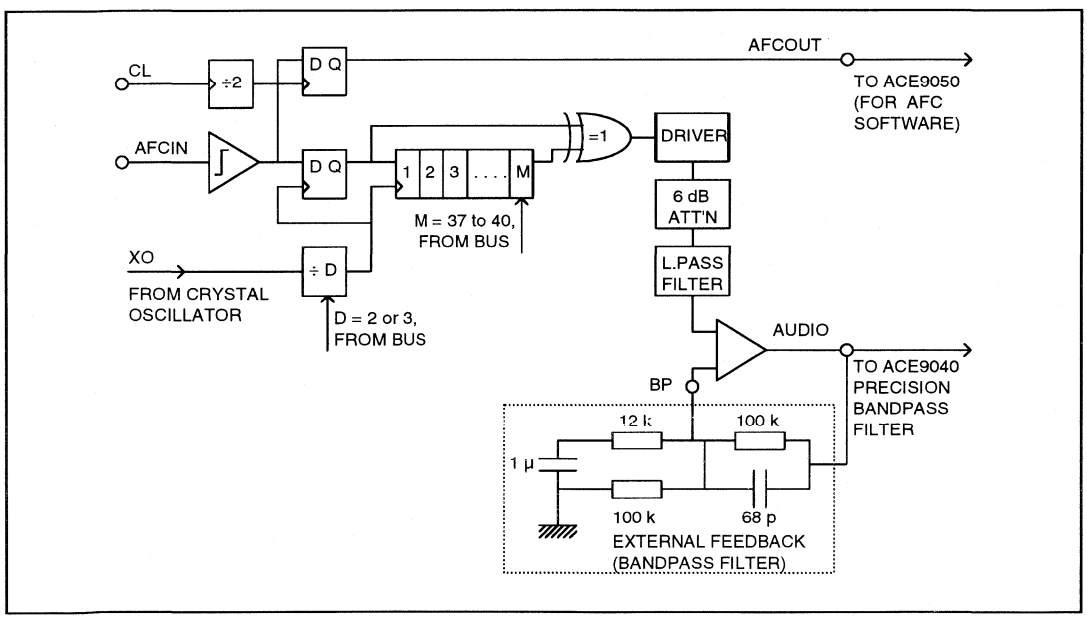


Fig. 18 Audio Discriminator And AFCOUT Circuit

The input signal to the pin AFCIN is approximately a squarewave from the second (final) I.F. amplifier-limiter at 450 or 455 kHz and is A.C. coupled to the pin through a capacitor of typically 1 nF to drive a Schmitt trigger and become a logic signal. This signal carries the received modulation - speech, SAT and signalling data. AFCIN is first amplified and limited and then processed in two separate paths as in figure 18.

One path samples the input signal at 504 kHz, with a clock generated by a divide-by-two from the CL clock. This sampling gives a mixed-down output AFCOUT at 54 kHz when the input is at exactly 450 kHz and otherwise tracks the offset to allow estimation of the local oscillator error and the crystal error so that an AFC loop can be built to adjust the crystal to exactly the correct frequency. Further details of this feature are given in the APPLICATIONS HINTS section. AFCOUT is also used by the modem in the ACE9050 to receive signalling DATA.

The other path is the audio discriminator which is a purely digital implementation of the delay-and-multiply technique where the exclusive-OR gate acts as a digital multiplier and compares two samples of the AFCIN signal separated by a programmable delay to extract the audio and drive the speech and SAT paths in the ACE9040. The delay length, M, and the crystal divider, D, are both programmable for the various crystal and intermediate frequency choices.

After demodulation the audio is low-pass filtered on-chip to remove the doubled sampling clock and then bandpass filtered to nearer telephone bandwidth by an on-chip amplifier with off-chip feedback components.

The I.F. signal is digitised at a rate set by the crystal in use and by the divider D in figure 18 and so will be in the range 4·267 to 7·680 MHz. These rates are all greater than the maximum audio frequency of 3·4 kHz by a factor of at least 1254 (which is over 2^{10}) and so the quantisation allows better than 63 dB signal to noise ratio in the final audio, even though only single bit quantising is used. The I.F. is oversampled by a much smaller ratio and so will have a smaller signal to noise ratio if measured in its total bandwidth, but this bandwidth is reduced in the demodulation process to give a good audio signal to noise ratio in the system.

To power down the discriminator a Normal command can be used:

DATA1	DATA2	DATA3
xxxxxxxx	01 D_5 xxxxx	xxxxxxxx

where the discriminator is powered down if DATA2:D_5 is LOW or is set active if DATA2:D_5 is HIGH.

The values of the programmable constants D and M are set by a Set-up command, which can also use DATA1 bit D_5 for the lock logic filter period and DATA1 bits D_2, D_1, D_0 for the OSC8 mode programming:

DATA1	DATA2	DATA3
D_7 D_6 xxxxxx	10xxxxxx	xx1xxx00

The two control bits D_7, D_6 set the values for D and M as in table 3. From this table of frequencies and division ratios it is possible to calculate the length of the delay M in terms of cycles of the input I.F. to understand the discrimination process shown in table 4.

It can be seen that a 12·8 or 15·36 MHz crystal will give a delay of a few whole cycles plus or minus one quarter cycle to a very good accuracy and that a 14·85 MHz crystal similarly gives some whole cycles plus or minus an odd third of a cycle.

These non-integer delays are needed because the delays are not locked to the I.F. input on AFCIN, and to get a demodulated output the comparisons must include an edge time, at least for some samples. The odd quarter or third of a cycle ensures that the phase of the start of the delay time will rapidly increase relative to the I.F. signal and so avoid low frequency beats, when the system could sit in the state where a steady part of one cycle is compared with a steady part of another for a long period of time and so give no output.

The accuracy of the delay is not important as a small error will only give a D.C. offset in the output but the delay must be consistant to avoid adding modulation to the output so in the ACE9030 it is derived from the crystal frequency.

The sampling rate must not be a harmonic of the I.F., or very close to one, to prevent the sampling phase becoming synchronised to the signal and so missing all edges, leading to the modulation being lost for long periods of time at the beat frequency (a 14·85 MHz crystal cannot be used in D = 3 mode with an I.F. at 450 kHz as 14·85 MHz ÷ 3 is 4·95 MHz which is 11 × 450 kHz). It cannot be assumed that a sampling rate greater than 4 MHz always meets the Nyquist criterion for the I.F. signal at nominally 450 or 455 kHz because the input signal is often a square wave from a limiting amplifier and if not is converted to a switching logic signal in the Schmitt trigger input buffer giving many significant harmonics. The modulation deviation is up to 14·5 kHz and is multiplied by the harmonic number to give increasingly wide deviation such that the spectrum eventually becomes continuous, but at a low level, for the very high (e.g.17th or above) harmonics. A sampling rate of a few MHz will then retain all required information and allow distortion free demodulation but is undersampling in Nyquist terms so aliasing effects must be avoided by choosing a frequency separated from the nearest harmonic of the I.F. by at least twice the modulation frequency. All combinations given in tables 3 and 4 can safely be used but care is needed if a different crystal or I.F. is required. For example, a 14·4 MHz crystal cannot be used in ÷ 2 mode with a 450 kHz I.F. but ÷ 3 can be used and with an M of 40 will give a delay of 3·75 I.F. cycles and alias-free demodulation.

Sampling the I.F. signal at a rate of only 9·3 to 16·9 times the I.F. will remove the fine detail of the modulation from each individual cycle of the I.F. but the modulation bandwidth is very low (both speech and tones) compared to this sampling rate so the information will be preserved as infrequent whole sample steps, which when averaged over many samples will show the correct modulation.

To explain the operation of the discriminator an example diagram of the sampling points and the comparison delay is given in figure 19, with the effect of modulation on the input shown by fine lines. The increasing separation of these dotted

DATA1 bit D_7	DATA1 bit D_6	Set D	Set M	Intended I.F.	Intended Crystal
0	0	2	39	450 kHz	12·8 or 14·85 MHz
1	0	3	40	455 kHz	12·8 or 14·85 MHz
0	1	3	37	450 kHz	15·36 MHz
1	1	2	38	455 kHz	15·36 MHz

Table 3

D_7, D_6	D	M	Crystal Freq.	Sampling Rate	I.F.	Delay as I.F. cycles
0, 0	2	39	12·80 MHz	6·400 MHz	450 kHz	2·742
0, 0	2	39	14·85 MHz	7·425 MHz	450 kHz	2·363
1, 0	3	40	12·80 MHz	4·267 MHz	455 kHz	4·266
1, 0	3	40	14·85 MHz	4·950 MHz	455 kHz	3·677
0, 1	3	37	15·36 MHz	5·120 MHz	450 kHz	3·252
1, 1	2	38	15·36 MHz	7·680 MHz	455 kHz	2·251

Table 4

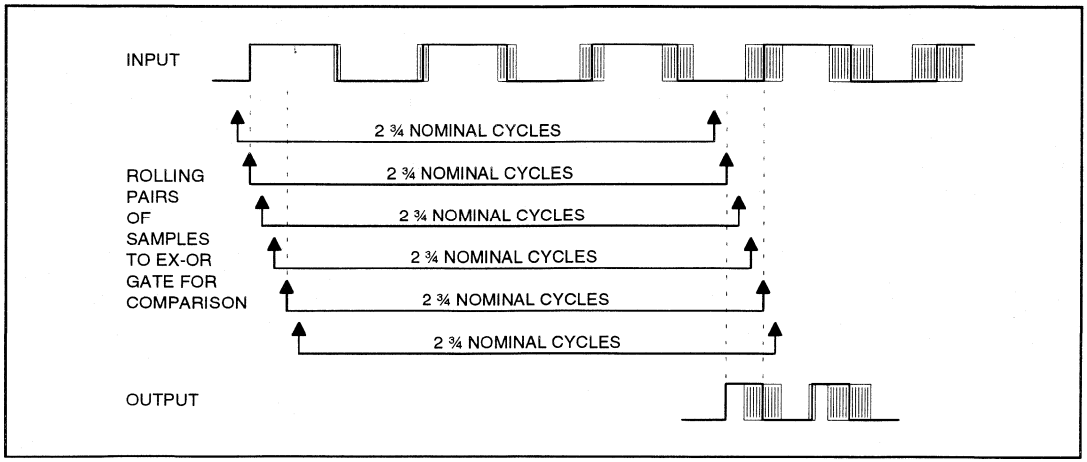


Fig. 19 F.M. Discriminator Example Timing Diagram

lines from the unmodulated position indicates that the total phase effect of f.m. increases as more cycles are examined. The modulation lines are drawn as the phase change on the real input waveform but the separation from the nominal edge position can also be interpreted as the probability of a whole cycle shift on the sampled version of the signal as in the ACE9030.

Only six delay comparisons are shown, stepping across at the sampling rate, but the effect of the pattern can easily be seen by continuing the sequence, and two conclusions can be drawn:

1) The output waveform is at twice the frequency of the input - this is true for all delay-and-multiply schemes.

2) The output high time is modulated by the phase modulation accumulated over the delay duration and the output period is only modulated slightly by the instantaneous input phase shifts so the effect is to modulate the duty cycle. Due to the sampling of the I.F. input the modulation will really be quantised so the width of the modulation box should be read as a probability of a whole cycle shift in edge position rather than as a phase shift but the effect is the same when averaged over many cycles.

By converting the modulation from a phase shift to a duty cycle all that is then needed to recover the original baseband signal is to smooth the discriminator output to remove the 900 kHz sampling, leaving an analog signal proportional to the original frequency deviation and to the delay length. The low-pass filter in ACE9030 is first order and has its – 3 dB point at approximately 70 to 80 kHz to significantly reduce the clock level; tne audio bandpass filter then further reduces this level to give a cleaner audio output to drive the ACE9040 where it is again filtered.

The demodulation gain can be determined by considering the effects of a 1 kHz frequency offset on the input signal, and using I.F. = 450 kHz and Delay = 2·742 cycles and V_{DD} = 3·75 V in the example:

A 1 kHz frequency offset will give a phase change in the I.F. signal, during each cycle, of $2\pi \times$ (1 kHz / I.F.) radians or as a fraction of a cycle, (1 kHz / I.F.) which in this example is 1/450 of a cycle.

If the discriminator delay is measured in I.F. cycles the change in output pulse width for each of the two output pulses is: (Delay in cycles) x (phase change per cycle) = Delay x (1 kHz / I.F.) in I.F. periods, which in this example is 2·742 x 1/450 periods of 450 kHz, or 13·5 ns.

Output pulses occur at a rate of 2 x I.F., so the change in output pulse width measured in output periods is 2 x (change measured in I.F. periods), giving 2 x Delay x 1 kHz / I.F. The duty cycle is defined as pulse width / period so the result is also the change in duty cycle. For this example the change is 0·012.

The output is a logic signal so its amplitude is V_{DD} for all

D_7, D_6	D	M	Delay as I.F. cycles	I.F. kHz	Absolute Gain in µV/Hz, V_{DD} = 3·75 V.	Absolute Gain in µV/Hz, V_{DD} = 4·85 V.	Relative Gain
0, 0	2	39	2·742	450	45·7	59·1	1·8 dB
0, 0	2	39	2·363	450	39·4	50·9	0·5 dB
1, 0	3	40	4·266	455	70·3	90·9	5·6 dB
1, 0	3	40	3·677	455	60·6	78·4	4·3 dB
0, 1	3	37	3·252	450	54·2	70·1	3·3 dB
1, 1	2	38	2·251	455	37·1	48·0	0 dB

Table 5

settings and for all modulation, thus the final effect of a 1 kHz offset is an output change of 2 x Delay x 1 kHz x V_{DD} / I.F. and the example gives 0·045 V.

Removing the arbitrary 1 kHz, the gain at the exclusive-OR gate is given by:

Gain = 2 x Delay in I.F. cycles x V_{DD} / I.F.
with the units of volts per Hertz of deviation.

To be strict, the pulse width is reduced for a positive deviation, so the gain is negative, but this may be ignored as the audio polarity is not of any relevance and also is inverted several times before driving the earpiece.

Using the delay lengths from table 4 the range of gains (at the exclusive-OR gate) can be listed and then compared with the lowest as shown in table 5.

This shows a gain range of 5·6 dB which must be allowed for in the later stages, but also gives absolute gains which show the discriminator could cause saturation in the following stage if a high deviation signal is received. For example speech can be set to 8 kHz deviation so the maximum voltage (with V_{DD} at 3·75 V) is 70·3 x 8000 µV = 562 mV peak. With ST and SAT the total deviation can become 14·5 kHz, potentially giving 1·019 V peak signal, or over 2 V peak-to-peak and leading to possible saturation. There is also the full V_{DD} switching waveform to handle. Other supply levels will simply scale the signals and not change the saturation problem. A 6 dB attenuator is included in the low pass filter that follows the discriminator output driver to avoid any possibility of saturation in the audio reconstruction filter. This attenuator is a simple 2:1 potential divider so will also halve the D.C. level of the signal.

A further effect to be considered is the D.C. offset that results from using delays that are not ideal multiples of cycles of the AFCIN frequency. It can be seen from the Timing Diagram, figure 19, that when the delay is exactly an odd number of quarter cycles each half cycle at one end of the delay will symmetrically straddle an edge the other end of the delay so an unmodulated input will give an output with a 1:1 mark:space ratio; this corresponds to a mid-supply level at the attenuator input, see figure 20. The attenuator output will then be centred at $V_{DD}/4$, so the nominal D.C. gain, 2 x, of the bandpass filter will give the AUDIO output centred at mid-supply.

When a mode is selected with an odd number of thirds of a cycle the output mark:space ratio is offset, and approximating 2·363 as $^{7}/_{3}$ or 3·677 as $^{11}/_{3}$ the effect can be seen in figure 21.

The signal will now be centred on a level at $^{2}/_{3}$ or $^{1}/_{3}$ of supply, at the attenuator input (giving $^{1}/_{3}$ or $^{1}/_{6} \times V_{DD}$ at its output) and by adjusting the D.C. gain of the bandpass filter it is possible to set the AUDIO to a mid-supply centre if required.

The components used in the bandpass filter feedback circuit should be chosen to both set the pass band frequencies (for example 50 Hz to 30 kHz) and also to set the A.C. and D.C. gains to complement the discriminator's gain and D.C. offset. Typcal A.C. gain at mid-band is around 20 dB. This filter is not of high enough order to remove all out of band noise without distorting the speech channel so to get the final band limited signal precision high order filters such as in the ACE9040 are required.

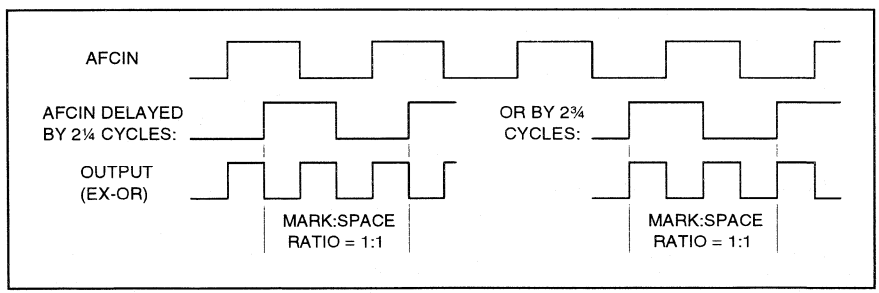


Fig. 20 Demodulation With Odd Number Of Quarter Cycles

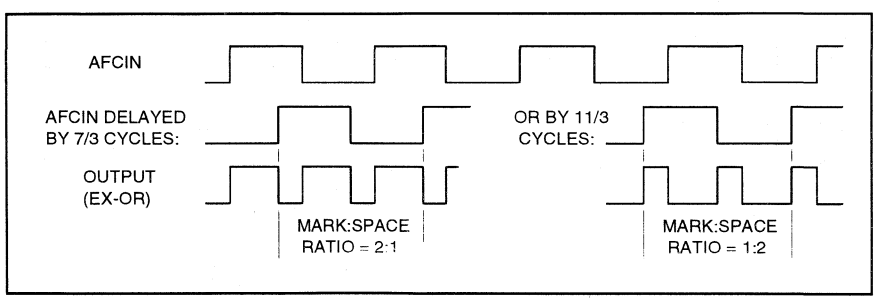


Fig. 21 Demodulation With Odd Thirds Of A Cycle

FUNCTIONAL DESCRIPTION - BLOCKS IN THE SYNTHESISERS

There are two synthesisers in the ACE9030 for use by the radio system, a Main loop to set the first local oscillator to the frequency needed for the channel to be received and an Auxiliary loop to generate an offset frequency to be mixed with the Main output to give the transmit frequency. The modulation is added to the Auxiliary loop by pulling the VCO tank circuit and is then mixed onto the final carrier frequency. In a typical cellular terminal the first Intermediate Frequency is 45 MHz so the Main synthesiser will be set 45 MHz above the receive channel frequency. Many cellular systems operating around 900 MHz use a 45 MHz transmit-receive offset, with the mobile transmit channel below the receive channel frequency so the Auxiliary synthesiser will be set to a fixed frequency of 90 MHz.

Loop dynamics needed for the Main synthesiser are set by the re-tuning time during hand-off and to help simplify the off-chip loop filter components there are Fractional-N and Speed-up modes available for this synthsiser, primarily for use in ETACS terminals. The Auxiliary loop does not change frequency so the only constraints are power-up time and microphonics, so a simple synthesiser is used.

The two loops share a common reference divider to save power and also to control the relative phase of the two sets of charge pumps.

As described in the section FUNCTIONAL DESCRIPTION - CONTROL BUS there is often benefit in holding LATCHC at a high level to minimise bus clock interference to the synthesiser loops. The dummy word in figure 11 is the preferred technique to set LATCHC to high for normal operation.

At power-on, the reset generator in the Radio Interface section is used to initialise both synthesisers to their power down state. In this state they can be programmed with required numbers to be ready for power-on when the whole terminal has fully initialised.

Reference Divider

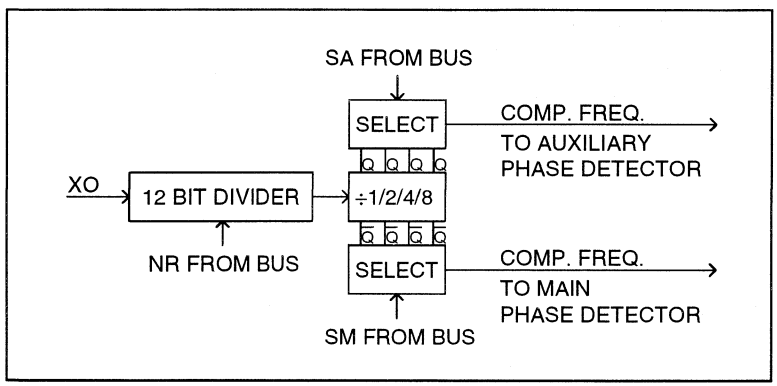


Fig. 22 Reference Divider

A common reference divider is used for the two synthesisers, but to allow some difference in comparison frequencies the final four stage output selectors are repeated for each synthesiser as shown in figure 22. To reduce interaction between the two synthesisers the divider outputs are arranged in antiphase so that loop correction charge pump pulses occur alternately in each loop. This phase separation also reduces the peak current in the charge pump power supply and can reduce interference to other sections of the mobile terminal.

The input clock to the reference divider is the internal signal XO from the crystal oscillator. The two outputs drive the Auxiliary and the Main phase detectors directly.

A standby mode is available for the reference divider and is enabled whenever both synthesisers are in standby.

The programming numbers are all loaded from the serial bus in Word D, NR directly sets the ratio of the 12 bit divider but SA and SM select the final divisions as in the following tables:

SA bit 1	SA bit 0	Auxiliary Tap
0	0	÷1
0	1	÷4
1	0	÷2
1	1	÷8

SM bit 1	SM bit 0	Main Tap
0	0	÷1
0	1	÷4
1	0	÷2
1	1	÷8

The minimum allowed value of NR is set by the need to generate some small time windows around the comparison edges for Lock Detect logic and for Fractional-N compensation so a value of at least 8 is required. The maximum NR is 4095 as normal for a 12 bit counter and this is then increased by a factor of 1, 2, 4, or 8 in the final divider. A typical required reference division is ÷512 so neither of these limits should constrain the system design.

Auxiliary Synthesiser

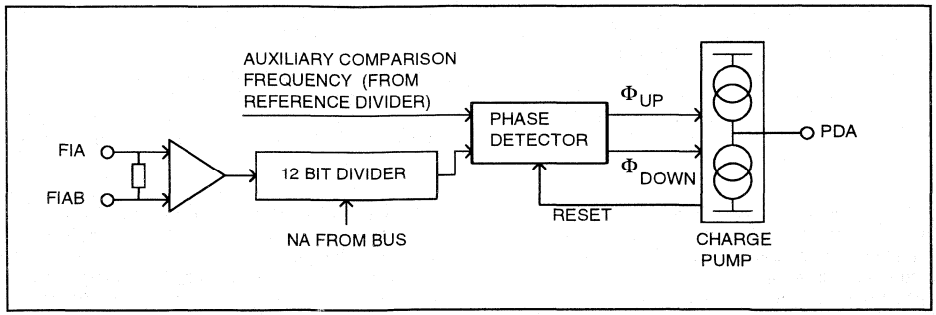


Fig. 23 Auxiliary Synthesiser

The Auxiliary Synthesiser operates with an input frequency up to 135 MHz. The input buffer will amplify and limit a small amplitude sinewave signal and so can be driven from the ACE9020 VCO directly. There are three main blocks in this synthesiser: a 12-bit programm-able divider, a digital phase detector, and output charge pumps to drive a passive loop filter.

To assist fast recovery from power-down the inputs FIA and FIAB are designed to be d.c. driven by the TXOSC+ and TXOSC– outputs from ACE9020.

FIA can also be used single-ended if it is driven by a signal with double amplitude, the correct d.c. level and if FIAB is decoupled to ground by a capacitor (see Electrical Characteristics for full details). Internal biasing will set the d.c. level on FIAB.

The 12 bit programmable divider is set by the NA bits in Word C and ratios from 3 to 4095 can be used. This drives the phase detector along with the comparison frequency signal from the common reference divider.

A digital phase detector is used and is designed to eliminate any deadband around the locked state, this is especially important when modulation is added.

The phase detector drives switched current sources to pump charge onto an external passive loop filter which is primarily an integrator, resulting in the minimum of external components. The charge pump output current level is set by the external resistor on pin RSMA and the ratio is fixed so that nominal $I_{AUX} = 8 \times I_{RSMA}$. This bias resistor also sets the main synthesiser output current but that current has a programmable ratio to enable different currents for each loop. The pin RSMA does not need any decoupling and to avoid all possibilities of oscillation the external capacitance should be less than 5 pF.

The polarity of the output is such that a more positive voltage on the loop filter (PDA pin) sets a higher VCO frequency.

A standby mode for the auxiliary synthesiser can be selected if bit DA in Word D is HIGH.

This synthesiser is used to add modulation to the transmitted signal. The most convenient approach, as shown in figure 31, is to drive the positive end of the varactor diode in the tank circuit with the loop filter to set the frequency and then to drive the negative end with the modulation from a summing circuit (speech plus SAT plus data or ST) from ACE9040.

Main Synthesiser

The main synthesiser in the ACE9030 is designed to operate with a two-modulus prescaler and will accept frequencies up to 30 MHz. To assist fast recovery from power-down the inputs FIM and FIMB are designed to be d.c. driven by the DIV_OUT+ and DIV_OUT– outputs from the ACE9020 or similar outputs from standard prescalers.

FIM can also be used single-ended if it is driven by a signal with double amplitude, the correct d.c. level and if FIMB is decoupled to ground by a capacitor (see Electrical Characteristics for full details). Internal biasing will set the d.c. level on FIMB.

The block diagram depends on which mode is selected but is basically the same as the Auxiliary synthesiser with added features for each mode. The common element is the phase detector, which is the same circuit used in the Auxiliary synthesiser and again drives switched current sources to pump charge into an external passive loop filter to minimise the external components. The charge pump output current level is set by the external resistor on pin RSMA and the multiplying ratio is programmable by the bus and the chosen mode as in table 6. This bias resistor also sets the Auxiliary synthesiser output current as described above.

A standby mode for the main synthesiser can be selected if bit DM in Word D is HIGH.

The Main synthesiser can be used in different modes depending on the requirements of the communication system it is operating in:

Normal mode

The most straightforward to use and adequate for most analogue cellular telephone systems.

Normal Mode with Speed-up

This adds a fast slew drive to the loop filter during channel changes so that the time from channel to channel is significantly reduced but once the change is expected to be complete the loop reverts to normal mode. A little care is needed in parameter choice and loop filter design to ensure the loop is stable in both modes and there is likely to be a higher level of comparison sidebands during speed-up mode. This combination offers a faster channel change or a lower level of comparison frequency sidebands once on channel, or with care some of each advantage.

Fractional-N mode

When selected this mode is permanently active and by interpolating channels between comparison frequency steps allows a higher comparison frequency to give both a faster channel change time and a lower comparison sideband level. The higher comparison frequency also allows a higher loop bandwidth which can reduce phase noise in the locked system. It is not difficult to get the Fractional-N loop compensation correct to minimise sidebands at the fractional frequency as the ACE9030 fractions are only $^1/_5$'s or $^1/_8$'s. For further details see the later section "Detailed Operation of Fractional-N Mode".

Fractional-N Mode with Speed-up

This gives the ultimate loop performance from the ACE9030 but care is needed when designing the loop filter and when choosing the values of the control parameters.

Main Synthesiser - Normal Mode

In Normal mode the Main synthesiser is similar to the Auxiliary synthesiser with the addition of control for an external prescaler, see figure 24.

The 12-bit counter first counts down for N1 cycles, with MODMP set HIGH, then counts up for N2 cycles, with MODMP set LOW, and finally gives an output pulse (every N1 + N2 cycles) to the phase comparator and repeats the whole sequence. The use of an up/down counter allows the control of a two modulus prescaler without needing a separate counter for that purpose. To give time for the function sequencing a minimum limit of 3 is put on N1 and a programmed value of 0 for N2 will be treated as 256 and so is not normally used. Choices of values for N1 and N2 are described in the later sections "Two Modulus Prescaler Control" and "Programming Example for Both Synthesisers".

The phase detector operates with the same arrangement of overlapping up and down pulses as the Auxiliary phase detector to again avoid any dead band, the charge pump current is also set by the same resistor on pin RSMA but for the Main charge pumps the current is also controlled by the bus. In the bias circuit the current I_{RSMA} through the external resistor on pin RSMA is divided by 32 to give a reference current Ibo ($Ibo = I_{RSMA} \times {}^1/_{32}$) and this current is then multiplied by the value CN from the control bus to give the normal charge pump current Iprop(0). The pin RSMA again does not need any decoupling and to avoid all possibilities of oscillation the external capacitance should be less than 5 pF.

CN can be changed for different channels, to track the division ratio set by N1 and N2, to maintain the same PLL loop gain over the operating band but in most cellular systems the total band is narrow compared to the frequencies and a fixed CN is adequate. Other synthesiser control parameters do not need changing and could be loaded at power-on and then left unaltered.

Main Synthesiser - Normal Mode withSpeed-up

During Speed-up the drive to the loop filter is increased to change channels faster. There will be a slight degradation of sideband performance during the change but this does not affect the final system performance. Speed-up lasts for the duration of the LATCHC pulse that loads an A or A2 word from the bus and as soon as the pulse ends the currents return to normal to give clean synthesis. The normal charge pump current is increased by a factor (2^{L+1}) to give 2, 4, 8, or 16 times Iprop(0), as defined in Normal Mode, and is then referred to as Iprop(1), as in figure 26. A second charge pump is enabled to drive the capacitor Ci in the loop filter directly, and as this is always larger than capacitor Cp this extra output is set to Iprop(1) x K. The factors L and K are used to control speed-up and are loaded at power-up and can be left at fixed values.

Speed-up is always enabled by LATCHC when an A or A2 word is loaded. When speed-up is not required the LATCHC pulse should be short and the parameters L and K set to their minimum to give an insignificant effect.

Main Synthesiser - Fractional-N Mode

Fractional-N mode is the same as Normal mode with the addition of the Fractional-N system, shown in figure 25.

In Fractional-N mode the modulus of the prescaler is changed in a cyclic manner to interpolate channels between the comparison frequency steps. Depending on the state of the FMOD bit loaded in Word D the pattern can be 5 (FMOD = 0) or 8 (FMOD = 1) cycles long, giving the choice of $^1/_5$'s or $^1/_8$'s of the comparison frequency and the fractional numerator is set by NF in Word A or A2. The accumulator repeatedly adds NF to its own value and generates an overflow whenever this value exceeds the count modulo number. This overflow output to the Modulus Control logic will force one cycle to change from MODMP HIGH to MODMP LOW to in turn set the prescaler to the higher ratio for one

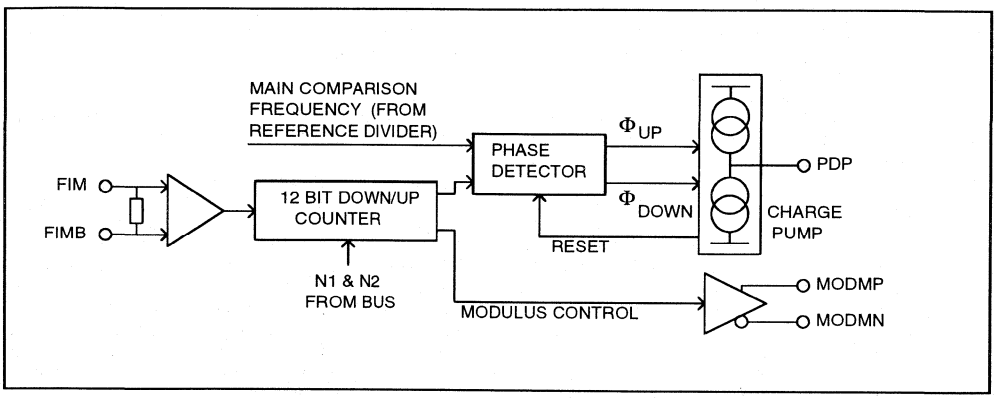


Fig. 24 Main Synthesiser - Normal Mode

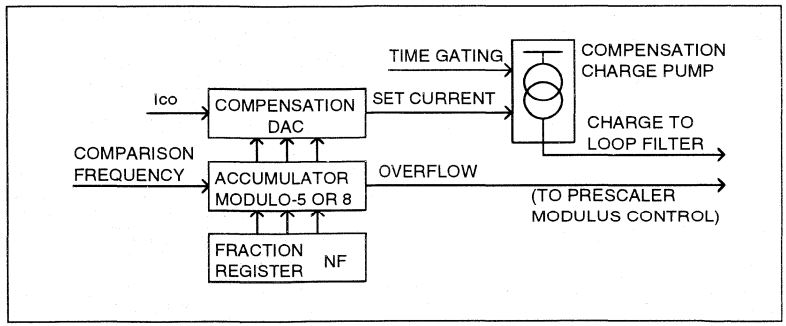


Fig. 25 Fractional-N Add-On To Main Synthesiser

cycle and so increment the total division.

To avoid loop modulation due to the accumulating phase shift at the fractional frequency, a compensation charge must also be driven onto the loop filter to track the accumulated phase error so a current Icomp(0) is output on PDP for a fixed short duration. Icomp(0) is given by Icomp(0) = ACC × Ico, where ACC is the value of the phase accumulator and Ico is a current set by a resistor on pin RSC such that Ico = I_{RSC}/320. In a typical system the required value of Ico is between $^1/_{10}$ and $^1/_3$ of Ibo and thus the resistor on RSMA has a value between one and three times the value of the resistor on RSC. As with RSMA, the pin RSC does not need any decoupling and to avoid all possibilities of oscillation the external capacitance should be less than 5 pF. For a full description of this mode see the later section "Detailed Operation of Fractional-N Mode".

In fractional-N mode a zero fraction numerator, in both $^1/_5$'s and $^1/_8$'s mode, will force the accumulator to zero and not simply leave it at an arbitrary fixed value. This feature makes testing easier by setting the accumulator to a known state, but is also useful in operation by stopping all compensation pulses when none are needed. Similarly in $^1/_8$'s mode if $^1/_4$ (and $^3/_4$) or $^1/_2$ fractions are set then the LSB or two LSB's in the accumulator will be forced to zero to relax the tolerance on the compensation.

Main Synthesiser - Fractional-N Mode with Speed-up

In Fractional-N mode with Speed-up the normal compensation current is increased by the same factor (2^{L+1}) as the main charge pump current to give Icomp(1), and at the same time the integrating capacitor is also driven with a compensating charge by a current Icomp(2) set to Icomp(1) × K. This extra compensation is included so that the loop will step to exactly the desired frequency during the Speed-up phase and then be on channel when normal Fractional-N begins.

Main Synthesiser Charge Pumps

The charge pumps for all modes are shown together in figure 26. The charge pumps on pin PDP are used normally to hold a channel and are also used in speed-up modes at a

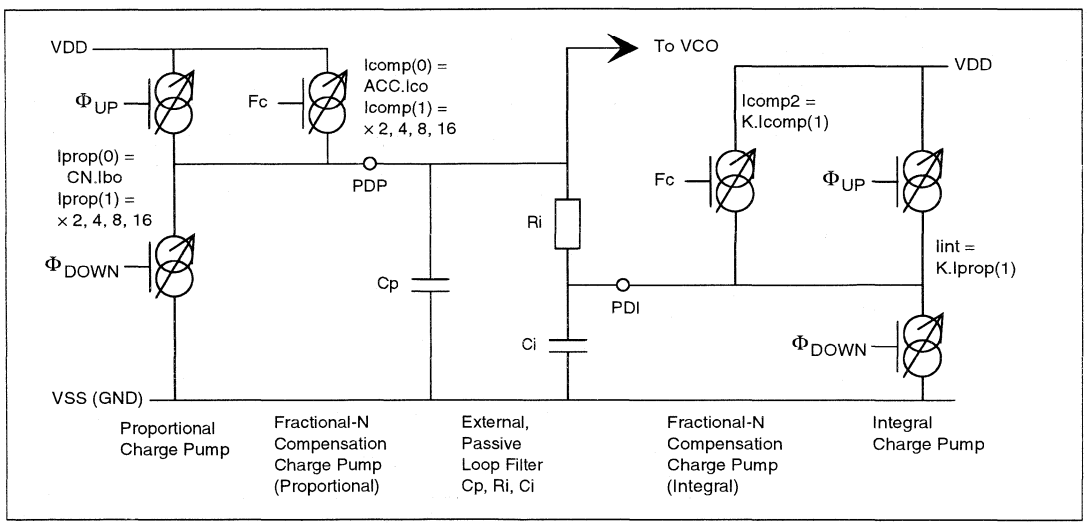


Fig. 26 Main Synthesiser Charge Pumps

larger current. The charge pumps on PDI are only used in speed-up and then drive the integrating capacitor Ci directly. The control signals $Ø_{UP}$ and $Ø_{DOWN}$ are the error signals fron the phase detector and have a duration proportional to the phase error, the signal Fc is the Fractional-N compensation gating pulse and has a fixed duration set by the crystal oscillator.

Nominal Charge Pump Currents

Shown in table 6, charge pump currents are set by the resistors RSMA and RSC and by scaling coefficients loaded from the serial bus. CN is an 8 bit number, L is 2 bit and K is 4 bit. Fractional-N compensation also depends on the instantaneous value ACC in the fractional accumulator, a 3 bit number.

Pin	Charge pump	Normal	Speed-up	Maximum setting*
PDP	Main	$Iprop(0) = CN \times I_{RSMA}/32$	$Iprop(1) = 2^{L+1} \times Iprop(0)$	1·0 mA
PDI	Main	Off	$Iint = K \times Iprop(1)$	5 mA
PDP	Fractional-N	$Icomp(0) = ACC \times I_{RSC}/320$	$Icomp(1) = 2^{L+1} \times Icomp(0)$	12 µA
PDI	Fractional-N	Off	$Icomp(2) = K \times Icomp(1)$	180 µA
PDA	Auxiliary	$Iauxil = 8 \times I_{RSMA}$	no auxiliary speed-up	512 µA

* Larger values of current can be set by the programming numbers and the resistor values, but the circuit is not then guaranteed to give the calculated current.

Table 6

Two Modulus Prescaler Control

The Main ACE9030 synthesiser is designed to operate with the two-modulus prescaler section of the ACE9020. This allows channels to be spaced at the comparison frequency while keeping the clock rates within the range possible in CMOS. ACE9030 can also be used with standard two-modulus prescalers such as SP8715.

The prescaler will have two division ratios, R1 and R2, selected by a Modulus Control signal and designed to switch quickly from one ratio to the other so that a sequence of R1 and R2 can be used to give the required total division. It is usual to have R2 = R1 + 1 and to select R1 by setting Modulus Control to the HIGH state and R2 by a LOW state.

To reduce interference the Modulus Control output from ACE9030 is a pair of differential signals MODMP and MODMN each with a limited voltage swing but still able to drive selected standard prescalers from GEC-Plessey Semiconductors if MODMP is used alone. Even if a prescaler with non-differential control input is used there could still be some benefit in running a MODMN track on the circuit board beside the MODMP track to partly cancel capacitive coupling to sensitive nodes. Simplified waveforms are shown in figure 27.

Unlike many conventional synthesisers that use two separate counters, to give both the total count, M, and the portion for which the prescaler is at its higher ratio, A, there is only one counter in the ACE9030 for both these functions. This counter is loaded with the value N1, counts down to zero, changes direction, counts up to N2, is again loaded with the value N1 and changes direction to down, and so the cycle is repeated indefinitely. As a comparison with conventional synthesisers (N1 + N2) replaces M and N2 replaces A.

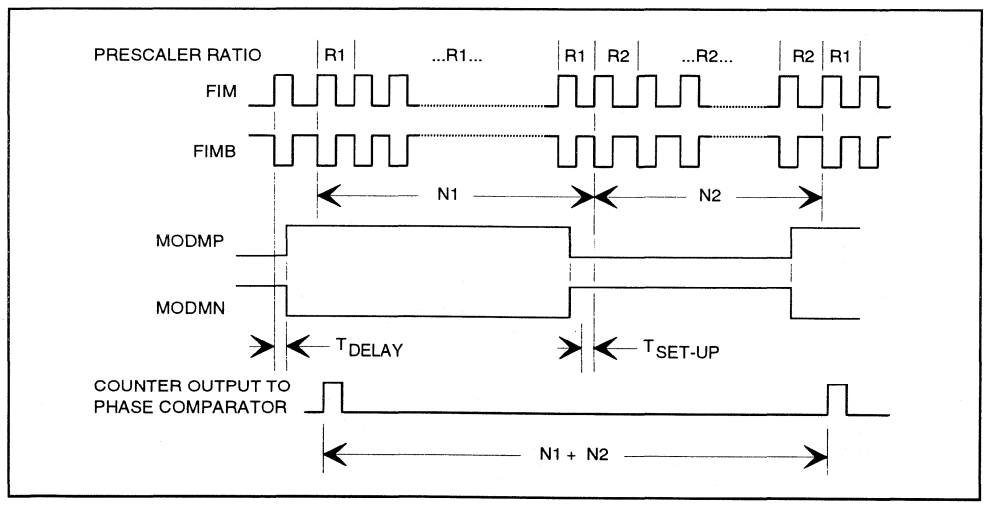


Fig. 27 Modulus Control Timing Diagram

An output to drive the phase comparator is generated from the N1 load signal at the start of each cycle, giving a pulse every (N1 + N2) counts and to help minimise phase noise in the complete synthesiser this pulse is re-timed to be closely synchronised to the FIM/FIMB input. During the N1 down count the modulus control MODMP is held HIGH to select prescaler ratio R1 and during the N2 up count it is LOW to select R2, so the total count from the VCO to comparison frequency is given by:

$$N_{TOT} = N1 \times R1 + N2 \times R2$$

but $R2 = R1 + 1$

so $N_{TOT} = (N1 + N2) \times R1 + N2$

It can be seen from this equation that to increase the total division by one (to give the next higher channel in many systems) the value of N2 must be increased by one but also that N1 must be decreased by one to keep the term (N1 + N2) constant. It is normal to keep the value of N2 in the range 1 to R1 by subtracting R1 whenever the channel incrementing allows this (i.e. if N2 > R1) and to then add one to N1. These calculations are different from those for many other synthesisers but are not difficult.

The 12-bit up/down counter has a maximum value for N1 of 4095 and to give time for the function sequencing a minimum limit of 3 is put on N1. There is no need for such large values for N2 so its range is limited by the programming logic to 8 bit numbers, 0 to 255 and to simplify the logic a set value of 0 will give a count of 256. If a value of 0 for N2 is wanted then N2 should be set instead to R1 and the value of N1 reduced by (R1 + 1), also equal to R2.

To ensure consistent operation some care is needed in the choice of prescaler so that the modulus control loop has adequate time for all of its propagation delays. In the synthesiser there is propogation delay T_{DELAY} from the FIM/FIMB input to the MODMP/MODMN output and in the prescaler there will be a minimum time T_{SET-UP} from the change in MODMP/MODMN to the next output edge on FIM/FIMB, as shown in figure 27. For predictable operation the sum $T_{DELAY} + T_{SET-UP}$ must be less than the period of FIM/FIMB or otherwise, if the rising and falling edges of MODMP/N are delayed differently, the prescaler might give the wrong balance of R1 and R2. This will often set a lower limit on the frequency of FIM than that set by the ability of the counter to clock at the FIM rate. For 900 MHz cellular telephones the use of a ÷ 64/65 prescaler normally ensures safe timing.

Fractional-N mode operates by forcing the MODMP/MODMN outputs to the R2 state for the last count of the N1 period whenever the Fractional-N accumulator overflows, effectively adding one to N2 and subtracting one from N1, and so increases the total division ratio by one for each overflow. The effect of this is to increase the average division ratio by the required fraction.

PROGRAMMING EXAMPLE FOR BOTH SYNTHESISERS

To Illustrate the choice of programming numbers consider the ETACS system as now used in the UK.

This began as TACS with 600 channels (numbered 1 to 600) from 890 to 905 MHz (mobile transmit) with the provision to expand by 400 channels (601 to 1000) from 905 to 915 MHz. This additional spectrum was given over to GSM use before TACS needed expanding, so TACS was later extended by 720 extra channels from 872 to 890 MHz, to form ETACS and leaving a somewhat odd channel numbering system. The channel numbers are stored as 11-bit binary numbers and are listed here as both negative numbers to follow on downwards from channel 1 and also as large positive numbers as these are the preferred names. These two numbering schemes are really the same, as the MSB of a binary number can be interpreted as either a sign bit (2's complement giving the negative values) or as the bit with the highest weight (1024 for an 11 bit number, giving the large positive values).

Each channel is 25 kHz wide but as the channel edges are put onto the whole 25 kHz steps the centre frequencies all have an odd 12·5 kHz. This is not ideal for the synthesiser but does give the maximum number of channels in the allocated band.

The mobile receive channels are a fixed 45 MHz above the corresponding transmit frequency, as is the case with most cellular systems. In the ACE9030 the intention is to use the main synthesiser to generate the receiver local oscillator at the first I.F. above the mobile receive carrier, and to then mix the auxiliary synthesiser frequency with this to produce the transmit frequency. A typical I.F. is 45 MHz, leading to an auxiliary frequency of 90 MHz and a crystal of 14·85 MHz with a tripler for the second local oscillator, and a final I.F. of 450 kHz.

The channel numbers and corresponding frequencies are shown in table 7.

CHANNEL NUMBER	MOBILE TRANSMIT FREQUENCY (MHz)	MOBILE RECEIVE FREQUENCY (MHz)	MAIN VCO (MHz)
1329 or –719	872·0125	917·0125	962·0125
...	...	...	...
2047 or –1	889·9625	934·9625	979·9625
0	889·9875	934·9875	979·9875
1	890·0125	935·0125	980·0125
2	890·0375	935·0375	980·0375
3	890·0625	935·0625	980·0625
...	...	...	...
600	904·9875	949·9875	994·9875

Table 7

The reference divider needs to produce the main comparison frequency of 12·5 kHz from the crystal at 14·85 MHz, a ratio of 1188, which can be formed by a NR of 1188 followed by a SM select giving ÷1, or 594 followed by ÷2, or by 297 and ÷4. The auxiliary divider must divide 90 MHz down to the auxiliary comparison frequency, which is related to the main comparison frequency but can usefully be larger. Using 12·5 kHz needs a ratio of 7200 which is too large a value for NA, 25 kHz needs 3600 and could be used, but 50 kHz and a ratio of 1800 helps to minimise loop filter size. With this choice the values to be set are:

NR = 297, to give 50 kHz into SA, SM selector.
SA = 00, to give ÷1, and leave 50 kHz for auxiliary comparison frequency.
SM = 01, to give ÷4, and hence 12·5 kHz for main comparison frequency.
NA = 1800, to give 90 MHz.

In this example Fractional-N operation is not chosen, but if it is required then SM should be set to 00 to give 50 kHz comparison frequency in both synthesisers and then fractions of $^1/_4$ or $^3/_4$ used by setting NF = 2 or 6, with FMOD set to 1 to give $^1/_8$'s. The values of N1 and N2 can then be found by following a procedure similar to the following.

For the main synthesiser, starting at channel 1, to divide 980·0125 MHz down to 12·5 kHz is a total ratio of 78401 and this will be split between the prescaler and the ACE9030 programmable divider. A ÷64/65 prescaler is most common, and will be in ÷64 mode as its normal state, so the 78401 can be split into a ÷64 followed by ÷1225 with a remainder of 1. The remainder is achieved by setting the prescaler to ÷65 for 1 cycle, so using R1 = 64, and R2 = 65 the programmable values can be:

$$N2 = 1, \text{ and } (N1 + N2) = 1225, \text{ thus } N1 = 1224$$

These values are suitable for use but are not the only possible set - if desired N2 can be increased to 65 if N1 is reduced to 1160. The actual choice in practice is set by whichever gives the more convenient mathematics in the system controller, the only limits are the basic equation: $N_{TOT} = (N1 + N2) \times R1 + N2$, which must be met for all channels and the fact that a set value of 0 for N2 will actually give a count of 256 so for easy calculations $N2 \neq 0$ (in practice for a TACS system not using Fractional-N all N2 values are odd numbers so 0 is never needed).

Other channels can easily be added, without forgetting that each channel is two comparison steps (2 × 12·5 kHz) above the next lower, so for channels 1 to 32,

$$N2 = 2 \times \text{Channel Number} - 1, \text{ and } N1 = 1225 - N2$$

and for channels 33 to 64,

$$N2 = 2 \times (\text{Channel Number} - 32) - 1, \text{ and } N1 = 1226 - N2$$

Rather than having several sets of separate equations for each group of channels it is possible to combine them all into one set by adding two variables to split the channel number into a modulo-32 and a remainder number. Let C32 = int((Channel Number − 1) ÷ 32), where "int(x)" means the integer part of (x), and let CN2 = Channel Number − (32 × C32), then:

$$N2 = (2 \times CN2) - 1, \text{ and } N1 = 1225 - N2 + C32$$

These are clearly valid for channels 1 to 600 (the original TACS channels) but to cover the extra channels for ETACS the negative numbers need more processing to avoid negative N2 values. The simplest answer is to add an offset to the channel number and then subtract an equivalent value from the N1 equation. As the channels are in blocks of 32 for the calculations it is helpful to choose a multiple of 32 for the offset, and the most negative channel is −719 so the lowest suitable offset value is 736 (that is 23 × 32). This gives the following steps for all TACS/ETACS channels:

CNOFF = Channel Number + 736
CB32 = int((CNOFF − 1) ÷ 32)
CN2 = CNOFF − (32 × CB32)
N2 = (2 × CN2) − 1
N1 = 1202 − N2 + CB32

These operations are given in easy to understand stages but in a real system it could be more efficient to combine or rearrange some steps. If a high level language is used then integer and remainder functions might be available and could save a little programming time, whereas if low level or assembler language is used an integer function will need to be built, in this case by a 5 bit right shift to both divide by 32 and to lose the fraction.

It might be noticed that avoiding N2 = 0 was very easy as all values of N2 in this system are odd numbers, due to the 12·5 kHz offset from band edges. Other systems do not have this offset so a little care is needed in choosing constants in the corresponding equations.

DETAILED OPERATION OF FRACTIONAL-N MODE

Without using the Fractional-N mode the loop will lock the VCO frequency, f_{VCO} to the comparison frequency, f_{COMP} at a multiple set by the total division ratio N_{TOT}, where:

$$N_{TOT} = (N1 + N2) \times R1 + N2$$

giving:

$$f_{VCO} = f_{COMP} \times N_{TOT}$$

From these equations it can be seen that if N_{TOT} is an integer the minimum frequency step is f_{COMP}. It is not possible to make a non-integer divider but by alternating the ratio between N_{TOT} and $N_{TOT} + 1$ in a suitable pattern the effect of a fractional increase in N_{TOT} can be achieved. This is called Fractional-N operation.

The control of the pattern of N_{TOT} and $N_{TOT} + 1$ cycles is by an accumulator set to count with a modulus equal to the fractional denominator and which adds the numerator of the fraction every comparison cycle. When the accumulator overflows by its value exceeding the value of the denominator the total division ratio is increased for one cycle. In ACE9030 the choice of denominator is 5 or 8 and is set by the FMOD bit in Word D, the numerator is set by the three NF bits in Word A or A2 and the increase in total division from N_{TOT} to $N_{TOT} + 1$ is done by changing the modulus control signal to the prescaler so that an R1 cycle becomes an R1 + 1 cycle.

As an example of the operation of the accumulator consider FMOD set HIGH to give modulo-8 counting and NF set to 011 to give a $^3/_8$ fraction and the accumulator starting at any arbitrary value as shown in table 8.

From this table it can be seen that the pattern repeats every 8 cycles and that the ratio is incremented for 3 of each 8, giving the desired $N_{TOT} + {}^3/_8$. It can be shown that the pattern always repeats every 8 cycles, or whatever modulus is chosen for all fractions and that the number of $N_{TOT} + 1$ cycles is always the fractional numerator.

By spreading the $(N_{TOT} + 1)$ counts throughout the pattern rather than having them as a continuous block the loop is less

Increment (= NF)	Accumulator value		Division Ratio
	...previous values		
3	5		N_{TOT}
3	0	& overflows	$N_{TOT}+1$
3	3		N_{TOT}
3	6		N_{TOT}
3	1	& overflows	$N_{TOT}+1$
3	4		N_{TOT}
3	7		N_{TOT}
3	2	& overflows	$N_{TOT}+1$
3	5		N_{TOT}
3	0	& overflows	$N_{TOT}+1$
	and so on...		

Table 8

disturbed by the variations in division ratio but there is still some frequency modulation given by the Fractional-N operation. The simplest way to remove this ripple on the synthesiser is to use a lower bandwidth loop filter but this also removes all of the advantage of fast channel change when using Fractional-N, so the method used in ACE9030 is to calculate the waveform of the ripple and then inject a compensation signal onto the loop filter.

Fractional-N Compensation

If the Fractional-N system is operating correctly the synthesiser sets the VCO frequency so that:

$$f_{VCO} = f_{COMP} \times (N_{TOT} + F) \quad . \quad . \quad . \quad . \quad . \quad (1)$$

where F is the fraction given by:

$$F = \frac{NF}{MOD}$$

NF is the fraction set in Word A or A2
MOD is the modulus, 5 or 8

The total division alternates between N_{TOT} and $N_{TOT}+1$ so the frequency seen at the phase comparator will also alternate. This divided signal f_{FRACN} is compared with the uniform comparison frequency f_{COMP} and will give a phase error due to the different periods. There will also be some phase error due to leakage on the loop filter, leading to some correction pulses on the charge pumps to maintain lock, but these will be very small in a well designed synthesiser once the loop is locked, so can be ignored here. For each ÷ (N_{TOT}) cycle:

$$f_{FRACN} = f_{COMP} \times \frac{N_{TOT}+F}{N_{TOT}} = f_{COMP} \times \left(1 + \frac{F}{N_{TOT}}\right)$$

and so the phase error increases each cycle by:

$$\frac{F}{N_{TOT}} \times (f_{COMP}\ \text{Period}) \quad . \quad . \quad . \quad . \quad . \quad (2)$$

This phase error gives an unwanted correction pulse on the $\emptyset_{DOWN}$ output as the VCO frequency is too high for the division ratio in use. The phase error increases as ÷ N_{TOT} cycles follow each other until eventually the accumulator overflows and causes a ÷ (N_{TOT} + 1) cycle.
For each ÷ (N_{TOT} + 1) cycle:

$$f_{FRACN} = f_{COMP} \times \frac{(N_{TOT}+F)}{(N_{TOT}+1)}$$

and in this case the phase error increases in the opposite direction each cycle by:

$$\frac{(F-1)}{(N_{TOT}+1)} \times (f_{COMP}\ \text{Period}) \quad . \quad . \quad . \quad . \quad . \quad (3)$$

This phase error gives an unwanted correction pulse on the $\emptyset_{UP}$ output, as the VCO frequency is too low for the division ratio in use.

Any phase can be considered to be the locked condition so to simplify later calculations the phase given by a ÷ (NTOT + 1) cycle which leaves 000 in the accumulator will be chosen as the locked state and compensation will be added to achieve this. Only unwanted $\emptyset_{DOWN}$ outputs then need to be removed by cancellation and also that the total phase error in any cycle, based on formula (2), is given by replacing F, the fraction required, by the current sum of fractions, which is the value of the accumulator ACC divided by the modulus in use. This replacement is clearly valid if the state of the accumulator is considered when starting from a zero value and then adding the fractional count each cycle until an overflow is reached; when starting from a non-zero value there is some residual phase error from the overflow state so the accumulator still gives the correct phase error. Thus the phase error needing correction on the loop filter is:

$$\textbf{Phase error} = \frac{\textbf{ACC}}{\textbf{N}_{TOT} \times \textbf{MOD}} \times (\textbf{f}_{COMP}\ \textbf{Period}) \quad . \quad . \quad . \quad . \quad . \quad (4)$$

This error could be cancelled by a phase shift on the comparison clock from the reference divider but this is very difficult in practice so the method used in ACE9030 is to add an extra charge pump to the loop filter to directly cancel the pulse given by the normal charge pump due to this phase error. The current given by the proportional charge pump is Iprop(0) in normal mode or Iprop(1) in speed-up mode so taking normal mode first the charge that must be cancelled is:

$$\frac{ACC}{N_{TOT} \times MOD} \times (f_{COMP}\ \text{Period}) \times \text{Iprop}(0) \quad . \quad . \quad . \quad . \quad . \quad (5)$$

This formula could be used as it stands but the circuit can be simplified if it is recalled that Iprop(0) depends on the CN value so that loop dynamics are kept constant over a wide range of frequencies by changing CN in proportion to the total division ratio N_{TOT}. In those systems where CN is held constant the synthesiser is in effect considered to be operating over a narrow frequency band so N_{TOT} can also be considered constant and the following calculations still apply. The value of Iprop(0) is set by a DAC in ACE9030 from the reference current Ibo so that:

$$\text{Iprop}(0) = CN \times \text{Ibo} \quad . \quad . \quad . \quad . \quad . \quad (6)$$

and the value of CN tracks N_{TOT} with a scaling factor SF such that:

$$CN = SF \times N_{TOT}$$

putting both of these equations into formula (5) gives the charge to be cancelled as:

$$\textbf{Charge} = \frac{\textbf{ACC} \times \textbf{SF}}{\textbf{MOD}} \times (\textbf{f}_{COMP}\ \textbf{Period}) \times \textbf{Ibo} \quad . \quad . \quad . \quad . \quad . \quad (7)$$

The value of SF can be found from any channel but to get a quick estimate the highest frequency can be considered as there is a fixed upper limit on CN of 256 so:

$$SF = \frac{CN(max)}{N_{TOT}(max)}$$

Putting suggested typical values into equation (7); $N_{TOT}(max) = 10000$, $CN(max) = 250$, and $MOD = 8$, and then assuming the current flows for the whole comparison period the current to be multiplied by ACC is Ibo / 320. The typical Ibo is only 1 µA so this is a very small current of around 3 nA and would be too small to control accurately and certainly too small for production testing.

The error signal to be cancelled is a narrow pulse at the comparison frequency so the best cancellation of the whole spectrum of the error is also a narrow pulse. It is not practical to generate a variable width pulse to match the error pulse but a fixed width variable amplitude pulse is possible and it can be timed to approximately coincide with the error pulse to give good cancellation.

The compensation current amplitude is also increased by gating it with a small time window and in ACE9030 the gate is set to two cycles of the reference clock which straddle the active edge of the comparison frequency signal to the phase comparator. The total reference division from reference clock to comparison frequency is the programmable divider set by NR in Word D multiplied by 1, 2, 4, or 8 as selected by the SM bits also in Word D and this total may be called R_{MAIN}, so for the compensation current the scaling is $R_{MAIN} / 2$.

The charge needed is still as in equation (7) but the current can be defined as:

$$Icomp(0) = ACC \times Ico \quad . \quad . \quad . \quad . \quad . \quad (8)$$

where, in ACE9030, the compensation reference current Ico is set by an external resistor RSC such that:

$$Ico = \frac{I_{RSC}}{320}$$

but this Ico must be chosen to cancel the error charge in equation (7), and the scaling effect of 2 reference cycles in R_{MAIN} has been derived above, giving:

$$Ico = \frac{SF}{MOD} \times \frac{R_{MAIN}}{2} \times Ibo$$

then removing SF to help evaluate the values needed:

$$Ico = \frac{CN(max)}{MOD \times N_{TOT}(max)} \times \frac{R_{MAIN}}{2} \times Ibo \quad . \quad . \quad . \quad . \quad . \quad (9)$$

this can then be further processed by replacing R_{MAIN} and $N_{TOT}(max)$ by the frequency ratios:

$$R_{MAIN} = \frac{f_{CRYSTAL}}{f_{COMP}} \quad \text{and} \quad N_{TOT}(max) = \frac{f_{VCO}(max)}{f_{COMP}}$$

then when substituting these into equation (9) the f_{COMP} terms cancel leaving:

$$Ico = \frac{CN(max)}{MOD \times f_{VCO}(max)} \times \frac{f_{CRYSTAL}}{2} \times Ibo \quad . \quad . \quad . \quad . \quad . \quad (10)$$

For a typical AMPS cellphone the $f_{VCO}(max)$ for 45 MHz I.F. is 938·97 MHz, $f_{CRYSTAL}$ is 14·85 MHz, MOD is 8 and CN(max) can be assumed to be chosen around 200, giving Ico = 0·198 x Ibo.

Fractional-N Mode with Speed-Up

When Speed-up is active the main proportional charge pumps are run at an increased current and the integral charge pumps are switched on to move the loop filter voltage faster. The phase errors due to Fractional-N mode will be the same as normal once the loop is locked so the compensation pulses must be increased to match the proportional and integral charge pump currents in order to allow a smooth change over to normal mode at the end of Speed-up time. The same 2^{L+1} and K coefficients as used for the proportional and integral charge pump currents are used on the compensation currents so from equation (8):

Normal Mode:

Proportional Compensation Current:

$Icomp(0) = ACC \times Ico$

Integral Compensation Current:

none = off

Speed-up Mode:

Proportional Compensation Current:

$Icomp(1) = 2^{L+1} \times ACC \times Ico$

Integral Compensation Current:

$Icomp(2) = K \times 2^{L+1} \times ACC \times Ico$

Required Accuracy of Compensation

With the compensation scheme used in ACE9030 it is not possible to get perfect cancellation of the loop disturbance by the Fractional-N system due to the mis-match of the pulse shapes leaving some high frequency terms, but if the areas are matched there will be complete removal of the low frequency components and the loop filter can be assumed able to remove higher frequencies.

Typical timing waveforms for the phase error and its compensation are shown in figure 28 for a loop operating in 1/8 s mode (hence MOD = 8), with a VCO at 1 GHz, and a comparison frequency of 100 kHz (hence N_{TOT} = 10,000 and f_{COMP} period = 10 µs) so that each phase error can be found from equation (4) as:

(ACC x 10 µs) / (10,000 x 8) = ACC x 0·125 ns.

If the reference is a 12·8 MHz crystal, it gives a correction pulse duration, two reference cycles, of 2/(12·8 MHz) = 156 ns.

If the charge pump current of 250 µA is set by a CN value of 250 the reference current Ibo from equation (6) is 1 µA and the compensation step current Ico can be found from equation (10) as 0·2 x Ibo = 0·2 µA.

Areas of the error and the compensation pulses, equations (4) and (8) must match to get good low frequency cancellation. Although shown as a very narrow pulse on $Ø_{DOWN}$ the phase error will often appear as a change in size of the pulses on either $Ø_{DOWN}$ or $Ø_{UP}$ which occur to maintain lock. The following calculations would then apply to the changes and give the same final result.

If there was no compensation the $Ø_{DOWN}$ pulses would give sidebands at a level set by the loop filter capacitor values and the VCO gain.

In a typical system the filter proportional capacitor can be 6·8 nF and the VCO could cover 30 MHz in 3 V, giving 10 MHz/V. Assuming for the moment that all error pulses are the same at the level of a mid-range ACC value, say 4, and do

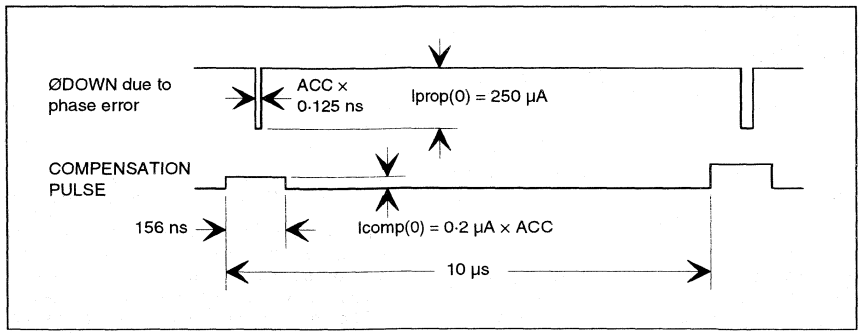


Fig. 28 Fractional-N Phase Error And Compensation Pulse

not ramp in size and that the loop somehow stays on the correct frequency:

Average phase error: = mid-range ACC x 0·125 ns
= 4 x 0·125 ns = 0·5 ns
Charge into filter: Q_{ERR} = 0·5 ns x 250 µA
= 125 fC per pulse
Voltage step: $V_{ERR} = Q_{ERR} \div C_{PROP}$
= 125 fC ÷ 6·8 nF = 18·4 µV
Frequency step: $F_{ERR} = V_{ERR}$ x VCO gain
= 18·4 µV x 10 MHz/V = 184 Hz

This gives a signal with a modulation frequency of 100 kHz with a step deviation of 184 Hz and if the loop is to stay on frequency the waveform must ramp back between steps, giving a sawtooth with an amplitude of ± 92 Hz. Fourier analysis gives the level of the fundamental as (2/π) x peak level, to give 58·6 Hz deviation and hence a modulation index β (peak deviation ÷ modulation frequency) of only 0·000586, putting it well into the narrow band f.m. category. At such small deviations the sideband amplitude is β/2 of the carrier, giving 0·000293 times or – 71 dBc. There will also be higher harmonics present but these will all be at lower levels.

This calculation assumed all phase error pulses are the same, but in reality the size varies in a pattern determined by the fractional numerator (0 to 7) with a period equal to the demoninator (8) times the comparison period. The fractions that give the highest level of output at $^1/_8 \times f_{COMP}$ are $^1/_8$ and $^7/_8$ and with these the phase error changes in seven steps of a staircase waveform until the eighth cycle, when the phase resets and the pattern starts again. The loop will settle to the correct average frequency by adding a d.c. offset for the mean level of the staircase, leading to an error waveform which is approximately a sawtooth wave with a step size of 7 in units of ACC value. The peak deviation is then $^7/_4$ times the previous calculation of ± 92 Hz and the level of the fundamental is again (2/π) x peak level, giving 102 Hz deviation at a frequency now of $^1/_8$ x f_{COMP} (12·5 kHz). β then becomes 102/12500 = 0·00816, giving sidebands at up to 0·00408 times or – 47 dBc.

Compensation pulses are used to cancel the effect of the unwanted phase corrections, and if these match to within 10 % they should give a reduction of 20 dB in the fundemental sideband levels, down to a worst figure of – 67 dBc. The low harmonics will also be adequately cancelled but higher harmonics will be left to the loop filter to remove, and as the bandwidth is set by the comparison frequency at only 8 times the Fractional-N fundamental these harmonics will always be well attenuated.

A typical system specification (AMPS) is – 60 dBc so the harmonic spectrum of the modulation needs to be considered to find the manufacturing margins but if the Fractional-N system is only used to help achieve correct lock times and spurious levels (rather than solve all loop problems on its own) then this example suggests that the compensation is not critical and can give a performance advantage at little cost.

More critical compensation is needed if N_{TOT} is less or if the comparison period is longer, but these cancel if the VCO stays at the same frequency, equation (4). Changing only the comparison frequency in the above example would then give the same 184 Hz deviation. In practice the loop filter capacitor value is likely to also change to match the new comparison frequency giving a peak deviation proportional to the comparison frequency. The modulation index is inversely proportional to the comparison frequency so the final sideband level is not, in practice, much affected by the comparison frequency choice, but the separation from the carrier is affected. This all suggests the above example is not just a spot typical result but will apply over a broad range of systems and allow Fractional-N to be used whenever desired.

APPLICATIONS HINTS

V_{DD} & V_{SS} Supply Pins

All V_{DD} pins must be well decoupled to ground. All V_{SS} pins must be connected through very low impedance lines to the ground point.

Serial Bus

Edge speeds on the serial bus should not be too fast in order to avoid ringing which then can cause significant modulation of the synthesisers, including CLK8.

Loop Filters

Both synthesisers use passive loop filters and typical circuits can be either of these two configurations; the need for the extra roll-off in the right hand circuit is only for the more critical applications.

The loop filter needed is partly set by the application specification and partly by the architectural design of the cellphone. The main synthesiser will need to hop channels at a rate set by the hand-off times of the network and so is well defined. The auxiliary synthesiser is always on the same frequency and so could be a very slow loop to lock but in many systems it will be powered down for as much time as possible to economise on battery use and will then need to power-up and lock quickly, leading to a more complex filter.

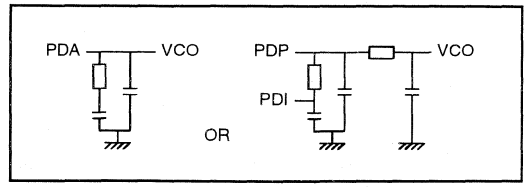


Fig. 29 Typical Synthesiser Loop Filters

The values of the components in these filters may be calculated with the help of appendix AB43 in the Personal Communications Handbook or for a more complete analysis the application note AN94, available from GEC Plessey Semiconductors' Marketing Department, may be used. This note was written specifically for the NJ88C33 synthesiser but the mathematics apply equally well to the ACE9030.

AFC Circuit

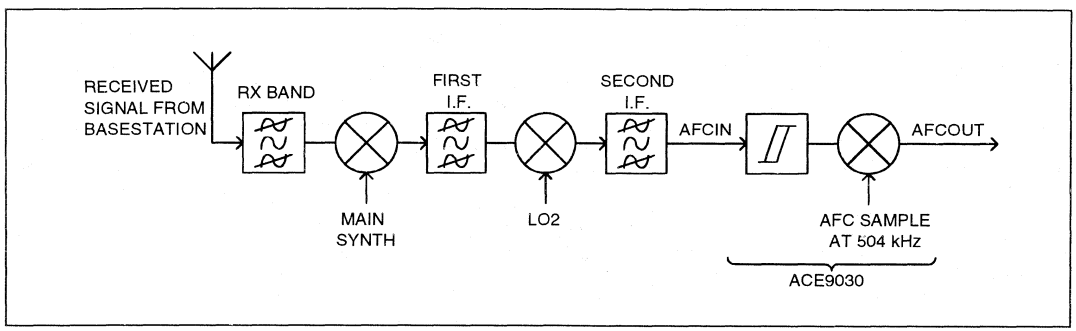


Fig. 30 Simplified Receiver Architecture

In order to fine trim the crystal oscillator frequency to the correct value the ACE9030 includes a sampling circuit to convert the final intermediate frequency signal (input on AFCIN) to a logic signal and then to mix it down to a low frequency output (on AFCOUT) for counting in the microcontroller. The operation of this system can be explained with the use of a simplified block diagram of the receiver architecture as in figure 30.

Most receivers run the first mixer with a high-side local oscillator controlled by the Main synthesiser, so a positive crystal frequency error will give an increased First I.F. This is then mixed down further by a low-side second oscillator, LO2 in the ACE9030, derived by multiplying the same crystal as used for the Main synthesiser. A positive crystal frequency error would now give a reduced second I.F. if the error in the first I.F. is ignored, but the overall effect is an increase by an amount slightly smaller than the increase in the first I.F.

The second I.F. signal AFCIN at around 450 kHz drives the F.M. Discriminator to recover the modulation and also feeds a third mixer where high-side injection is used to give a very low output frequency, around 54 kHz, and is output on AFCOUT for counting. This third mixer is driven by a clock derived from the crystal but at a much reduced frequency so the effect of the high-side mixing dominates to give an output which drops in frequency when the crystal has a positive frequency error. As a result of the chain of mixing stages the error in the first local oscillator due to the crystal frequency will give a similar frequency shift at the output of the third mixer which is then a large percentage change in the frequency of AFCOUT so it is possible to measure AFCOUT against the crystal to determine the trim needed.

To illustrate the sensitivity of the AFC loop a numerical example can be used, and in the calculations that follow the selection of parameters for the synthesisers are also included to show how some choices are made.

Assume the required receiver frequency is AMPS channel 1, that is 870·030 MHz and that the cellular terminal is built with a 45 MHz first I.F., a 450 kHz second I.F., and a 14·85 MHz crystal.

To receive 870·030 MHz with a 45 MHz first I.F. needs the first local oscillator, the Main synthesiser, to run at a frequency of 870·030 + 45·000 = 915·030 MHz when using high-side injection. For AMPS the most convenient comparison frequency is the channel spacing of 30 kHz so the total division from VCO to phase comparator (N_{TOT} as used elsewhere) will be 30501 for this channel and the reference

division will be 495 for a 14·85 MHz crystal; the term $f_{CRYSTAL}$ is used to refer to the exact crystal frequency in the following calculations.

Thus Main synthesiser (nominally 915·030 MHz) generates:

$$f_{CRYSTAL} \times 30501 \div 495 = f_{CRYSTAL} \times 61{\cdot}61818182$$

This result is independant of the chosen comparison frequency which is given above as an illustration only.

With this drive to the first mixer the actual first I.F. (nominally 45 MHz) is:

$$f_{CRYSTAL} \times 61{\cdot}61818182 - 870{\cdot}030 \text{ MHz}$$

The second mixer is required to downconvert 45 MHz to 450 kHz so needs an LO2 at 44·550 MHz which is $3 \times f_{CRYSTAL}$ and this integer multiplication is the reason for choosing a 14·85 MHz crystal. This mixer operates with low-side injection so the actual second I.F. on the AFCIN pin (nominally 450 kHz) is:

$$f_{CRYSTAL} \times 61{\cdot}61818182 - 870{\cdot}030 \text{ MHz} - 3 \times f_{CRYSTAL}$$

$$= f_{CRYSTAL} \times 58{\cdot}61818182 - 870{\cdot}030 \text{ MHz}$$

This signal feeds the F.M. discriminator to extract the modulation and is also used to derive the AFC information.

The AFC mixer uses a 504 kHz clock derived from the crystal ($f_{CRYSTAL} \times 504 \div 14850 = f_{CRYSTAL} \times 0{\cdot}03393939$) to high-side downconvert AFCIN to a low frequency on AFCOUT, giving:

$$(f_{CRYSTAL} \times 0{\cdot}03393939) - (f_{CRYSTAL} \times 58{\cdot}61818182 - 870{\cdot}030 \text{ MHz}).$$

This is 870·030 MHz – $f_{CRYSTAL} \times 58{\cdot}58424243$ and is the difference between two large but similar numbers, one fixed and the other a multiple of $f_{CRYSTAL}$ and will have an overall value strongly dependent on $f_{CRYSTAL}$.

To evaluate the sensitivity of the system consider a + 1 ppm change in crystal frequency, giving AFCOUT at 53·130 kHz instead of its nominal at 54 kHz, a shift of 870 Hz or 1·61 %. This frequency can be counted in the microcontroller using a timebase derived from $f_{CRYSTAL}$ or any other crystal reference as the error in the timebase due to the crystal is swamped by the changes in AFCOUT.

The counting of AFCOUT should be over a period long enough to resolve changes of around 1 % which means at least 2 ms but is normally a little longer to filter off some noise and modulation on the signal; around 10 ms is a good starting value for system development.

Once the crystal error has been estimated the DAC's controlling the crystal frequency can be adjusted to bring the whole cellular terminal into frequency alignment with the basestation which is normally assumed to be very accurately held at the correct frequency; effects like Doppler shift will be significantly less than 1 ppm for all intended users. Some damping in the control loop for the crystal will be needed to avoid overshoot and hunting, possibly implemented as always under-correcting the crystal or by limiting the slew rate of the corrections.

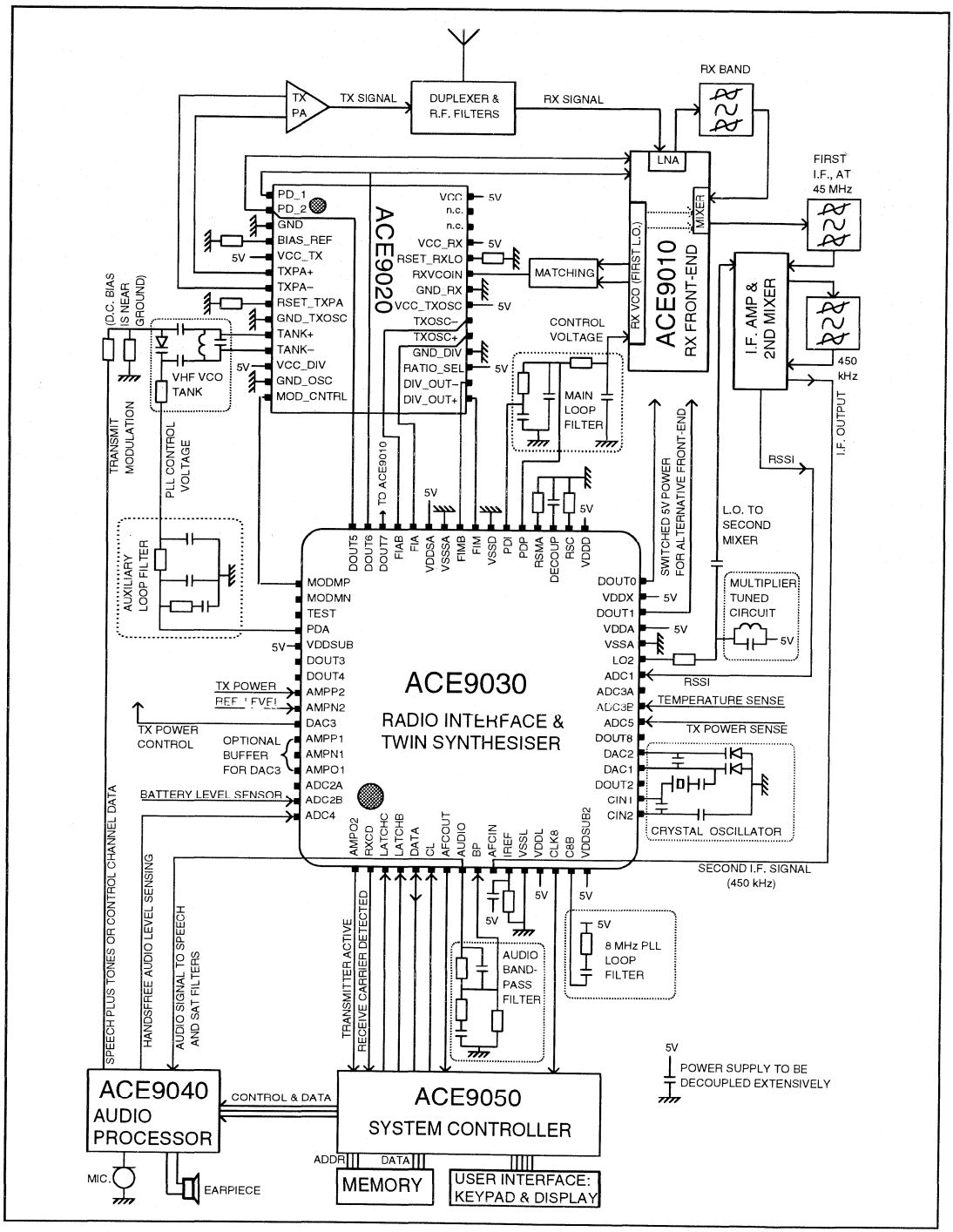


Fig. 31 Complete cellular terminal, showing details of ACE9030 typical application.

ACE9040

AUDIO PROCESSOR for AMPS and TACS CELLULAR PHONES

ACE9040 provides all the speech signal processing and data/SAT tone filtering needed for AMPS or TACS analog cellular telephones.

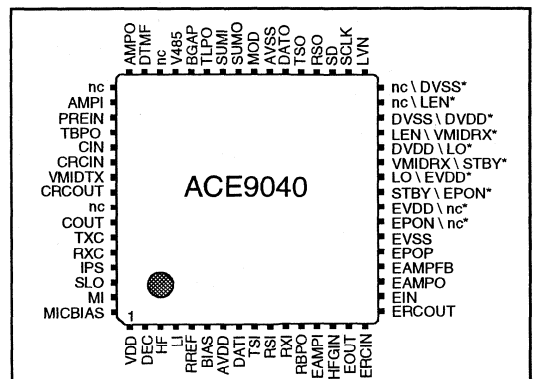
Transmit voice channel functions comprise a microphone amplifier, soft limiter, bandpass filter, compressor, hard limiter, lowpass filter and a gain controlled amplifier to set deviation level. Additional transmit circuits include a DTMF generator, data and SAT filters, deviation setting amplifiers for data/ST and SAT and a modulation combiner.

ACE9040's receive path comprises a bandpass filter, expander, volume control and power amplifiers to directly drive an earpiece or handsfree transducer.

Gain settings, mute switches and filter characteristics are programmed via a three wire serial interface.

To implement a handsfree function, both transmit and receive paths have rectifiers for signal amplitude monitoring via an external pin and signal path attenuators controlled via the serial interface.

ACE9040 combines minimum power consumption with low external component count. Standby modes greatly reduce supply current and extend battery charge intervals.



Note: Pin 1 is identified by moulded spot and by coding orientation. (7 x 7 mm package pinout)*

FP64
VP64*

Fig.1 Pin connections - top view

FEATURES

- Low Power and Low Voltage (3·6 to 5·0 V) Operation
- Power Down Modes
- Direct Connections to Microphone and Earpiece
- Compander with wide operating range:
  Compressor 74 db typ., Expander 36 dB typ.
- SAT Bandpass and Data Lowpass Filters
- Handsfree Operation Supported
- DTMF Generator
- Serial Bus Controlled Gains and Filter Responses
- Part of the ACE Integrated Cellular Phone Chipset
- NMT version available
- TQFP 64 Pin 10x10 mm or 7x7 mm Packages

APPLICATIONS

- AMPS and TACS Cellular Telephones
- Two-Way Radio Systems

RELATED PRODUCTS

ACE9040 is part of the following chipset:

- ACE9010 R.F. Front End with VCO
- ACE9020 Receiver and Transmitter Interface
- ACE9030 Radio Interface and Twin Synthesiser
- ACE9050 System Controller and Data Modem

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6 V
Storage temperature	- 55 °C to + 150 °C
Operating temperature	- 40 °C to + 85 °C
Voltage at any pin	- 0.3 V to V_{DD} + 0.3 V

ORDERING INFORMATION

Industrial temperature range
TQFP 64 lead 10 x 10 mm, 0·5 mm pitch (FP64)
ACE9040/IG/FP1R - devices shipped in trays
ACE9040/PR/FP1R - pre-production
TQFP 64 lead 7 x 7 mm, 0·4 mm pitch (VP64)
ACE9040/IG/FP2R - devices shipped in trays
ACE9040/PR/FP2R - pre-production

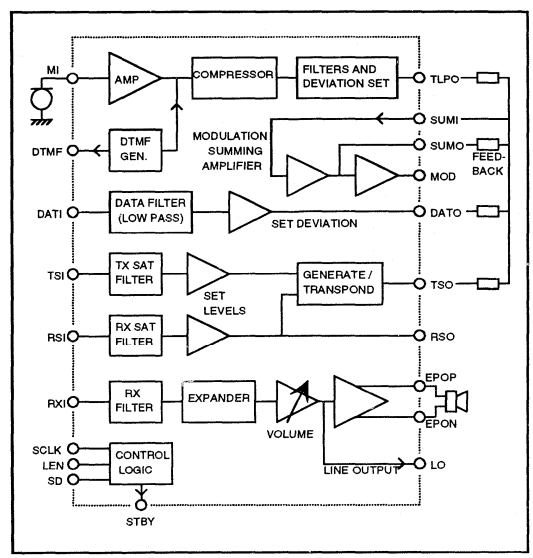


Fig. 2 ACE9040 Simplified Block Diagram

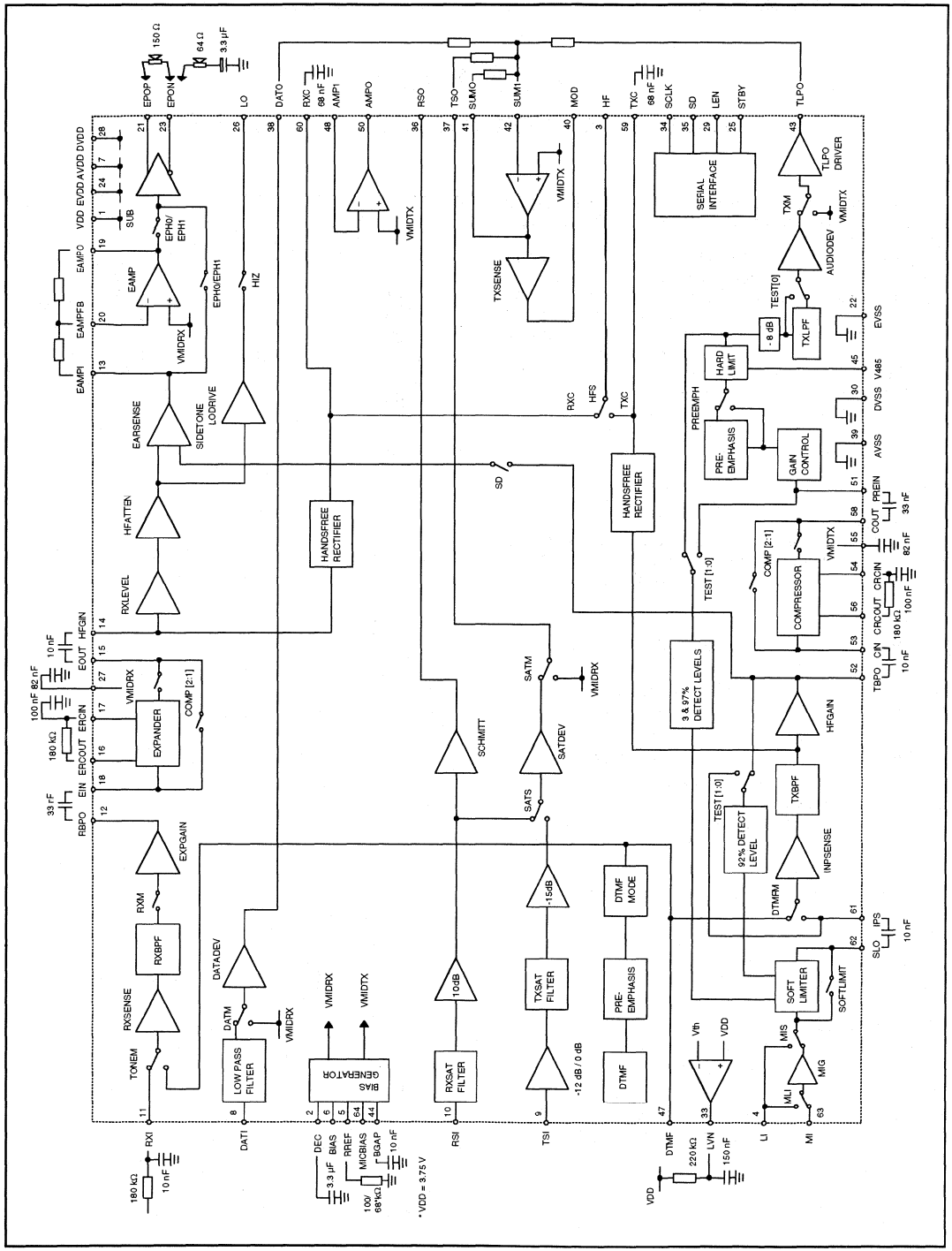


Fig. 3 ACE9040 Detailed Block Diagram

PIN DESCRIPTIONS

Pin No. FP package	Pin No. VP package	Name	Description
1	1	V_{DD}	V_{DD} supply to substrate, pin should be at highest d.c. voltage
2	2	DEC	Mid-supply reference decoupling connection, 3.3 µF to GND
3	3	HF	Output from TX or RX handsfree rectifier, switched by bit "HFS"
4	4	LI	Line input
5	5	RREF	Reference bias current set for all op-amps by resistor to GND
6	6	BIAS	Buffered mid-supply reference output
7	7	AV_{DD}	Analogue V_{DD} input
8	8	DATI	Transmit data input
9	9	TSI	SAT path input for locally generated tone
10	10	RSI	SAT path receiver input for received tone
11	11	RXI	Speech path receiver input
12	12	RBPO	Audio output from EXPGAIN block
13	13	EAMPI	Output from EARSENSE amp
14	14	HFGIN	Input to RX volume control and handsfree attenuator
15	15	EOUT	Expander speech output
16	16	ERCIN	Expander time constant input, 180 kΩ to ERCOUT, 100 nF to GND
17	17	ERCOUT	Expander time constant output, 180 kΩ to ERCIN
18	18	EIN	Expander speech input, 33 nF to RBPO
19	19	EAMPO	Output from EAMP op-amp
20	20	EAMPFB	Inverting input to EAMP op-amp
21	21	EPOP	Earpiece driver positive output
22	22	EV_{SS}	Earpiece V_{SS} (GND) supply connection
-	23/24	nc	No connection
23	25	EPON	Earpiece driver negative output
24	26	EV_{DD}	Earpiece V_{DD} supply input
25	27	STBY	Standby output: low indicates standby state, high is V_{DD} output @ 10 mA
26	28	LO	Line output
27	29	VMIDRX	RX path mid-supply reference voltage, 82 nF to GND
28	30	DV_{DD}	Digital V_{DD}
29	31	LEN	Serial interface latch signal input, rising edge triggered
30	32	DV_{SS}	Digital V_{SS} (GND) connection
31/32	-	nc	No connection
33	33	LVN	Low supply V_{DD} voltage indicator comparator output, reset active low output
34	34	SCLK	Serial interface system clock input
35	35	SD	Serial interface data input
36	36	RSO	Received (regenerated) SAT output
37	37	TSO	Transmit SAT output, regenerated or returned
38	38	DATO	Transmit data filter output.
39	39	AV_{SS}	Analogue V_{SS} (GND)
40	40	MOD	Modulation output: sum of Speech, Data and SAT
41	41	SUMO	Modulation summing amplifier output
42	42	SUMI	Modulation summing amplifier input
43	43	TLPO	Transmit audio lowpass filter output
44	44	BGAP	Bandgap voltage output, 10 nF to GND
45	45	V485	Hard limiter gain selection for 3.75 V or 4.85 V nominal supplies
46	46	nc	No connection
47	47	DTMF	DTMF tone output
48	48	AMPO	Auxillary op-amp output
49	49	nc	No connection
50	50	AMPI	Auxillary op-amp inverting input (non-inverting internally connected to VMIDTX)
51	51	PREIN	Transmit pre-emphasis filter input
52	52	TBPO	Transmit bandpass filter output
53	53	CIN	Compressor audio input, 10 nF from TBPO
54	54	CRCIN	Compressor time constant input, 100 nF to GND, 180 kΩ to CRCOUT
55	55	VMIDTX	TX path reference voltage, 82 nF to GND
56	56	CRCOUT	Compressor time constant output, 180 kΩ to CRCIN
57	57	nc	No connection
58	58	COUT	Compressor audio output, 33 nF to PREIN
59	59	TXC	Transmit handsfree audio level sensing rectifier smoothing filter, 68 nF to GND
60	60	RXC	Received handsfree audio level sensing rectifier smoothing filter, 68 nF to GND
61	61	IPS	Transmit audio gain INPSENSE adjustment block input
62	62	SLO	Soft limiter output
63	63	MI	Microphone input
64	64	MICBIAS	Bias for electret or active microphone

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated (Note 1):

T_{AMB} = – 40 °C to + 85 °C, V_{DD} = 3.6 V to 5.0 V

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply Current and Power Down Modes						
Operating supply current	I_{DD}		13		mA	V_{DD} = 4.85 V R_{REF} = 100 kΩ
				13	mA	V_{DD} = 3.6 V R_{REF} = 68 kΩ
Standby						
Supply Current	$I_{DD(STBY)}$			200	µA	
Attenuation of all inputs signals		40			dB	
Wakeup response time				10	ms	
Sleep (Standby with CLK stopped)						
Supply current	$I_{DD(SLEEP)}$			200	µA	STBY bit set
Delay between setting STBY bit and stopping clock		20			µs	
Delay to starting clock after wakeup		100			µs	

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Transmission Path					
Microphone Amp, MI to SLO pins					
Input bias		$V_{DD}/2$			Internal 150 kΩ bias resistor to $V_{DD}/2$
Microphone input gain	31	32	33	dB	MIS = 1, MLI = 0, MIG = 1
Microphone crosstalk (no MI signal)			– 40	dB	MIS = 1, MLI = 0, MIG = 1
Line input, LI to SLO pins					
Input bias		$V_{DD}/2$			Internal 100 kΩ bias resistor
LI input Gain	– 0.5		0.5	dB	MIS = 0, MLI = 0, MIG = 0
LI input Gain	21	22	23	dB	MIS = 1, MLI = 1, MIG = 0
LI input crosstalk (no LI signal)			– 40	dB	MIS = 1, MLI = 1, MIG = 1
Soft Deviation Limiter, LI to SLO pins					
Nominal gain		0		dB	Limiter not functioning.
Attenuation range	– 30		– 29	dB	
Attenuation steps	0.27	0.5	0.67	dB	
Distortion			2	%THD	Output at 1 Vrms
Attack level:Hard limiter output: enabled	2		98	% V_{DD}	d.c. input on PREIN
disabled	4		96	% V_{DD}	TEST[1:0] = 11
Attack level at TBPO pin		92		% V_{DD}	d.c. input at IPS TEST[1:0] = 11
Attack time		40		µs	Per gain step when signal outside threshold
Decay time		1.68		ms	Per gain step
INPSENSE Gain Stage, IPS to TBPO pins					
Nominal gain	7.5	8	8.5	dB	Input = 100 mVrms, INPS[4:0] = 15, THF = 0 dB,
Gain adjustment range	– 12		12.8	dB	Relative to nominal gain Input = 100 mVrms,
Gain step size	0.6	0.8	1	dB	INPS[4:0] = 0 to 31, THF = 0 dB

Note 1. 100% production tested at 25 °C but guaranteed over specified temperature range.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated (Note 1):

T_{AMB} = – 40 °C to + 85 °C, V_{DD} = 3.6 V to 5.0 V

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
TX Audio Bandpass Filter TXBPF, IPS to TBPO					
Noise			– 72	dBV	
Distortion			1	%THD	1 Vrms output
Frequency response relative to 1040 Hz	– 60.5		– 38.5	dB	f = 60 Hz
	– 25.5		– 10.5	dB	f = 184 Hz INPSENSE = 0 dB
	– 1.0		+ 0.5	dB	f = 430 Hz THF = 0 dB
	– 0.5		+ 0.5	dB	f = 676 Hz, 1040 Hz
	– 0.5		+ 0.5	dB	f = 1410 Hz, 1900 Hz
	– 1.5		– 0.5	dB	f = 3260 Hz
	– 3.0		– 1.5	dB	f = 3500 Hz
	– 10.5		– 5	dB	f = 4120 Hz
	– 20.5		– 15.5	dB	f = 5590 Hz
	– 90.5		– 30.5	dB	f = 9900 Hz
TX Handsfree Gain Stage HFGAIN					
Nominal gain		0		dB	
Gain range	– 52.5	– 49	– 45.5	dB	THF[2:0] = 0 to 7
Gain step size	6.5	7	7.5	dB	
TX Compressor Stage, CIN to COUT pins					
Unity gain level	671	707	742	mVrms	= Vref (Unaffected level)
Input range	0.79		1000	mVrms	
Linearity CIN to COUT: (Deviation from 2:1 I/O relationship)			± 0.5	dB	CIN = Vref + 3 dB to Vref - 59 dB BW = 300 Hz to 3.4 kHz
Attack time		3		ms	12 dB step: - 8 dB to - 20 dB relative to the unity gain (Vref) level
Decay time		13.5		ms	Attack & Decay levels = 1.5 and 0.75 of steady state final value
Distortion			2	%THD	BW = 300 Hz - 3.4 kHz
Frequency response			± 0.2	dB	BW = 300 Hz - 3.4 kHz
TX Pre-emphasis, PREIN to TLPO pins					
Input impedance		75		kΩ	
Internal compressor and BAR:					
Nominal gain TACS	– 7.5	– 7	– 6.5	dB	COMP[2:1] = 10 or 01 at 1 kHz
Nominal gain AMPS	– 11.5	– 11	– 10.5	dB	
External compressor and bypass:					
Nominal gain AMPS & TACS	– 0.5	0	+ 0.5	dB	COMP[2:1] = 11 or 00 at 1 kHz
Frequency response	5.8	6	6.2	dB/ Octave	TEST[1:0] = 01 PREEMPH = 0 (active) f = 300 to 3400 Hz

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated (Note 1):

T_{AMB} = – 40 °C to + 85 °C, V_{DD} = 3.6 V to 5.0 V

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Hard Deviation Limiter					
Gain	13	13.5	14	dB	V485 pin = 0 V (for V_{DD} = 3.75 V)
	15.5	16	16.5	dB	V485 pin = V_{DD} (for V_{DD} = 4.85 V)
Low Pass Filter TXLPF, PREIN to TLPO pins					
Distortion			1.5	%THD	1.5 Vp-p Output level
Noise			– 60	dBV	BW = 30 Hz to 30 kHz
Frequency response TACS/AMPS	0.3		0.7	dB	f = 307 Hz
Relative to 1 kHz	– 0.5		+ 0.5	dB	f = 676 Hz, 1040 Hz
	– 0.5		+ 0.5	dB	f = 1410 Hz, 1900 Hz
	– 3.0		– 1.5	dB	f = 3010 Hz
	– 38.0		– 13.0	dB	f = 3500 Hz
	– 60.0		– 38.0	dB	f = 4120 Hz
	– 60.0		– 38.0	dB	f = 5590 Hz
	– 60.0		– 38.0	dB	f = 9900 Hz
	– 60.0		– 35.0	dB	f = 11870 Hz
	– 60.0		– 35.0	dB	f = 14950 Hz
Gain	– 8.5	– 8	– 7.5	dB	
Attenuation with TXLPF bypassed		8		dB	TEST[0] = 1
Gain Stage AUDIODEV, PREIN to TLPO					
Nominal gain		0		dB	Output at TLPO
Gain adjustment	- 2.8		3.2	dB	
Attenuation step size	0.2	0.4	0.6	dB	Control bits: AUDEV[3:0]
TXM switch attenuation			– 60	dB	AUDIODEV = 0 dB
Combined TX path					
Gain with 7 mV at Microphone input	31.0		35.0	dB	INSENSE = 0 dB, V485 = 0 V
Distortion			1.3	% THD	THF & AUDIODEV = 0 dB
Noise			- 50.0	dBV	MI gain = 22 dB, V_{DD} = 3.6 V
Output d.c. level	1.65		1.9	V	COMP[2:1] = 00, Softlimit = off

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated (Note 1):

T_{AMB} = – 40 °C to + 85 °C, V_{DD} = 3.6 V to 5.0 V

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Receive Path					
RX Input stage RXSENSE, RXI to RBPO pins					
Input bias		$V_{DD}/2$			Internally biased to $V_{DD}/2$ by 150 kΩ
Nominal gain	7.5	8	8.5		
Gain adjustment range	– 6		6.4	dB	Input 40 mVrms at RXI
Gain adjustment step size	0.2	0.4	0.6	dB	RXM = 1, RXSENSE = 0 to 31
RX Audio Bandpass Filter RXBPF					
Gain		0		dB	
Distortion			1	%THD	At 1 kHz with 40 mVrms input
Noise			– 60	dB	BW= 30 Hz to 30 kHz
Frequency Response	– 90.0		– 45.0	dB	f = 60 Hz RXSENSE = 0 dB
Relative to 1040 Hz	– 15.0		– 7.0	dB	f = 184 Hz COMP[1:0] = 00
	– 1.0		+ 0.5	dB	f = 430 Hz
	– 0.5		+ 0.5	dB	f = 676 Hz, 1040 Hz
	– 0.5		+ 0.5	dB	f = 1410 Hz, 1900 Hz
	– 3.0		– 0.5	dB	f = 3260 Hz
	– 10.0		– 6.0	dB	f = 3500 Hz
	– 40.0		– 25.0	dB	f = 4120 Hz
	– 40.0		– 25.0	dB	f = 5590 Hz
	– 90.0		– 40.0	dB	f = 9900 Hz
RXM mute switch attenuation			– 40	dB	Output switched to $V_{DD}/2$ when muted.
Rx Internal Expander					
Gain EXPGAIN: internal	11.8	12.3	12.8	dB	COMP[2:1] = 10
external and bypass		0		dB	COMP[2:1] = 00 or 11
Unity gain level	900	1000	1100	mVrms	= Vref (Unaffected level)
Linearity EIN to EOUT			± 1	dB	EIN = Vref to Vref - 33 dB
(Deviation from 2:1 input/output)					BW = 300 to 3400 Hz
Distortion			2	%THD	1 Vrms
Frequency response			± 0.2	dB	300 to 3400 Hz
Attack time		3		ms	6 dB step (- 4 dB and -10 dB) relative to the unity gain (Vref) level at 1 kHz to pin EIN. Output at EOUT.
Decay time		13.5		ms	Attack and delay time levels = 0.57 and 1.5 of final steady state value.
RX Volume Control RXLEVEL					
Nominal Gain	– 11	– 12	– 13	dB	RXV[2:0] = 3, RHF = 0 dB
Gain adjustment range	– 9		12	dB	RXV[2:0] = 0 to 7
Gain adjust step size	2	3	4	dB	EARSENSE = 0 dB, Sidetone = 0 dB
RX Handsfree Gain Stage HFATTEN					
HFGAIN to EAMP nominal gain	– 0.4	0	0.4	dB	RHF, RVX, EARSENSE = 0 dB, SD =0
Gain range	– 52.5	– 49	– 45.5	dB	RHF[2:0] = 0 to 7
Gain control step size	6.5	7	7.5	dB	EARSENSE = 0 dB, Sidetone = 0 dB
RX Line Driver LODRIVE					
LO gain	4	5	6	dB	RVX = 0 dB, RHF = 0 dB, HIZ =1
Distortion			2	%THD	1.0 Vrms output
LO mute	– 40			dB	HIZ = 0
Noise			– 80	dBV	BW = 30 Hz to 30 kHz
LOoutput during mute	1.5	$V_{DD}/2$	2.1	V	V_{DD} = 3.6 V

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated (Note 1):

T_{AMB} = – 40 °C to + 85 °C, V_{DD} = 3.6 V to 5.0 V

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Rx Earpiece Gain Adjustment EARSENSE					
Nominal gain		0		dB	
Total gain	- 2.8		3.2	dB	EARS[3:0] = 0 to 15
Gain adjustment step size	0.2	0.4	0.6	dB	RVX = 0 dB, RHF = 0 dB, SD = 0
Distortion			1	% THD	Output 1 Vrms
Rx Sidetone Path, IPS to EAMPI					
Attenuation at EARSENSE amp input	18	19	20	dB	EARSENSE = 0 dB
Sidetone mute			– 40	dB	SD = 0
Rx Earpiece Drivers EPOP & EPON					
EPON single ended gain	5.5	6	6.5	dB	Output = 2 Vpp, 120 Ω EPON to EPOP
EPOP single ended d.c. level	1.7	$V_{DD}/2$	1.9	V	V_{DD} = 3.6 V, EPH1 = 1, EPH0 = 0
EPOP single ended a.c. level			– 20	dB	
EPON single ended distortion			1	% THD	Output = 2 Vpp
EPON & EPOP differential gain	11.5	12	12.5	dB	150 Ω (± 20 %) EPON to EPOP
EPOP differential distortion			1	%THD	Output = 4 Vpp, EPH1 = 1, EPH0 = 1
Earpiece mute switch attenuation	40			dB	EPH0 = 0 & EHP1 = 0
EPON external mode:					64 Ω (± 20 %) + 3.3 µF to GND,
EPON gain relative to EAMPI	5.5		6.5	dB	EAMPFB open, Input = HFGIN
EPON distortion			1	% THD	Output = 1.1 Vpp
EPOP output current external mode	– 10		10	µA	At V_{DD} & 0 V
EPON & EPOP mute			– 40	dB	EPH1 = 0, EPH0 = 0
EPOP Noise			– 80	dBV	EPH1 = 1, EPH0 = 1
Transmit Data Path					
TX Data Filter 16 kHz & 20 kHz					
Input bias at DATI		$V_{DD}/2$		V	Internally tied via 800 kΩ resistor to $V_{DD}/2$.
Nominal gain	- 6.5	- 6	- 5.5	dB	Input = 1 Vrms
Distortion			1.5	%THD	Output = 1.5 Vp-p
Noise			-60	dBV	BW = 30 Hz to 30 kHz
DATM mute switch attenuation	40			dB	
Data Filter frequency response					
16 kHz (TACS)	– 0.3		0.3	dB	f = 676 Hz, 1040 Hz
	– 0.3		0.3	dB	f = 4120 Hz, 12120 Hz
	– 1.0		0.0	dB	f = 13960 Hz
	– 2.0		– 1.0	dB	f = 14950 Hz DATM = 1
	– 3.0		– 2.0	dB	f = 16050 Hz DATADEV = 0 dB
	– 3.5		– 2.5	dB	f = 16420 Hz Relative to 1040 Hz
	– 4.0		– 3.0	dB	f = 17040 Hz DATAF[1:0] = 10
	– 6.0		– 4.0	dB	f = 18020 Hz
	– 9.5		– 7.5	dB	f = 19990 Hz
	– 11.0		– 9.0	dB	f = 20970 Hz

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated (Note 1):

T_{AMB} = – 40 °C to + 85 °C, V_{DD} = 3.6 V to 5.0 V

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
TX Data Filter 16 kHz & 20 kHz (continued)					
Data Filter frequency response					
20 kHz (AMPS)	– 0.3		0.3	dB	f = 676 Hz, 1040 Hz
	– 0.3		0.3	dB	f = 4120 Hz, 16050 Hz
	– 1.0		0.0	dB	f = 18020 Hz
	– 2.0		– 0.5	dB	f = 18880 Hz DATAF[1:0] = 11
	– 3.0		– 1.5	dB	f = 20240 Hz DATM = 1
	– 3.5		– 2.0	dB	f = 20540 Hz DATADEV = 0dB
	– 4.0		– 2.5	dB	f = 20970 Hz Relative to 1040 Hz
	– 5.0		– 3.0	dB	f = 21960 Hz
	– 6.0		– 4.0	dB	f = 22820 Hz
	– 8.0		– 5.0	dB	f = 24050 Hz
TX Data Gain Stage DATADEV, DATI to DATO pins					
Nominal gain		0		dB	
Gain adjustment	- 2.8		3.2	dB	DATD[3:0] = 7
Gain adjustment steps	0.2	0.4	0.6	dB	DATM = 1 DATAF[1:0] = 00
TXSAT and RXSAT Bandpass Filters 6 kHz					
RXSAT Filter					
RXSAT gain	9		11	dB	Input = 400 mVrms at 6030 Hz, SATDEV = 0 dB, SATM = 1, SATS = 0dB
RXSAT 6 kHz frequency response	– 90.0		– 35.0	dB	f = 2520 Hz Relative to 6030 Hz
	– 90.0		– 35.0	dB	f = 3500 Hz SATS = 0 dB,
	– 90.0		– 35.0	dB	f = 4120 Hz TACS = 1,
	– 29.0		– 24.0	dB	f = 4980 Hz SATD = 15 (0 dB),
	– 0.30		0.50	dB	f = 5900 Hz SATM = 1
	– 0.10		0.35	dB	f = 5960 Hz
	– 0.10		0.35	dB	f = 6030 Hz
	– 0.30		0.50	dB	f = 6090 Hz
	– 26.5		– 22.0	dB	f = 7010 Hz
	– 90.0		– 29.0	dB	f = 8060 Hz
	– 90.0		– 35.0	dB	f = 9040 Hz
	– 90.0		– 35.0	dB	f = 9290 Hz
RSO Schmitt output	5.5	6.0	6.5	kHz	SATS = 0 dB, TACS = 1

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated (Note 1):

T_{AMB} = – 40 °C to + 85 °C, V_{DD} = 3.6 V to 5.0 V

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
TXSAT Filter 6 kHz					
TXSAT gain	– 28.0		– 26.0	dB	TACS =1, SATS = 1, Output = 1 Vpp at 6030 Hz
TXSAT 6 kHz frequency response	– 90.0		– 35.0	dB	f = 2520 Hz Relative to 6030 Hz
	– 90.0		– 35.0	dB	f = 3500 Hz SATS = 1
	– 90.0		– 35.0	dB	f = 4120 Hz TACS = 1
	– 29.0		– 24.0	dB	f = 4980 Hz SATD = 15 (0 dB)
	– 0.30		0.50	dB	f = 5900 Hz SATM = 1
	– 0.10		0.35	dB	f = 5960 Hz
	– 0.10		0.35	dB	f = 6030 Hz
	– 0.30		0.50	dB	f = 6090 Hz
	– 25.0		– 22.0	dB	f = 7010 Hz
	– 60.0		– 35.0	dB	f = 8060 Hz
	– 60.0		– 35.0	dB	f = 9040 Hz
	– 80.0		– 35.0	dB	f = 9290 Hz
Gain Stage SATDEV					
Nominal gain		0		dB	
Gain adjustment range	- 4.5		4.8	dB	SATS = 0, TACS = 1, SATM = 1
Gain adjustment size	0.1	0.3	0.5	dB	SATD[4:0] = 0 to 31
Distortion			2	% THD	Output = 1.1 Vpp
SATM switch mute attenuation	40			dB	SATM = 0
Noise			– 60	dBV	SATD[4:0] = 15 (0 dB)
DTMF Generator					
DTMF output level	60		85	mVrms	V_{DD} = 3.6 V, high & low tone
DTMF single tone distortion:					
TONEM switch on (via TBPO)			5	% THD	Low group, TONEM = 1
TONEM switch off			– 40	dB	TONEM = 0
DTMF switch on (via RBPO)			5	% THD	High group, DTMFM = 1
DTMF switch off			– 40	dB	DTMFM = 0
DTMF high group pre-emphasis	– 0.5		0.5	dB	DTWIST = 0
	1.5		2.5	dB	DTWIST = 1
Gain Stage TXSENSE, SUMI to MOD pins					
Gain	- 0.5	0	0.5	dB	Output at MOD.
Gain adjustment	- 2.8		3.2	dB	TXSEN[3:0] = 0 to 15
Gain adjustment step size	0.2	0.4	0.6	dB	
Distortion			2	%THD	Output = 1 Vrms
Noise			– 80	dBV	BW = 30 Hz to 30 kHz

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated (Note 1):

T_{AMB} = – 40 °C to + 85 °C, V_{DD} = 3.6 V to 5.0 V

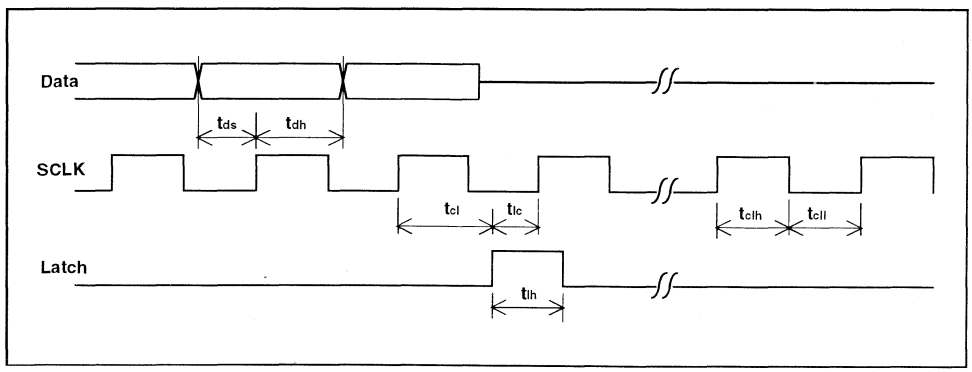
Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Handsfree Rectifiers					
Attack time		1		ms	Capacitors to GND =
Decay time		35		ms	68 nF at TXC & RXC pins
TX nominal output levels:					
d.c. offset	0.3		0.5	V	Input at IPS = 0 mVrms
a.c. level	1.4	1.5	1.6	V	Input at IPS = 40 mVrms, 1 kHz INPSENSE = 0 dB, HFS = 0 HFP = 1
RX nominal output levels:					
d.c. offset	0.3		0.5	V	Input at HFGIN = 0 mVrms
a.c. level	1	1.1	1.2	V	Input at HFGIN = 100 mVrms, 1 kHz HFS =1, HFP = 1
Voltage Outputs					
DEC & BIAS output voltage	1.70	$(V_{DD}-V_{SS})/2$	1.9	V	V_{DD} = 3.6 V, 3.3 µF decoupling to GND at DEC pin
Microphone Bias: Source 1 mA	2.7		2.9	V	MLI = 0, MIS = 1, V_{DD} = 3.6 V
Sink 1 mA	2.7		2.9	V	MLI = 0, MIS = 1, PD = 0
Microphone disabled	– 0.1		0.10	V	MLI = 0, MIS = 0
External Reference Resistor		100		kΩ	V_{DD} = 4.85 V
connected from pin RREF to GND		68		kΩ	V_{DD} = 3.75 V
Bandgap at BGAP	1.10		1.35	V	
LVN Supply Voltage Comparator					
					Default condition
V_{DD} = 3.6 V	– 10		10	µA	(high at V_{DD} – 0.2 V)
V_{DD} = 3.1 V	2.00		20.0	mA	(low at 0.4 V)
LVN comparator operating lower limit of V_{DD}		1		V	

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated (Note 1):

T_{AMB} = – 40 °C to + 85 °C, V_{DD} = 3.6 V to 5.0 V

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
DC Characteristics						
Logic input high	V_{IH}	0.7 x V_{DD}		V_{DD} + 0.3	V	
Logic input low	V_{IL}	- 0.3		0.3 x V_{DD}	V	
Input Capacitance	C_{in}			10	pF	
logic inputs leakage current	I_{ILK}			± 1	µA	SCLK, SD, LEN inputs V_{DD} = 3.6 V & 0.0 V
AC Characteristics						
Clock input frequency: Serial interface & SC Filters	f_{CLK}		1.008		MHz	
		-100		100	ppm	Deviation from 1.008 MHz
Clock duty cycle	D	40	50	60	%	
Number of clock rising edges to input data		24			clock cycles	
Clock cycles between latch pulses on LEN		30			clock cycles	
Clock cycles before power-up and after powerdown		8			clock cycles	
Data setup time	t_{ds}	80			ns	V_{DD} = 3.75 V ± 0.1 V.
Data hold time	t_{dh}	80			ns	T_A = - 40 °C to + 85 °C
Clock low	t_{cll}	400		600	ns	
Clock high	t_{clh}	400		600	ns	
Clock high to latch high	t_{cl}	440			ns	
Latch high to clock high	t_{lc}	220			ns	
Latch high	t_{lh}	240			ns	
Rise and fall times				50	ns	All digital inputs
Power Supply Rejection Ratio:	PSRR					V_{DD} = 3.8 V + 100 mVpp (a.c.) COMP[2:1] = 00.
TX path (LI to TLPO)				– 20	dB	LI = 0 dB, V485 = 13.5 dB INPSENSE = 0 dB, softlimit on.
RX path (RXI to EPOP)				– 30	dB	AUDIODEV, RXSENSE = 0 dB THF, RHF, EARSENSE = 0 dB RXV, SIDETONE off.
Crosstalk between RX and TX path				TBA	dB	



Serial Interface Input Timing

TYPICAL FREQUENCY RESPONSES

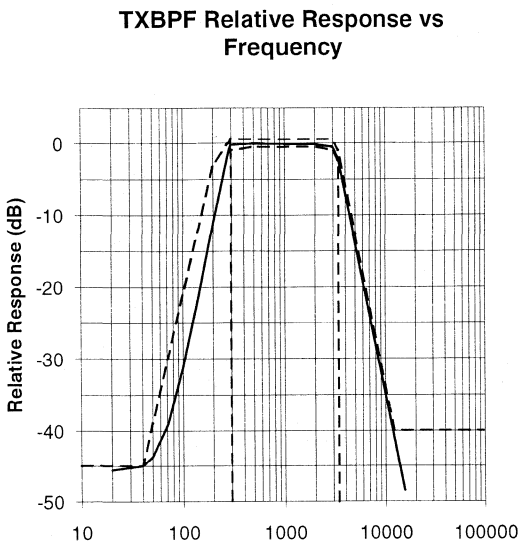


Figure 4

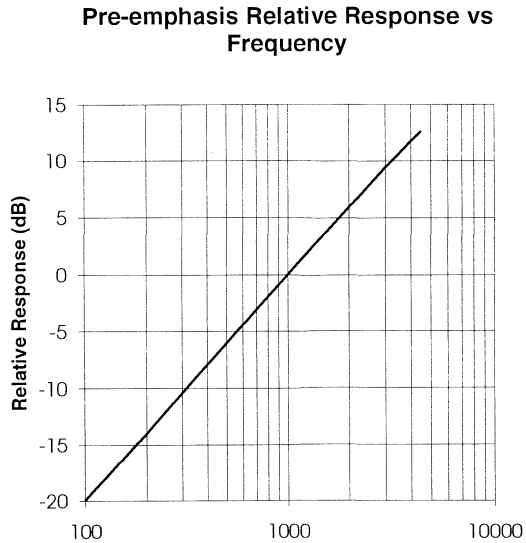


Figure 5

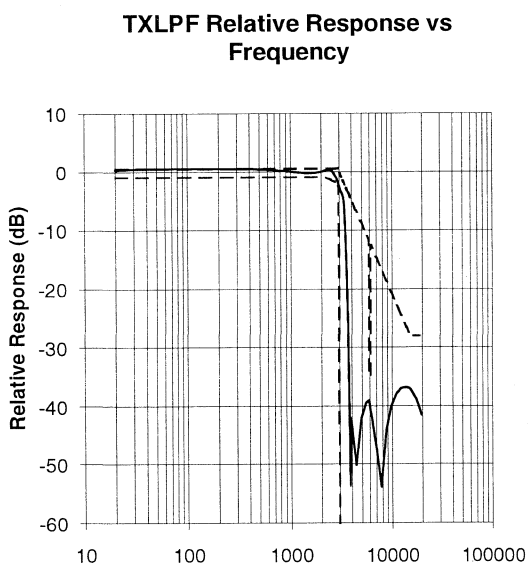


Figure 6

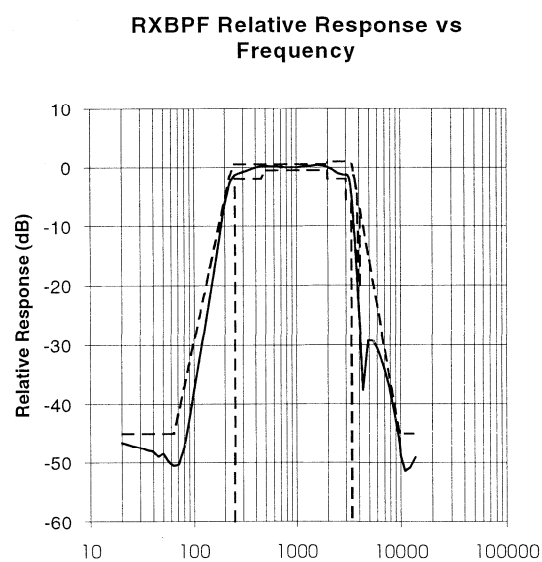


Figure 7

TYPICAL FREQUENCY RESPONSES

Transmit Overall Relative Response vs Frequency

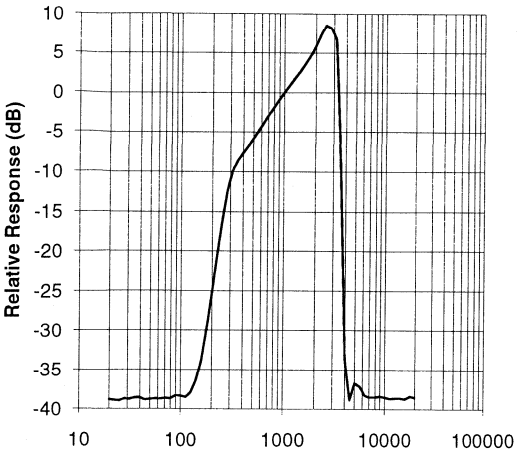


Figure 8

SAT Filter Relative Response vs Frequency

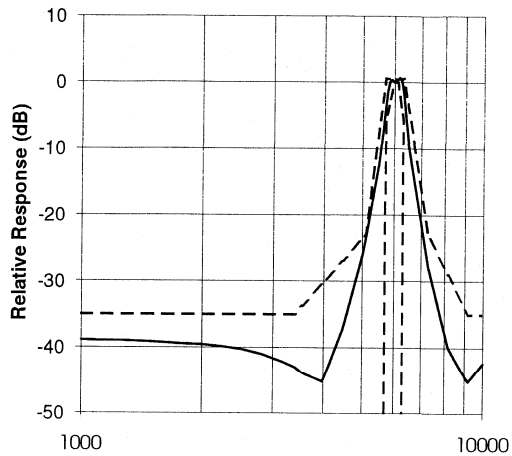


Figure 9

DESCRIPTION

ACE9040 combines all the voice, data and signalling processing circuits for analog cellular telephones operating with the AMPS or TACS systems.

Transmit channel functions comprise a microphone amplifier, soft limiter, bandpass speech filter, compressor, pre-emphasis filter, hard limiter, lowpass transmit filter and a gain control stage to set the deviation. Additional transmit circuits include a DTMF generator, a lowpass filter for either control data or signalling tone (ST), filters for supervisory audio tone (SAT), either transponded or locally re-generated, and deviation setting amplifiers for Data, ST and SAT. The outputs from the transmit functions feed a modulation combiner whose gain can be adjusted before driving a modulator and external power amplifier.

ACE9040's receive path consists of a bandpass filter, expander, volume control and power amplifier to directly drive the earpiece, either differentially or in single ended modes. Sidetone and DTMF tones can be introduced into the receive path.

Gain settings, filter characteristics and system control is programmed via a three wire serial interface to give optimum operation with either the AMPS or TACS analog cellular systems.

To implement a handsfree function, both transmit and receive paths have rectifiers which enable signal amplitude monitoring via an external pin and signal path attenuators controlled via the serial interface.

All filter characteristics are set by ratioed on-chip components and by a fixed externally input clock rate of 1·008 MHz and do not need trimming, filter response options are selected via the serial interface.

Gain adjustments for different system specifications and component tolerancing are set via the serial interface using gain control blocks in the transmit and receive signal paths. These eliminate the need for any mechanically adjusted potentiometers. Some gain levels change automatically when the control bits for one of the standards are set, others are under user control.

Power saving operates when an individual block is de-selected and for the whole circuit when in Standby. The circuit combines high performance with minimum power consumption and uses as few external components as possible.

SERIAL CONTROL BUS

All functions are controlled via a three wire serial interface. Input is via pins SD for serial data, SCLK for the clock input and LEN for the control message latch signal.

Incoming data bits are clocked in on the rising edges of SCLK clock input. At the end of each control message comprising three 8-bit data bytes, the rising edge of the LEN pulse latches in the data. A system controller should clock data out on clock falling edges to ensure the maximum timing margins.

The SCLK clock input must be at 1·008 MHz and continuous whenever the ACE9040 is active because ACE9040's switched capacitor filters use clocks derived from SCLK to set frequency responses.

ACE9040 expects a minimum of 30 clock cycles between LEN latch pulses, including the clock cycle containing the latch pulse. A minimum of 8 clock cycles before the beginning of an Operate command or after a Standby command are expected.

Three data bytes DATA1, DATA2, and DATA3 contain bits for system selection, control and mute switches, gain control and filter response settings, as shown in figure 10. The last two bits of DATA3, DATA3[1] and [0], determine the message type, either "Operation", "Initializing mode 0", "Initializing mode 1" or "Handsfree". The details of these four modes are described in tables 2 to 19.

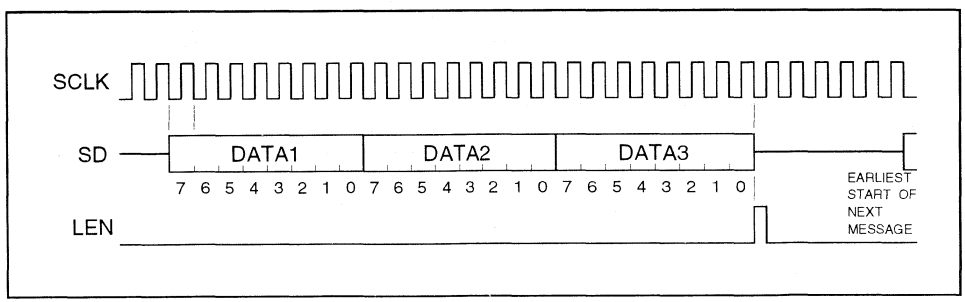


Fig. 10 Serial Receive Bus Timing

DATA3[1]	DATA3[0]	Mode
0	1	"Operation"
0	0	"Initializing mode 0"
1	0	"Initializing mode 1"
1	1	"Handsfree"

Table 1 Mode Selections

CONTROL BUS: OPERATION MODE

Data bit	Bit Name	Function	Effect when at 0	Effect when at 1
DATA3:				
[0]	DATA3[0]	Bus Mode Select	Must be "1"	Must be "1"
[1]	DATA3[1]	Bus Mode Select	Must be "0"	Must be "0"
[2]	PD	Power Down	Operate	Standby
[5:3]	RXV[2:0]	Receive Volume	See table 3	See table 3
[6]	HIZ	Line Output Drive Enable	Off	On
[7]	EPH1	Earpiece Mute	See table 5	See table 5
DATA2:				
[0]	RXM	Receiver Audio Mute	Muted	On
[1]	SATM	Transmit SAT Mute	Muted	On
[2]	DATM	Transmit Data Mute	Muted	On
[3]	TXM	Transmit Audio Mute	Muted	On
[4]	MLI	Microphone Select	See table 4	See table 4
[5]	DTMFEN	Enables each DTMF tone selection	Disabled	Enabled
[7:6]	DTMFMODE[1:0]	DTMF Tone Select	See table 6	See table 6
DATA1:				
[0]	DTMFM	Transmit DTMF Switch	Speech	DTMF
[1]	TONEM	DTMF RX path Confirm Tone Switch	Speech	DTMF
[5:2]	DTMF[3:0]	DTMF Code Select	See table 7	See table 7
[6]	MIS	Line Input Select	See table 4	See table 4
[7]	PREEMPH	Transmit Pre-emphasis Bypass	Active	Bypassed

Table 2 "Operation Mode", DATA3[1:0] = 01.

RXV[2]	RXV[1]	RXV[0]	Gain in dB
0	0	0	– 21
0	0	1	– 18
0	1	0	– 15
0	1	1	– 12
1	0	0	– 9
1	0	1	– 6
1	1	0	– 3
1	1	1	0

Table 3 Receiver Volume Control Nominal Levels set by RXV[2:0].

MLI	MIS	Function
0	0	LI selected, no gain
0	1	MI selected, Micamp gain
1	0	NOT ALLOWED
1	1	LI selected, Micamp gain

Table 4 Microphone Input Select

EPH1	EPH0	Function
0	0	Earphone mute
0	1	External Earpiece (EPON to ground)
1	0	Single ended output (EPON to EPOP)
1	1	Differential output (EPON and EPOP)

Table 5 Earphone Mode Select (EHP0 in Initializing mode 0)

DTMFMODE[1:0] bits 1 and 0	Tone generated
0 and 0	No tone.
0 and 1	Low frequency only.
1 and 0	High frequency only.
1 and 1	Dual tones.

Table 6 DTMF Mode Selection

DTMF[3:0] bits 3 2 1 0	Keypad legend	Low Freq. Hz.	High Freq. Hz.
0 0 0 0	1	697	1209
0 0 0 1	2	697	1336
0 0 1 0	3	697	1477
0 0 1 1	A	697	1633
0 1 0 0	4	770	1209
0 1 0 1	5	770	1336
0 1 1 0	6	770	1477
0 1 1 1	B	770	1633
1 0 0 0	7	852	1209
1 0 0 1	8	852	1336
1 0 1 0	9	852	1477
1 0 1 1	C	852	1633
1 1 0 0	*	941	1209
1 1 0 1	0	941	1336
1 1 1 0	#	941	1477
1 1 1 1	D	941	1633

Table 7 DTMF Tones

CONTROL BUS: INITIALIZING MODE 0

Data bit	Bit Name	Function	Effect when at 0	Effect when at 1
DATA3:				
[0]	DATA3[0]	Bus Mode Select	Must be "0"	Must be "0"
[1]	DATA3[1]	Bus Mode Select	Must be "0"	Must be "0"
[2]	EPH0	Earpiece Mode Select	See table 5	See table 5
[3]	DTWIST	DTMF Pre-emphasis	0 dB	2 dB
[4]	PDLVC	Power Supply Comparator	Active	Power Down
[6:5]	COMP[2:1]	Compander Control	See table 9	See table 9
[7]	INPS[0]	Transmit Audio Gain Adjust	See table 10	See table 10
DATA2:				
[3:0]	INPS[4:1]	Transmit Audio Gain Adjust	See table 10	See table 10
[7:4]	RXSEN[3:0]	Receive Audio Gain Adjust	See table 11	See table 11
DATA1:				
[0]	RXSEN[4]	Receive Audio Gain Adjust	See table 11	See table 11
[5:1]	SATD[4:0]	SAT Modulation Gain	See table 12	See table 12
[6]	SD	Sidetone Enable	Off	On
[7]	SOFTLIMIT	Enables Softlimiter	Off	On

Table 8 "Initializing Mode 0", DATA3[1:0] = 00.

COMP[2]	COMP[1]	Mode
0	0	Bypass Compander
1	0	Internal Compander
1	1	External Compander
0	1	BAR Signal Input Mode (RBPO at high impedance)

Table 9 Compander Operating Modes set by COMP[2:1].

INPS[4]	INPS[3]	INPS[2]	INPS[1]	INPS[0]	Gain (dB)
0	0	0	0	0	− 12·0
0	0	0	0	1	− 11·2
:	:	:	:	:	:
:	:	:	:	:	:
1	1	1	1	0	+ 12·0
1	1	1	1	1	+ 12·8

Table 10 INPSENSE Transmit Audio Nominal Gain settings by INPS[4:0].

RXSEN[4]	RXSEN[3]	RXSEN[2]	RXSEN[1]	RXSEN[0]	Gain (dB)
0	0	0	0	0	− 6·0
0	0	0	0	1	− 5·6
:	:	:	:	:	:
:	:	:	:	:	:
1	1	1	1	0	+ 6·0
1	1	1	1	1	+ 6·4

Table 11 RXSENSE Receive Audio Nominal Gain settings by RXSEN[4:0].

SATD[4]	SATD[3]	SATD[2]	SATD[1]	SATD[0]	Gain (dB)
0	0	0	0	0	− 4·5
0	0	0	0	1	− 4·2
:	:	:	:	:	:
:	:	:	:	:	:
1	1	1	1	0	+ 4·5
1	1	1	1	1	+ 4·8

Table 12 SATDEV Transmit SAT Nominal Modulation Gain settings by SATD[4:0].

CONTROL BUS: INITIALIZING MODE 1

Data bit	Bit Name	Function	Effect when at 0	Effect when at 1
DATA3:				
[0]	DATA3[0]	Bus Mode Select	Must be "0"	Must be "0"
[1]	DATA3[1]	Bus Mode Select	Must be "1"	Must be "1"
[3:2]	TEST[1:0]	Test Mode Select	see table 14	see table 14
[4]	SATS	SAT source Select	RXSAT	TXSAT
[6:5]	DATAF[1:0]	Data Filter Bandwidth Select	see table 15	see table 15
[7]	TACS	Cellular System Select	‡	TACS‡
DATA2:				
[3:0]	TXSEN[3:0]	Combined Modulation Gain	see table 16	see table 16
[7:4]	DATD[3:0]	Data Modulation Gain	see table 16	see table 16
DATA1:				
[3:0]	AUDEV[3:0]	Audio Modulation Gain	see table 16	see table 16
[7:4]	EARS[3:0]	Earpiece "EARSENSE" Gain	see table 16	see table 16

‡See table 19.

Table 13 "Initializing Mode 1", DATA3[1:0] = 10.

TEST[1]	TEST[0]	Test Mode
0	0	Operate mode (not in test mode)
1	0	Test DTMF
0	1	Bypass TXLPF
1	1	Bypass TXLPF & Softlimiter test

Table 14 Test Modes selected by TEST[1:0].

DATAF[1]	DATAF[0]	Cut-off Frequency
1	0	16 kHz
1	1	20 kHz

Table 15 Data Filter Bandwidths selected by DATAF[1:0].

TXSEN[3] DATD[3] AUDEV[3] EARS[3]	TXSEN[2] DATD[2] AUDEV[2] EARS[2]	TXSEN[1] DATD[1] AUDEV[1] EARS[1]	TXSEN[0] DATD[0] AUDEV[0] EARS[0]	Gain (dB)
0	0	0	0	− 2·8
0	0	0	1	− 2·4
:	:	:	:	:
:	:	:	:	:
1	1	1	0	+ 2·8
1	1	1	1	+ 3·2

Table 16 TXSENSE, DATADEV, AUDIODEV, and EARSENSE Nominal Gains set, respectively, by TXSEN[3:0], DATD[3:0], AUDEV[3:0], and EARS[3:0].

CONTROL BUS: HANDSFREE MODE

Data bit	Bit Name	Function	Effect when at 0	Effect when at 1
DATA3:				
[0]	DATA3[0]	Bus Mode Select	Must be "1"	Must be "1"
[1]	DATA3[1]	Bus Mode Select	Must be "1"	Must be "1"
[4:2]	THF[2:0]	Transmit Handsfree Gain	see table 18	see table 18
[7:5]	RHF[2:0]	Receive Handsfree Gain	see table 18	see table 18
DATA2:				
[0]	HFP	Handsfree Rectifiers Power	Off	On
[1]	HFS	HF Output Connection Path	Transmit	Receive
[2]	MIG	Microphone Amplifier Gain	+ 22 dB	+ 32 dB
[4:3]	not used	-	-	-
[5]	AMPS	Cellular System Select	‡	AMPS‡
[6]	not used	-	-	-
[7]	-	-	must be "0"	must be "0"
DATA1:				
[2:0]	-	-	must be "0"	must be "0"
[5:3]	not used	-	-	-
[7:6]	not used	-	-	-

‡See table 19.

Table 17 "Handsfree Mode", DATA3[1:0] = 11.

THF[2] RHF[2]	THF[1] RHF[1]	THF[0] RHF[0]	Gain (dB)
0	0	0	0
0	0	1	– 7
0	1	0	– 14
0	1	1	– 21
1	0	0	– 28
1	0	1	– 35
1	1	0	– 42
1	1	1	– 49

Table 18 TXHFGAIN and RXHFGAIN Handsfree Attenuator Nominal Gains, set by THF[2:0] and RHF[2:0].

CIRCUIT OPERATING MODES

ACE9040 has three operating modes: Operate, Standby and Sleep. In Operate mode all parts of the circuit are active, except for any explicitly powered down and the DTMF generator which only powers up when tones are generated. The pin STBY is pulled high in Operate mode to supply V_{DD} to external audio circuits, such as a compander.

Standby Mode

Standby mode is used when the cellular terminal is waiting for a call and is selected by an "Operation mode" control message with bit PD at "1". In this mode all analog circuits, data paths, filters and their clock drivers are powered down giving a greatly reduced supply current. In standby mode all switch and level controls retain their previous state, the pin STBY is not driven removing the V_{DD} supply from external circuits. To leave Standby mode an operate command should be given by using an "Operation mode" control message with bit PD at "0".

Sleep Mode

Sleep mode is the same as Standby but without a clock input. To enter sleep mode the standby command should be given and after a delay of at least 20 µs the SCLK clock stopped. To wake-up from sleep mode, the the SCLK clock must be started and after a delay of at least 100 µs an operate command given.

Power on Reset

At power up ACE9040 is put into Standby mode. ACE9040 is set up by the controlling processor via the serial interface using four control messages: "Operation", "Initializing mode 0", "Initializing mode 1" and "Handsfree". Usually the "Operation" control message would be sent last as it contains the power down/up bit PD.

CELLULAR SYSTEM SELECTION

Two control bits are used to set the filter responses and gain levels for the AMPS or TACS cellular systems. These bits are TACS in control message "Initializing mode 1" and AMPS in control message "Handsfree mode" and select the system as shown in table 19.

Bits		System
AMPS	TACS	Selected
0	0	Not valid
0	1	TACS
1	0	AMPS
1	1	Not valid

Table 19 Cellular System Selection

TRANSMIT VOICE PATH

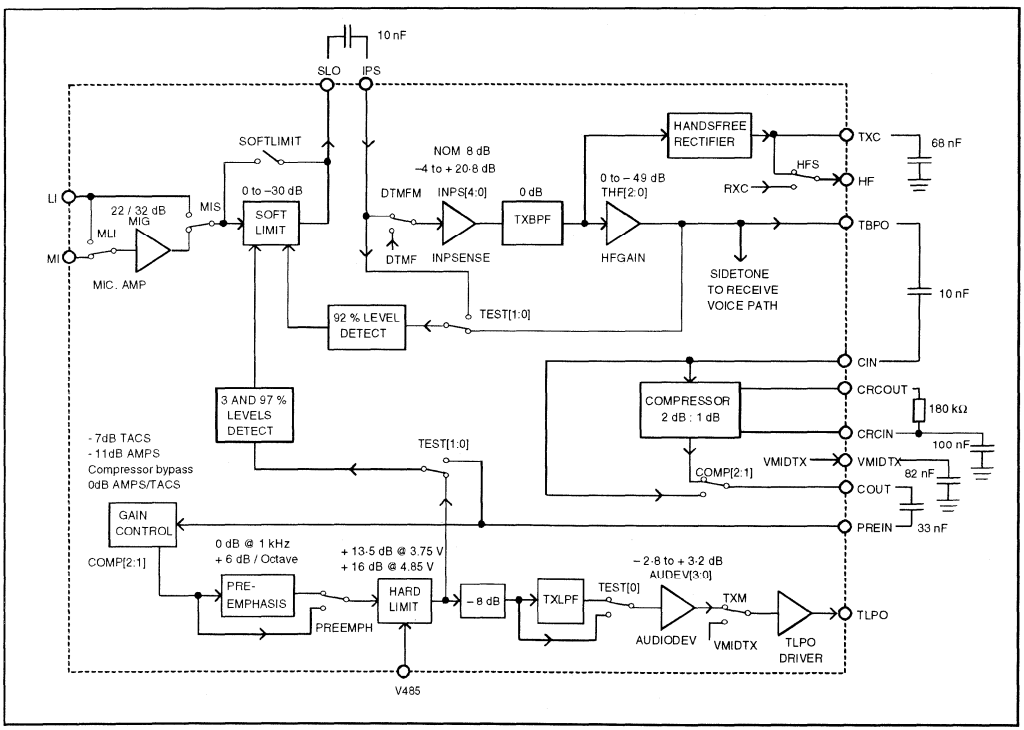


Fig. 11 Transmit Voice Path

TRANSMIT INPUT SIGNAL PRECONDITIONING

Microphone Amplifier (MIG)

Microphone signals input at MI via switch MLI are amplified by a gain selectable amplifier of either 22 dB or 32 dB, controlled by the MIG bit in the "Handsfree mode" control message. The microphone amplifier's input can also be connected to the line input LI via the MLI switch. The microphone amplifier's output drives the soft limiter via switch MIS which also allows higher level signals from the line input LI to bypass the microphone amplifier to drive the soft limiter directly. These two switches are controlled by the MIS and MIL bits in the "Operation mode" control message.

Soft Limiter

Signal amplitude is restricted without clipping to the correct level for F.M. deviation by the soft limiter. This operates as an AGC system, controlled by the signal amplitude at the compressor input and the hard limiter output later in the signal processing path. If the signal is too large at either of these points the soft limiter forward gain is reduced. The nominal soft limiter gain range of 0 to - 30 dB in 64 steps of 0·5 dB covers all normal volume changes occuring during a conversation. Soft limiter attack and decay times are set by internal clocks derived from SCLK and ramp the gain steps at nominal rates of one step down every 40 µs when the signal is too large and one step up every 1·68 ms when the signal is too small.

The soft limiter output at pin SLO is externally coupled with a capacitor to the input pin IPS of the following gain adjust stage, INPSENSE. When the speech channel is used to send DTMF signalling tones a switch, controlled by bit DTMFM in the "Operation mode" control message, selects the internal DTMF signal rather than the speech signal at input IPS.

For test purposes TEST[1:0] bits in the "Initializing Mode 1" control message can configure switches to give access to the softlimiter comparator inputs. When TEST[1:0] bits are high the 3 & 97 % window comparator is switched from the hard limiter output to PREIN input and the 92 % comparator is switched to IPS input.

INPSENSE AMPLIFIER and TXBPF FILTER

Both microphone and transmit voice path tolerances are trimmed in the INPSENSE gain adjustment block following the soft limiter and DTMF switch. INPSENSE has a nominal gain of 8·0 dB with a trim range of - 12·0 to + 12·4 dB relative to the nominal gain set by bits INPS[4:0] in the "Initializing mode" control message.

Transmit signal preconditioning is completed by a bandpass filter TXBPF to limit the audio signal to a speech bandwidth of 300 Hz to 3·4 kHz. This filter uses switched capacitor techniques and is preceded by an anti-alias filter and followed by a smoothing filter to remove the clock from its output. The typical frequency response is shown in figure 4 which also shows the mask defined by type approval limits.

HANDSFREE FUNCTIONAL BLOCKS

Between the transmit bandpass filter and the compressor two extra functions are included for use with handsfree operation. Firstly an attenuator HFGAIN is provided to give progressive signal reduction in handsfree mode with a range of 0 to - 49 dB in 7 dB steps, set by bits THF[2:0] in the "Handsfree mode" control message. The HFGAIN attenuator's output drives pin TBPO which is externally capacitively coupled to the compressor input at pin CIN and internally drives both the soft limiter and sidetone circuits.

The second function provided for handsfree operation is a signal rectifier whose output, filtered by an external capacitor at pin TXC, drives output pin HF via switch HFS with a d.c. transmit level. Switch HFS is controlled by bit HFS in the "Handsfree mode" control message. Under control of bit HFS both receive and transmit levels are available at HF output pin for external comparison to implement the handsfree function. The handsfree system is further described in the section HANDSFREE OPERATION.

COMPRESSOR

ACE9040 provides a 2:1 compressor to halve the transmit dynamic range as required by analog cellular systems. Within the operating signal range each 2 dB change in input level gives a 1 dB change in output level. A transmit signal is input through pin CIN and output on pin COUT, the signal is referenced to a mid-supply voltage. CRCIN and CRCOUT are connections for the external attack and delay time constant setting components.

The compressor's nominal unity gain (unaffected) level is 707 mV. Above this level the signal at CIN is attenuated and below this level the signal is amplified to achieve the 2:1 dB compression. Table 20 gives the nominal, Vmax and Vmin levels at CIN and nominal levels at COUT corresponding with the TACS and AMPS systems for 0 dB, maximum and minimum deviation.

For the usual attack time of 3·0 ms and decay time of 13·5 ms a 180 kΩ resistor is connected between CRCIN and CRCOUT pins and a 100 nF capacitor between CRCIN and GND pins. An 82 nF capacitor should be connected between the VMIDTX and GND pins. Attack and decay time is measured with a 12 dB step, - 8 dB to - 20 dB relative to the unaffected level. Attack and decay times are respectively defined at points on the output envelope where it reaches x 1·5 and x 0·75 of the final steady state level.

External compressor connections allow the use of external coupling capacitors to remove d.c. offsets and optionally an external compander. The compressor can be internally bypassed allowing use of ACE9040 without companding in non-cellular applications, or for test purposes. Bits COMP[2:1] in the "Initializing mode 0" control message control the operation of the internal compander and are used to switch both the transmit compressor and receive expander into or out of the signal path. When not in use the internal compressor and expander are both powered down.

System	Vmax at CIN		Vmin at CIN		Nominal Input at CIN (0dB) levels mVrms	Nominal Output at COUT levels mVrms
	Vrms	dB	mVrms	dB		
TACS	1.0	+ 25	1.77	- 30	56	200
AMPS	1.0	+ 23	2.25	- 30	71	225

Table 20 Compressor CIN and COUT signal levels for TACS and AMPS

FINAL MODULATION PREPARATION

Pre-emphasis

A pre-emphasis filter follows the compressor to boost the amplitude of higher audio frequencies by tilting the frequency response by 6 dB per octave across the whole speech band as shown in figures 5 and 8. To prevent overload in the pre-emphasis filter the signal first passes through an attenuator set to suit the system in use. If an external compander is used or the companding function is bypassed the gain is set to 0 dB. When using the internal compander the gain is set to −7 dB for TACS or −11·0 dB for AMPS. Compander bypass is determined by control bits COMP[2:1]. The pre-emphasis filter and attenuator input is pin PREIN and the output is an internal connection to the hard limiter. The pre-emphasis filter, but not the attenuator, can be bypassed if the PREEMPH bit in the "Operation mode" control message is set to "1".

Hard Limiter

To ensure compliance with the peak deviation specification for cellular telephone systems, a hard limiter follows the pre-emphasis filter to remove any transient level changes that have passed through the soft limiter. This limiter will handle large signals and has symmetrical clipping levels close to the supply rails V_{DD} & V_{SS} (GND). To ensure clipping at the same hard limiter input signal level with both the nominal power supply voltages, hard limiter gain is adjusted by an external pin "V485". For the nominal supply voltages of 4.85 V and 3.75 V gain is respectively 16 dB (V485 pin at "1") and 13.5 dB (V485 pin at "0"). An 8 dB attenuator follows the limiter to prevent any further clipping of the signal in the following transmit lowpass filter.

TX Lowpass Filter TXLPF

A TXLPF lowpass filter with an optimised stop band response limits the signal bandwidth to a cut-off frequency of 3·0 kHz, the frequency response is shown in figure 6. The combined frequency response of the pre-emphasis and lowpass filter stages is shown in figure 8. It is possible for test purposes to bypass this lowpass filter by setting bit TEST[0] in the "Initializing mode 1" control message to a "1".

Speech Deviation Level Setting

A controlled gain stage AUDIODEV sets the output level to give the required FM deviation for speech. The gain is set by bits AUDEV[3:0] in the "Initializing mode 1" control message. AUDIODEV is followed by a transmit audio mute switch enabled by bit TXM in the "Operation mode" control message. A buffer drives output pin TLPO with the transmit speech signal (and DTMF when in use) which is added with DATA/ST and SAT tones in the modulation combiner.

TRANSMIT DATA AND DTMF PATHS

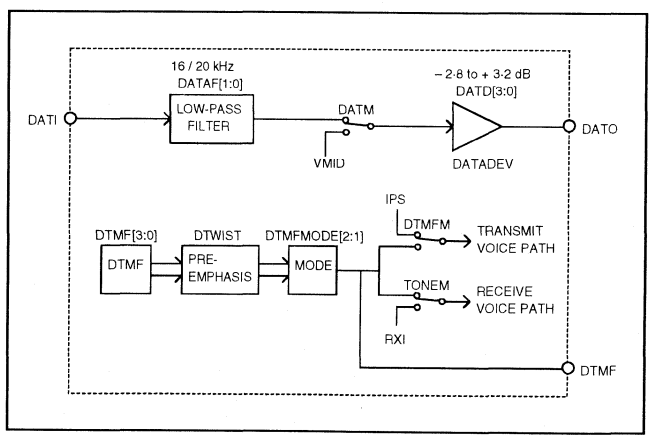


Fig. 12 Transmit Data and DTMF Paths

Transmit Data

Data communication from mobile terminals to base stations in the AMPS and TACS cellular phone systems takes place over the Reverse Control Channel (RECC) during call set-up and in short bursts over the Reverse Voice Channel (RVC) during a call.

RECC or RVC data is transmitted for AMPS or TACS as a 10 kHz or 8 kHz Manchester Coded FSK signal respectively. The data signal is generated by the ACE9050 "System Controller and Data Modem" or similar digital circuit to drive ACE9040's DATI input pin. The DATI input data signal is filtered using a 4th order Butterworth lowpass filter with nominal - 3 dB points of 16 kHz for TACS, or 20 kHz for AMPS. This filter is implemented using switched capacitor techniques and is preceded by a continuous time anti-alias

filter, the output buffer includes a clock rejection filter. The cut-off frequencies are programmed by bits DATAF[1:0] in the "Initializing mode 1" control message. Filtered data passes through the mute switch DATM and a variable gain stage DATADEV with a range of – 2·8 to + 3·2 dB to set the required level of deviation. The mute switch is controlled by bit DATM in the "Operation mode" control message. DATADEV is controlled by bits DATD[3:0] in the "Initialising Mode 1" control message. The data signal is buffered out to pin DATO to drive the modulation combiner.

DTMF

DTMF tones are generated when commanded via the serial interface and conform to the standard CCITT frequencies. All 16 standard tone pairs or any individual tone can be generated. To select DTMF tones data bits for transmission DTMFEN, DTMFMODE[1:0] and DTMF[3:0] need to be set using an "Operation mode" control message. Data bits DTMFMODE[1:0] select low, high or both tones of the pair as shown in table 6. Bits DTMF[3:0] select the tone pair as shown in table 7. DTMFEN set to "1" enables DTMF operation. To change DTMF tones, an "Operation mode" control message with DTMFEN set to "0" must be sent to cancel the previous selection.

An optional pre-emphasis of 2 dB of the high frequency tone group above the level of the low frequency group is enabled by bit DTWIST in the "Initializing mode 0" control message.

DTMF tones can be selected to replace the speech in either or both the transmit and receive paths. In the transmit path setting bit DTMFM to "1" in the "Operation mode" control message will connect the DTMF signal to INPSENSE gain adjustment block's input in place of the speech signal. In the receive path setting bit TONEM to "1" in the "Operation mode" control message will connect the DTMF signal to the input to RXSENSE gain adjustment block in place of the speech input at pin RXI.

DTMF signals are generated as sinewaves by an internal digital to analog converter and are smoothed by the transmit and receive filters. DTMF waveforms start and stop at a zero crossing to avoid transients in the filters and to limit their bandwidth. The DTMF signal is brought out directly on pin DTMF without further buffering.

The DTMF generator is powered down whenever a tone is not being generated, by setting DTMFMODE[1:0] to "00".

TRANSMIT & RECEIVE SAT PATHS

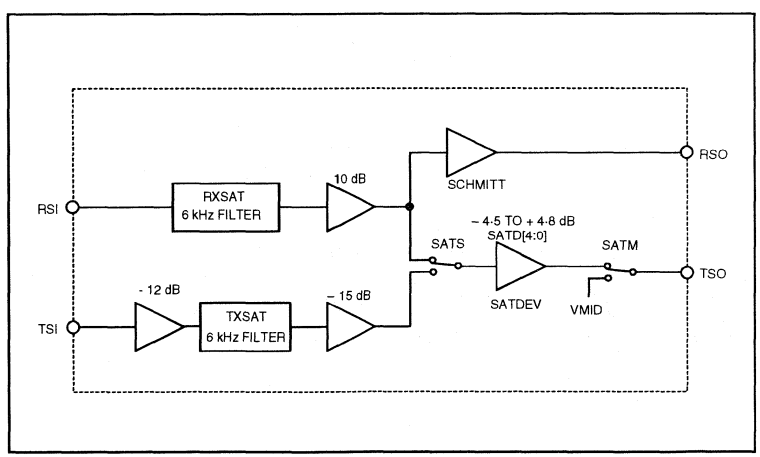


Fig. 13 Transmit and Receive SAT Paths.

Re-transmitted SAT

ACE9040 provides two alternative paths for Supervisory Audio Tones (SAT). The first of these re-transmits the received SAT tone to the base station after narrow band filtering and providing signal level adjustment. This path is selected by setting SATS bit to "0" in the "Initializing mode 1" control message. The baseband signal from the receiver FM discriminator drives the ACE9040 through the RSI pin into the RXSAT 6 kHz bandpass filter required for AMPS or TACS. The recovered SAT signal then passes through a 10 dB amplifier and the SATS selector switch to the deviation setting amplifier SATDEV. This is controlled by bits SATD[4:0] in the "Initializing mode 0" control message. SAT then passes through the SATM mute switch, controlled by bit SATM in the "Operation mode" control message, to output pin TSO for input to the modulation combiner.

Regenerated SAT

The alternative SAT path externally measures the SAT frequency and generates a local tone to match. This route is

selected by setting the SATS bit to "1" in the "Initializing mode 1" control message. The ACE9040 connects the receive filter RXSAT output through a Schmitt trigger to drive pin RSO with a logic level version of the received SAT. A system controller, such as an ACE9050, detects the frequency and generates a digital signal to drive back into the ACE9040 on pin TSI. After the signal level is reduced by -12 dB a 6 kHz bandpass filter TXSAT converts this square-wave into a sinewave. This is followed by a - 15 dB attenuator to reduce the near logic level signal to a normal modulation level. This signal drives the same SATDEV deviation setting stage and mute switch SATM as the returned signal to give an output at TSO.

Base Station Originated SAT

ACE9050, System Controller, can be used to generate a squarewave SAT at 6 kHz which is input to pin TSI and filtered by the TXSAT filter and output at TSO. The RXSAT filter path with its output at RSO, can be used to filter the received SAT from a mobile for verification by an external frequency detector that the mobile is transponding the correct tone. This is the same as the regeneration loop above but starting with generation.

TRANSMIT SIGNAL COMBINER

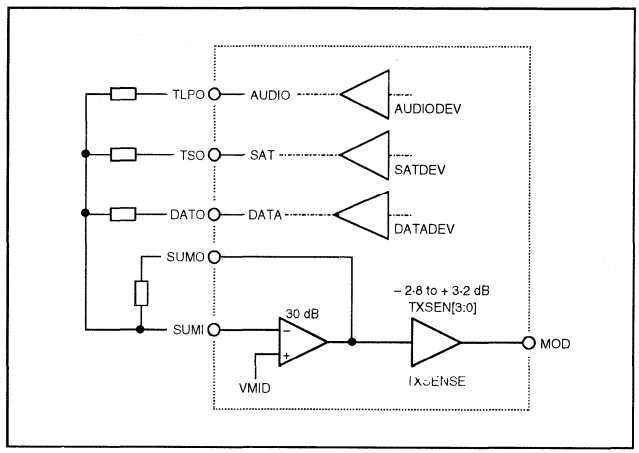


Fig. 14 Transmit Signal Combining Network and Modulation Driver

Used to modulate the transmitted r.f. output, the speech and optional DTMF signals at TLPO, SAT at TSO, and data and ST at DATO, are combined using an internal op-amp. This op-amp has an inverting input at pin SUMI and output at pin SUMO, the non-inverting input is internally biased to VMID. With an external feedback resistor between SUMI and SUMO, external resistors sum the inputs into pin SUMI and are chosen for each different cellular system to select the relative and absolute gains to give the correct deviation for each component of the modulation. Individual fine adjustments to take out component value tolerances can be made by setting: AUDIODEV, SATDEV and DATADEV gains, described in more detail in the sections TRANSMIT VOICE PATH, TRANSMIT AND RECEIVE SAT PATHS, and TRANSMIT DATA AND DTMF PATHS. A fine adjustment is made to the combined signal level by TXSENSE which drives the modulator through pin MOD. The gain of TXSENSE is set by bits TXSEN[3:0] in the "Initializing mode 1" control message over the range – 2·8 to + 3·2 dB.

RECEIVE VOICE PATH

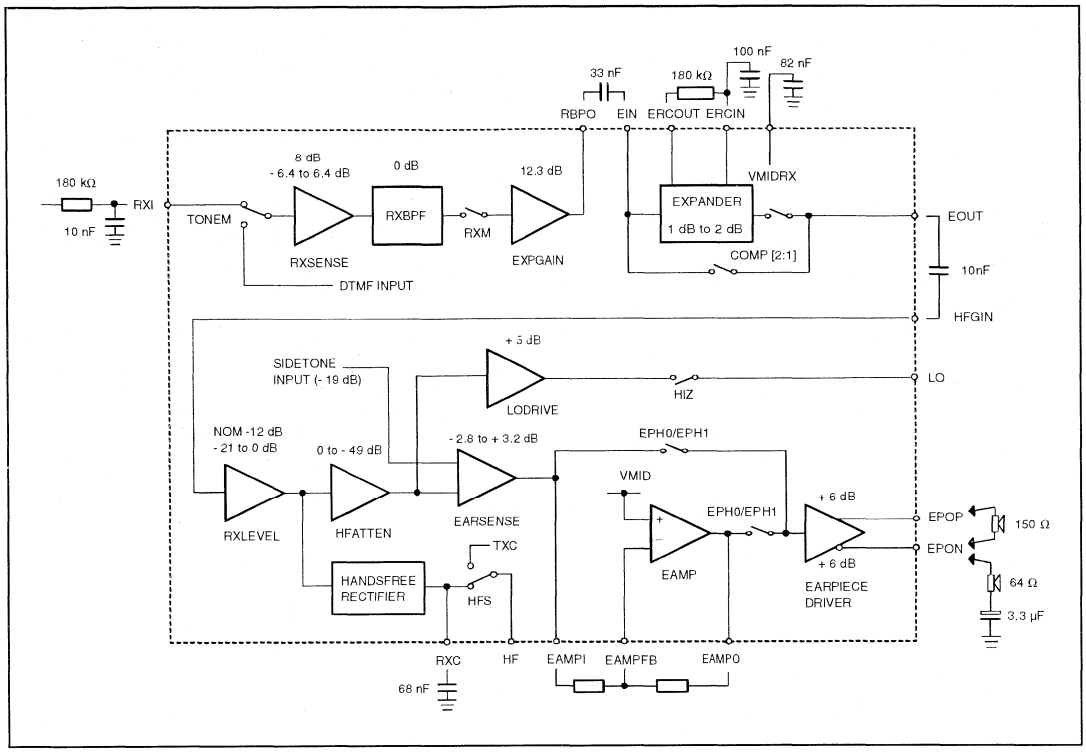


Fig. 15 Receive Voice Path

De-emphasis and Receive Signal Input

Demodulated FM signals drive the RXI input pin via an external de-emphasis lowpass R-C filter of typically 180 kΩ and 10 nF. With TONEM switch set to RXI the input signal is amplified in the block RXSENSE with a gain of + 8 dB. RXSENSE also provides fine adjustment over a range of - 6·0 dB to + 6·4 dB to take up signal level tolerances in the receiver output. Fine gain adjustment is controlled by RXSEN[4:0] bits in the "Initializing mode 0" control message.

When the DTMF generator in the transmit section is in use its output can be switched into the receive path to replace the RXI signal by setting bit TONEM in the "Operation mode" control message to "1". This does not affect the transmitted signal but allows the user to hear DTMF tones to confirm key press operation.

RX Bandpass Filter

The RXSENSE amplifier's output is bandpass filtered to the speech bandwidth of 300 to 3400 Hz by receive bandpass filter RXBPF, as shown in figure 7. RXBPF uses switched capacitor filter techniques but does not include an anti-alias input filter as signals at RXI from the external receiver's output and the internal DTMF generator's output are already bandlimited. The F.M. discriminator output signals from ACE9040's companion device "ACE9030: Radio Interface and Twin Synthesiser" are bandlimited by its output filter and ACE9040's internal DTMF tones are generated as sinewaves without the need for a further anti-aliasing filiter.

RXBPF filter output passes through the receive mute switch controlled by bit RXM in the "Operation mode" control message and is buffered to drive pin RBPO by amplifier EXPGAIN. During mute the RBPO pin is driven to the signal ground voltage at mid supply (as found on pin BIAS). EXPGAIN gain is nominally 12.3 dB when using the internal expander and 0 dB when using an external expander. The output circuit driving RBPO includes a smoothing filter to remove clock noise.

Expander

Input to the expander at pin EIN is coupled by an external capacitor from RBPO to remove any d.c. voltage offsets. Using external coupling also allows the option of using an external compander or bypassing the expander if a linear system is required. In either case the signal should feed back into ACE9040 at pin HFGIN. ACE9040's compander can be bypassed by setting bits COMP[2:1] in the "Initializing mode 0" control message to "00".

A ring tone from the BAR (Beep, Alarm, Ring) generator of ACE9050 "System Controller" can be added to the ex-

pander input EIN by using an external summing network and internally open circuiting the drive to pin RBPO during the tone (not just muting the speech). This is achieved with bits COMP[2:1] in the "Initializing mode 0" control message set to "01".

Signal dynamic range at input pin EIN is doubled in the 1:2 expander to restore the original signal. Within the operating signal range each 1 dB change in input level gives a 2 dB change in output level. The expander output drives pin EOUT which is coupled by an external capacitor to the input pin HFGIN. The external connection allows use of an external compander and removes any d.c. voltage offsets. Bits COMP[2:1] in the "Initializing mode 0" control message can be used to select external companding mode and power down the internal compressor and expander.

The expander's unity gain (unaffected) level EIN to EOUT is 1 V. Above this level gain is applied to the signal at EIN and below this level the signal is attenuated to achieve 1:2 dB expansion. Table 21 gives nominal, Vmax and Vmin levels at EIN and nominal levels at EOUT corresponding with the TACS and AMPS systems for 0 dB, maximum and minimum deviation.

Expander pins ERCIN and ERCOUT are used to set the attack and decay times for the expansion process. For the usual attack time of 3.0 ms and decay time of 13.5 ms, a resistor of 180 kΩ is connected between ERCIN and ERCOUT pins and a capacitor of 100 nF from ERCIN to GND. An 82 nF capacitor should be connected between VMIDRX and GND. Attack and decay time is measured with a 6 dB step, - 4 dB to - 10 dB relative to the unaffected level. Attack and decay times are defined respectively at points on the output envelope where it reaches x 0.57 and x 1.5 of the final steady state level.

Volume Control and Handsfree Attenuator

Two variable gain stages follow the expander, RXLEVEL for the volume control and HFATTEN for use with handsfree mode. Both blocks provide attenuation, expressed as gain to assist system level design, RXLEVEL from 0 to - 21 dB and HFATTEN from 0 to - 49 dB. RXLEVEL is controlled by bits RXV[2:0] in the "Operation mode" control message and HFATTEN is controlled by bits RHF[2:0] in the "Handsfree mode" control message.

RX Audio Output: Line Output and Earpiece

Following the handfree attenuator the signal path splits into two parallel paths: a line output for loudspeaking phones and drivers for a dynamic earpiece or external handsfree earpiece. Bits EPH1 and EPH0 in the "Operation Mode" and "Initializing Mode 0" control messages respectively control the operation of these outputs, see table 5.

The earpiece output path begins with a variable gain stage EARSENSE which is controlled by bits EARS[3:0] in the "Initializing mode 1" control message to give a gain range of - 2·8 to + 3·2 dB. A sidetone signal from the output of the handsfree attenuator HFGAIN at pin TBPO is added at EARSENSE's input if bit SD in the "Initializing mode 0" control message is set to "1". The output of this block is at pin EAMPI.

The signal at pin EAMPI is amplified by an opamp whose gain is set by external resistors, allowing overall gain setting for different models of cellular terminal. A resistor is connected from EAMPI to the amplifier input pin EAMPFB and a feedback resistor is connected from the amplifier output EAMPO to EAMPFB. The ratio of these two resistors sets the gain and the opamp's output including feedback resistors should not be loaded with less than 15 kΩ. Additional filtering can also be added to the receive path using the EAMP opamp.

Earpiece

The earpiece drivers have outputs at pins EPOP and EPON. One of three modes of output drive or a muted output condition is selected by bits EPH1 and EPH0, see table 5.

A dynamic earpiece, typically of 150 Ω resistance in series with 800 µH, can be driven when connected between pin EPON and EPOP. The drive mode can be either differential (EPH1 = 1, EPH0 = 1) or single ended (EPH1 = 1, EPH0 = 0). The differential output, drives a minimum of 4 Vpp into the load. The single ended output appears at EPON and drives a minimum of 2 Vpp into a load referenced to pin EPOP, which provides an output voltage at mid-supply.

Output drive is setup for an external handsfree earpiece with EPH1 = 0 and EPH0 = 1. This load, typically of 64 Ω resistance in series with 3.3 µF, is driven from pin EPON to ground and the EPOP output is put into a high impedance state. The minimum drive into this load is 1.1 Vpp.

The input for the EPOP and EPON output drivers is driven by the signal at the EAMPO pin for single ended and differential outputs or from EAMPI directly for a handsfree earpiece, bypassing the EAMP opamp. The gain from the earpiece drivers' common input, to both EPON's inverting and and EPOP's non-inverting outputs, is nominally + 6 dB.

Line Output

Line output amplifier LODRIVE with its output at pin LO has a gain of + 5 dB and is used to drive an external audio power amplifier. LODRIVE can drive a 1 kΩ load with a minimum of 1 Vrms. The LO output can be put into a high impedance state by setting bit HIZ in the "Operation mode" control message to "0". During power down EPON and EPOP and LO are tied to mid-supply voltage.

HANDSFREE OPERATION

In a handsfree telephone the simplest method of preventing howl round caused by acoustic feedback is to attenuate either the forward or return path until the loop gain is too low for sustained oscillation. The least active path is attenuated so the signal level in each path must be detected and compared so that the quieter can be attenuated.

In the ACE9040 the signal level in both the transmit and the receive paths are rectified, with smoothing capacitors at pins TXC and RXC respectively, to give d.c. voltages corresponding to the signal levels.

A switch HFS with its output at pin HF can be internally toggled between TXC and RXC to allow measurement of the

System	Vmax at EIN		Vmin at EIN		Nominal Input at EIN (0dB) levels mVrms	Nominal Output at EOUT levels mVrms
	Vrms	dB	mVrms	dB		
TACS	1.0	+ 12.5	43	- 15	245	60
AMPS	1.0	+ 12.3	22	-21	245	60

Table 21 Expander EIN and EOUT signal levels for TACS and AMPS

two levels at these pins by an external level sensing circuit such as an analog to digital converter input of ACE9030. The HFS switch is controlled by bit HFS in the "Handsfree mode" control message.

The system controller after comparison of the voltage levels at TXC and RXC pins can attenuate the weaker signal path by up to 49 dB, in 7 dB steps using blocks HFGAIN for transmit and HFATTEN for receive. Bits THF[2:0] and RHF[2:0] in the "Handsfree mode" control message are used to set the gains of HFGAIN and HFATTEN respectively. The rate of change of gain should be limited in the system controller to allow normal conversation.

Attack and decay time constants are set by the resistance and capacitance on the TXC and RXC pins. With the internal resistor to ground of approximately 500 kΩ and an external capacitor to ground of 68 nF the normal attack time of 1 ms and decay time of 35 ms is achieved. By adding a parallel resistor the ratio of attack to decay time can be altered.

To save power in a hand portable when handsfree operation is not needed, the transmit and receive signal rectifiers can be switched off by setting bit HFP in the "Handsfree mode" control message to "0".

BIASES AND REFERENCES

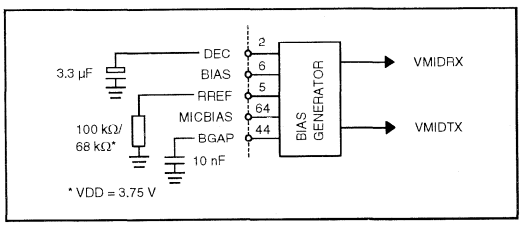


Fig. 16 Bias Circuits

BIAS, VMID and MICBIAS

Within ACE9040 most signals are single ended and swing either side of a mid-supply reference voltage. These internal references are all labelled VMIDxx in this data sheet.

A low impedance voltage source at mid-supply for use as an external signal ground is available on pin BIAS. This is a buffered copy of the voltage at pin DEC which is from an internal high impedance potential divider between V_{DD} and V_{SS}. The DEC pin should be decoupled to ground with a capacitor of greater than 3.3 µF. Two additional buffers provide copies of DEC's voltage at pins VMIDTX and VMIDRX, these are used as internal signal grounds for the transmit and receive paths respectively. VMIDTX and VMIDRX pins should be decoupled to GND with 82 nF capacitors. By using separate mid-supply signal grounds crosstalk due to the compander time constant circuits and the speech and tone signals are kept to a minimum.

Pin MICBIAS gives the bias needed for an electret microphone nominally 0·8 times V_{DD}, e.g. when V_{DD} is 3·75 V MICBIAS = 3 V

OP-AMP Reference Current

Reference currents for all the internal op-amps are set by an external resistor connected from pin RREF to ground (V_{SS}). Nominal values are 100 kΩ for V_{DD} = 4·85 V and 68 kΩ for V_{DD} = 3·75 V. A stable discrete resistor should be used to ensure consistent operation over a wide temperature range.

Power Supply Comparator - Reset Output

A power supply comparator is provided to give a reset at power-on and enable the system controller to initiate a clean shut-down sequence if the battery voltage falls too low. When V_{DD} is below a band-gap derived threshold the open-drain outut pin LVN drives to a logic low. This occurs for V_{DD} exceeding 1 V but less than a typical threshold of 3·35 V. An external resistor at LVN provides a pull-up to V_{DD} with a capacitor to ground (V_{SS}) to give a power-on reset delay. Typical values for RC are 220 kΩ and 150 nF. This RC combination also removes short transients or noise pulses from the signal at LVN during power up. If this comparator is not required the bandgap and comparator can be powered down by setting bit PDLVC in the "Initializing mode 0" control message to a "1".

Serial Data Clock

All switched capacitor filter switching clocks are derived from the serial data clock SCLK which must be fixed at 1·008 MHz to ensure correct frequency responses.

AMPLIFIER

An uncommitted op-amp is provided with its non-inverting input internally connected to VMID, inverting input at pin AMPI and output at pin AMPO.

APPLICATIONS INFORMATION

To help with system set up tables 22 to 25 show ACE9040's functions and their respective controlling bits. Table 23 shows the gains and filter characteristics predetermined when setting the TACS & AMPS cellular system selection bits. Tables 23 & 24 show these functions respectively for the transmit and receive sections of ACE9040. Table 25 shows the four control messages with an example of the data to turn all ACE9040 functions on.

Function Controlled by TACS & AMPS Bits			
		TACS	AMPS
Internal pre-emphasis gain control.	TACS = - 7.0 dB AMPS= - 11.0 dB	1 0	0 1

Table 22 Functions Controlled by TACS & AMPS Bits

Gain and filter set-ups for TACS, AMPS and user control bits: Transmit			
	TACS	AMPS	User control bit(s)
Microphone amp	22 or 32 dB	22 or 32 dB	MIG
Soft limiter	0 to - 30 dB	0 to - 30 dB	Internal
INPSENSE gain adjust	+ 8 dB (- 12.8 to + 12 dB)	+ 8 dB (- 12.8 to + 12 dB)	INPS[4:0]
TXBPF TX bandpass filter	0 dB	0 dB	Fixed
HFGAIN, TX Handsfree attenuator	0 to - 49 dB	0 to - 49 dB	THF[2:0]
Compressor: Compression about unaffected level. (707 mVrms, - 3 dBV)	2:1[1]	2:1[1]	Fixed
Pre-emphasis gain control (Internal compressor)	- 7 dB	- 11 dB	TACS & AMPS
Pre-emphasis gain control	0 dB	0 dB	Fixed
HARD LIMIT, Hard deviation limiter	+ 16.5 dB @ 4.85V + 13.5 dB @ 3.75V	+ 13.5 dB @ 3.75V + 16.5 dB @ 4.85V	V485 pin
TXLPF TX low pass filter	- 8 dB	- 8 dB	Fixed
AUDIODEV,	0 dB (-2.8 to + 3.2 dB)	0 dB (-2.8 to + 3.2 dB)	AUDEV[3:0]
TXSENSE, signal	0 dB (-2.8 to +3.2 dB)	0 dB (-2.8 to +3.2 dB)	TXSEN[3:0]
Nominal TX Channel Gain (bypassed compressor)	28.5[2] dB @ 3.75 V 31.5[2] dB @ 4.85 V	23.5[2] dB @ 3.75 V 26.5[2] dB @ 4.85 V	

Notes: 1. Above the unaffected (0 dB gain) level the compressor attenuates and below this level it provides gain.
2. MIC gain = 22 dB

Table 23 Transmit gain and filter set-ups for TACS, AMPS and user control bits

Gain and filter set-ups for user control bits: Receive			
	TACS	**AMPS**	**User control bit(s)**
External De-emphasis	- 21 dB[1]	- 21 dB[1]	Fixed externally
RXSENSE: Receive audio gain	+ 8 dB	+ 8 dB	Fixed
RXSENSE: Receive audio gain adjustment range	- 6 to + 6.4 dB	- 6 to + 6.4 dB	RXSEN[4:0]
RXBPF: RX bandpass filter	0 dB	0 dB	Fixed
RX Expander gain EXPGAIN: Internal	+ 12.3 dB	+ 12.3 dB	Fixed
RX Expander gain EXPGAIN: External	0 dB	0 dB	Fixed
Expander: Expansion about unaffected level (1000 mV, 0 dBV)	1:2[2]	1:2[2]	Fixed
RXLEVEL, Receive volume control	- 12 dB (+ 12 to - 9 dB)	- 12 dB (+ 12 to - 9 dB)	RXV[2:0]
HFATTEN, RX handsfree attenuator	0 to - 49 dB	0 to - 49 dB	RHF[2:0]
EARSENSE	0 dB (- 2.8 to + 3.2 dB)	0 dB (- 2.8 to + 3.2 dB)	EARS[3:0]
Ear piece driver	6 dB	6 dB	Fixed
Nominal Receive Gain	- 6.7 dB	- 6.7 dB	Fixed
(Expander bypassed)			
DATA and SAT Filters			
TX data path filter cut-off	16 kHz	20 kHz	DATAF[1:0]
TX & RX bandpass SAT filter centre frequency	6 kHz	6 kHz	Fixed

Notes: 1. Attenuation with an external de-emphasis network of series 180 kΩ with 10 nF to GND at RXI input.
2. Above the unaffected (0 dB gain) level the expander provides gain and below this level it attenuates.

Table 24 Receive, Data and SAT gain and filter set-ups for user control bits

OPERATING MODE								
WORD/BIT	D7	D6	D5	D4	D3	D2	D1	D0
DATA 1	PREEMPH	MIS	DTMF3	DTMF2	DTMF1	DTMF0	TONEM	DTMFM
DATA 2	DTMFMODE1	DTMFMODE0	DTMFEN	MLI	TXM	DATM	SATM	RXM
DATA 3	EPH1	HIZ	RXV2	RXV1	RXV0	PD	0	1
START-UP BIT SETTINGS								
DATA 1	0	0	0	0	0	0	0	0
				00_{HEX}				
DATA 2	0	0	0	0	1	1	1	1
				$0F_{HEX}$				
DATA 3	1	1	1	1	1	0	0	1
				$F9_{HEX}$				

INITIALIZING MODE 0								
WORD/BIT	D7	D6	D5	D4	D3	D2	D1	D0
DATA 1	SOFTLIMIT	SD	SATD4	SATD3	SATD2	SATD1	SATD0	RXSEN4
DATA 2	RXSEN3	RXSEN2	RXSEN1	RXSEN0	INPS4	INPS3	INPS2	INPS1
DATA 3	INPS0	COMP2	COMP1	PDLVC	DTWIST	EPH0	0	0
START-UP BIT SETTINGS								
DATA 1	1	0	1	0	0	0	0	1
				$A1_{HEX}$				
DATA 2	0	0	0	0	1	0	0	0
				08_{HEX}				
DATA 3	0	1	0	0	1	1	0	0
				$4C_{HEX}$				

INITIALIZING MODE 1								
WORD/BIT	D7	D6	D5	D4	D3	D2	D1	D0
DATA 1	EARS3	EARS2	EARS1	EARS0	AUDEV3	AUDEV2	AUDEV1	AUDEV0
DATA 2	DATD3	DATD2	DATD1	DATD0	TXSEN3	TXSEN2	TXSEN1	TXSEN0
DATA 3	TACS	DATAF1	DATAF0	SATS	TEST1	TEST0	1	0
START-UP BIT SETTINGS (TACS)								
DATA 1	1	0	0	0	1	0	0	0
				88_{HEX}				
DATA 2	1	0	0	0	1	0	0	0
				88_{HEX}				
DATA 3	1	1	0	0	0	0	1	0
				$C2_{HEX}$				

HANDSFREE								
WORD/BIT	D7	D6	D5	D4	D3	D2	D1	D0
DATA 1	X	X	X	X	X	0	0	0
DATA 2	0	X	AMPS	X	X	MIG	HFS	HFP
DATA 3	RHF2	RHF1	RHF0	THF2	THF1	THF0	1	1
START-UP BIT SETTINGS								
DATA 1	X	X	X	X	X	0	0	0
				00_{HEX}				
DATA 2	0	X	0	X	X	0	0	1
				01_{HEX}				
DATA 3	0	0	0	0	0	0	1	1
				03_{HEX}				

Table 25 Control Messages

ACE9050

SYSTEM CONTROLLER AND DATA MODEM

ACE9050 provides the control, peripheral and interface functions needed for AMPS or TACS analog cellular telephones.

ACE9050 contains an embedded 8 bit microcontroller with ROM, RAM and a serial communications interface. Peripheral functions include an AMPS/TACS data modem, I/O ports, watchdog, inter-chip serial interfaces, two pulse width modulators, IFC counter, tone generator, and crystal oscillator. ACE9050 can be put into processor emulation mode for software de-bugging.

The device uses GEC Plessey Semiconductors sub micron CMOS technology for low power and high performance.

Several power down modes are incorporated in the device for battery economy.

FEATURES

- Low Power Low Voltage (down to 3·6 V) Operation
- Power Down Modes
- Program Compatibility with Industry Standard Microcontroller
- AMPS and TACS Compatible Modem
- Processor Independent Watchdog
- SAT Detection, Generation and Loopback
- Internal RAM
- Interface to FLASH and EEPROM Memories
- I/O Ports for Keyboard Scanning and Display Driving.
- I²C Interface for Display
- Part of the ACE Integrated Cellular Phone Chipset
- TQFP 100 Pin Package.

APPLICATIONS

- AMPS, and TACS Cellular Telephone
- Two-Way Radio Systems

RELATED PRODUCTS

ACE9050 is part of the following chipset:

- ACE9010 R.F Front End with VCO
- ACE9020 Receiver and Transmitter Interface
- ACE9030 Radio Interface and Twin Synthesiser
- ACE9040 Audio Processor.

ORDERING INFORMATION

Industrial temperature range
TQFP 100 lead with 0·5 mm pin pitch, code FPD100
ACE9050/IG/FP1R - devices shipped in trays
ACE9050/PR/FP1R - pre-production

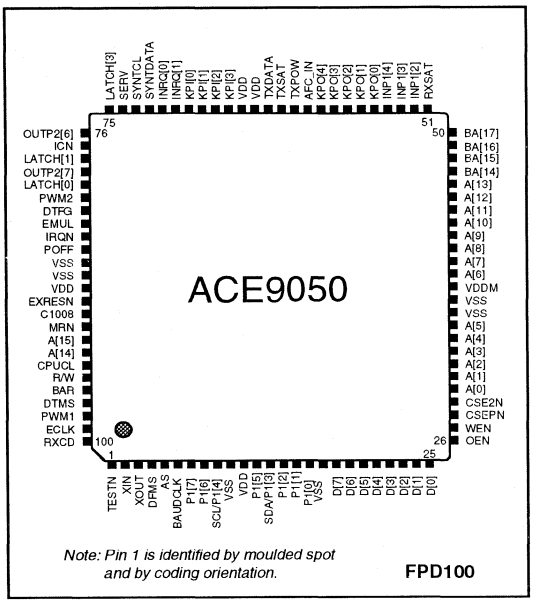


Fig.1 Pin connections - top view

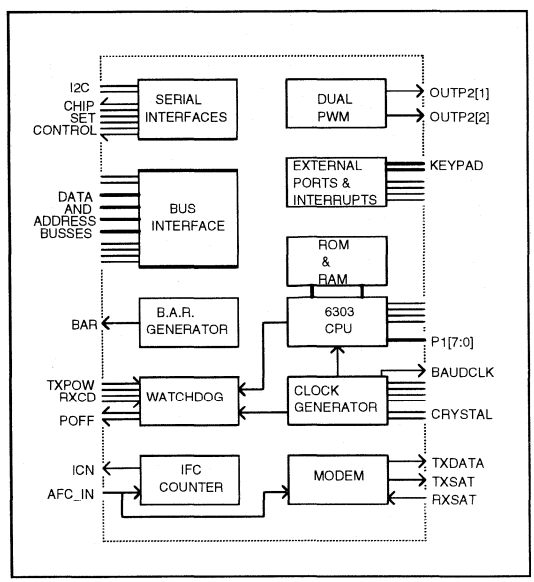


Fig. 2 ACE9050 Simplified Block Diagram

PIN DESCRIPTIONS

Pin No.	Name	Type	Block	Description
1	TESTN	I	CLK/WADO	0 = Test mode: Counter chains split and access test register.
2	XIN	I	CLK	Crystal Connection/ CMOS input: 8.064 MHz
3	XOUT	O	CLK	Crystal Connection
4	DFMS	I/O	CPU	Serial inteface (UART) output
5	AS	I	BINT	Address strobe (Latch address during emulation)
6	BAUDCLK	O(I)	BAUD	8 x CPU baud rate for emulation (input in test mode)
7	P1[7]	I/O	CPU	PORT 1 of CPU
8	P1[6]	I/O	CPU	PORT 1 of CPU
9	P1[4]/SCL	I/O	CPU and I²C	PORT 1 of CPU or I²C SCL
10	V_{SS}			Ground
11	V_{DD}			Digital supply
12	P1[5]	I/O	CPU	PORT 1 of CPU
13	P1[3]/SDA	I/O	CPU and I²C	PORT 1 of CPU or I²C SDA
14	P1[2]	I/O	CPU	PORT 1 of CPU
15	P1[1]	I/O	CPU	PORT 1 of CPU
16	P1[0]	I/O	CPU	PORT 1 of CPU
17	V_{SS}			Ground
18	D[7]	I/O	BINT	Data Bus (multiplexed address and data input for emulation)
19	D[6]	I/O	BINT	Data Bus (multiplexed address and data input for emulation)
20	D[5]	I/O	BINT	Data Bus (multiplexed address and data input for emulation)
21	D[4]	I/O	BINT	Data Bus (multiplexed address and data input for emulation)
22	D[3]	I/O	BINT	Data Bus (multiplexed address and data input for emulation)
23	D[2]	I/O	BINT	Data Bus (multiplexed address and data input for emulation)
24	D[1]	I/O	BINT	Data Bus (multiplexed address and data input for emulation)
25	D[0]	I/O	BINT	Data Bus (multiplexed address and data input for emulation)
26	OEN	O	DEC	Output enable
27	WEN	O	DEC	Write enable
28	CSEPN	O	CSCTRL	Chip select external EPROM
29	CSE2N	O	CSCTRL	Chip select external EEPROM
30	A[0]	O	BINT	Address line
31	A[1]	O	BINT	Address line
32	A[2]	O	BINT	Address line
33	A[3]	O	BINT	Address line
34	A[4]	O	BINT	Address line
35	A[5]	O	BINT	Address line
36	V_{SS}			Ground
37	V_{SS}			Ground
38	V_{DDM}			Digital supply for memory interface
39	A[6]	O	BINT	Address line
40	A[7]	O	BINT	Address Line
41	A[8]	O(I)	BINT	Address line (input during emulation)
42	A[9]	O(I)	BINT	Address line (input during emulation)
43	A[10]	O(I)	BINT	Address line (input during emulation)
44	A[11]	O(I)	BINT	Address line (input during emulation)
45	A[12]	O(I)	BINT	Address line (input during emulation)
46	A[13]	O(I)	BINT	Address line (input during emulation)
47	BA[14]	O	BINT	Address line (extended address from bank select segister)
48	BA[15]	O	BINT	Address line (extended address from bank select segister)
49	BA[16]	O	BINT	Address line (extended address from bank select segister)
50	BA[17]	O	BINT	Address line (extended address from bank select segister)
51	RXSAT	I	MODEM	SAT detector input TACS and AMPS
52	INP1[2]	I	EPORT	Bit 2 input Port 1
53	INP1[3]	I	EPORT	Bit 3 input Port 1
54	INP1[4]	I	EPORT	Bit 4 linput Port 1
55	KPO[0]	O	EPORT	Keypad scan output or output port
56	KPO[1]	O	EPORT	Keypad scan output or output port
57	KPO[2]	O	EPORT	Keypad scan output or output port
58	KPO[3]	O	EPORT	Keypad scan output or output port
59	KPO[4]	O	EPORT	Keypad scan output or output port
60	AFC_IN/ RXDATA	I	IFC/MODEM	54/450 kHz IF Input

PIN DESCRIPTIONS (continued)

Pin No.	Name	I/O	Block	Description
61	TXPOW	I	WADO	Power detect from transmitter
62	TXSAT	O	MODEM	SAT output (TACS/AMPS)
63	TXDATA	O	MODEM	TACS/AMPS modem output
64	V_{DD}			Digital supply
65	V_{DD}			Digital supply
66	KPI[3]	I	EPORT	Keypad scan input or input port
67	KPI[2]	I	EPORT	Keypad scan input or input port
68	KPI[1]	I	EPORT	Keypad scan input or input port
69	KPI[0]	I	EPORT	Keypad scan input or input port
70	INRQ[1]	I	EPORT	External interrupt (also bit 1 input port 1)
71	INRQ[0]	I	EPORT	External interrupt (also bit 0 input port 1)
72	SYNTDATA	O	SINT	Data to PLL
73	SYNTCL	O	SINT	Non-continuous clock to PLL 126 kHz
74	SERV	I	WADO	Watchdog inhibit
75	LATCH[3]	O	SINT	Latch of programmable length for ACE9030 synthesiser.
76	OUT2[6]	O	EPORT	Output port 2 bit 6 (10mA drive) LED driver
77	ICN	O(I)	IFC	IF counter output for emulation (input in test mode)
78	LATCH[1]	O	SINT	Latch output (to ACE9030 receiver interface)
79	OUTP2[7]	O	EPORT	Output port 2, bit 7, LED driver (10mA drive)
80	LATCH[0]	O	SINT	Latch output (to ACE9040)
81	OUTP2[2]/ PWM2/ LATCH[2]	O	PWM SINT	Output port 2, bit 2 / pulse width modulator number 2 output / latch output
82	DTFG	I/O	SINT	Bi-directional serial inter-chip data
83	EMUL	I	CPU	CPU emulation mode
84	IRQN	O(I)	CPU	CPU Interrupt for emulation (input in test mode)
85	POFF	O	WADO	Power on/off
86	V_{SS}			Ground
87	V_{SS}			Ground
88	V_{DD}			Digital supply
89	EXRESN	O	WADO	External reset output
90	C1008	O	CLK	1·008 MHz clock for serial inter-chip data
91	MRN	I	WADO	0 = Chip reset
92	A[15]	I	BINT	Address input for emulation only
93	A[14]	I	BINT	Address Input for emulation only
94	CPUCL	O	CLK	8.064 MHz clock input to SIS module
95	R/W	O(I)	BINT	Read / Write (input during emulation)
96	BAR	O	BAR	Beep / Alarm / Ring Tone output
97	DTMS	I/O	CPU	Serial inteface (UART) input
98	OUTP2[1]/ PWM1	O	PWM	Output port 2, bit 1, / Pulse width modulator number 1 output
99	ECLK	O(I)	CLK	Processor clock (input during emulation)
100	RXCD	I	WADO	Carrier detect from RX

Abbreviations

BAR	Beep, Alarm & Ring Tone generator	EPORT	External port
BAUD	Baud rate generator	I²C	I²C interface
BINT	Bus interface	IFC	IFC counter
CSCTRL	Chip select control	MODEM	AMPS and TACS modem
CLK	Clock generator	SINT	Serial inter-chip interface
CPU	6303 processor unit, UART and counter/timer	WADO	Watchdog

ELECTRICAL CHARACTERISTICS

V_{DD} = 3·75 ± 0·15 V. and T_{AMB} = – 40 °C to +85 °C.

Parameter	Min.	Typ.	Max.	Unit
Supply Current				
Sleep		100		µA
Fully operating (Note 1)		10		mA
Bus clock frequency		1008		kHz

Note 1: Depending on the modes selected and the current activity the supply current will generally be substantially less than this peak figure.

BLOCK DESCRIPTIONS

PROCESSOR UNIT

The processor unit is program compatible with the standard 6303. It contains the following hardware: a Serial Communications Interface (SCI), an 8 bit data bus, a 16 bit address bus, a timer, an 8 bit I/O port (P1), and an SCI interface port (P2).

The 6303 NMI Interrupt and Standby modes are not needed in a cellular phone and so are not supported. The processor can run at 1·008 MHz or at 2·016 MHz in Turbo mode. Up to 256 K of programme space can be accessed by using a paged addressing scheme. In Emulation mode the internal processor is bypassed to allow software development on an external processor.

MEMORY

The ACE9050 contains the following internal Memory:

512 bytes of ROM
6144 bytes of RAM

The ROM code facilitates the programming of FLASH memory via the SCI, and system initiation after a Reset.

The Internal RAM area represents the total RAM requirement anticipated for a cellular phone system. Along with the internal registers this occupies 6 K of programming space.

BUS INTERFACE and CONTROL

This block creates the Data, Address and Control lines for the external memory. The external address bus is expanded from the standard 16 bits up to 18 bits by a banked addressing scheme for the upper four bits. This increases the memory address space from 65 K to 256 K. Chip selects for both FLASH and EEPROM are included as are separate read and write lines. The internal ROM area can be mapped to the external memory space.

In Emulation mode this block creates the interface to the external processor.

EXTERNAL PORTS AND INTERRUPTS

The ACE9050 contains two keypad interface ports, two maskable external interrupts, and standard logic level input and output ports. The Keypad interface ports can be also be configured as standard ports. Two high current outputs are provided in one port for direct control of features such as LCD back-lighting

SERIAL CHIP INTERFACES

Two serial interface protocols are supported. One is the standard I^2C interface. The other is a dedicated interface to the ACE9030 Radio Interface and Twin Synthesiser and the ACE9040 Audio Processor. This supports serial data transfer at a rate of 1·008 MHz on a single bi-directional data line with associated Latch pulses to direct the data flow. The facility to programme the length of the synthesiser Latch pulse is provided to control speed-up mode duration if required.

BEEP, ALARM and RING TONE GENERATOR

The Beep, Alarm, and Ring Tone, BAR, generator is intended to drive the acoustic tone transducer. It has a single digital pulse train output which is enabled and disabled under software control. The On and Off times of the output pulses are determined via software to vary the frequency, signal period, and volume of the tone. The resolution of the pulse on and off times is 7·9 µs with a maximum time of 2·02 ms.

MODEM

The Modem provides a two way data transfer over the radio link between a base station and the on board Processor and supports the two cellular systems AMPS and TACS.

Data input can either be a 54 kHz sampled version of the IF or the 450 kHz IF direct with CMOS Logic Levels. Various data discrimination and decoding schemes can be selected by software. A squelch level is set by software so that the quality of each data byte can be assessed. The decoder contains a word sync detector, but no manipulation of data is made in the encoder so error correcting bits must be generated by the software.

SAT detection and generation at the standard three frequencies of 5970, 6000, and 6030 Hz is included. The SAT output can be switched between the internal SAT generator and the external SAT tone input as a loop back to transpond the receiver tone without further processing.

WATCHDOG and POWER CONTROL

The Watchdog function will provide an internal and external Reset. This will occur if the processor does not make a write access to a defined address every 4 seconds. During power up and reset conditions the watchdog is held in reset, and prevented from counting.

The Power control function is provided to control power switching of the Radio circuits to initiate correct start-up and to conserve battery current. The serial bus can be used to control power in the other ACE series circuits.

Two logic inputs exist for the Transmit power level and the Receive carrier strength monitoring and are gated so that if the Radio is Transmitting without Receiving for a set amount of time a Power Switch Off sequence is initiated as an autonomous time-out. This will also occur if the Power control Logic is not serviced by the Processor in a 30 second period.

Both the Watchdog and the Power Control can be inhibited via an external pin for development work or if not required.

IFC COUNTER

The Intermediate Frequency Control (IFC) Counter is used as part of the AFC Loop. The IFC Counter provides a pulse after a set number of IF input pulses. This number can be set in software to suit an IF input of either 54 kHz or 450 kHz. Pin AFCOUT on the ACE9030 is normally used and gives the 54 kHz signal. The sample will always be large enough to filter out frequency shifts caused by data and speech modulation.

The IFC Counter output is internally connected to the Processor block and also drives an external pin for development work.

TWIN PULSE WIDTH MODULATORS

Two independently programmable Pulse Width Modulators (PWMs) are available. The high time of the PWM can be

programmed using an eight bit register. The cycle time is set to 254 µs and the high time is programmable in approximately 1 µs steps. The PWM outputs are multiplexed with the Output port to reduce Chip pin count.

CLOCK GENERATOR

The Clock Generator provides all the various internal clocks required from an 8·064 MHz source. A Crystal Oscillator is provided if the system designer chooses to use a local Crystal frequency source, however, when the ACE9030 is used in the system it provides a suitable clock output derived from the synthesiser reference frequency.

External clock outputs are also provided to aid system design, at the Processor clock rate and at 8·064 MHz.

A 1·008 MHz clock output is also provided as part of the serial interface to the ACE9030 and ACE9040 and also to drive the filters in the ACE9040.

EMULATION MODE

This is intended as a test mode where the use of an external processor is possible. This mode is activated by setting the logic level on the pin EMUL. In Emulation mode the pins ECLK, AS, RW, IRQ, and A[8:15] become inputs and the data pins D[7:0] become multiplexed Address and Data line inputs. These are latched internally to produce separate address and data busses. These lines can interface directly to a standard external 6303 type microprocessor such as the HD6303R.

POWER DOWN MODES

To reduce overall power consumption selective power down of various blocks is available under software control. In the power down state each block will go to a predetermined logic state. The following blocks and outputs can be switched off:

Bus Interface
8·064 MHz external Clock
1·008 MHz external Clock
AMPS/TACS Modem
Serial Chip Interface

Section 5
PCM Circuits

MV1442

HDB3 ENCODER/DECODER/CLOCK REGENERATOR

(Supersedes June 1993 edition)

The MV1442, along with other devices in the GPS 2Mbit PCM signalling series comprise a group of circuits which will perform the common channel signalling and error detection functions for a 2.048Mbit PCM transmission link operating in accordance with the appropriate CCITT recommendations. The circuits are fabricated in CMOS and operate from a single +5V supply with all inputs and outputs being TTL compatible.

The MV1442 is an encoder/decoder for the HDB3 pseudo–ternary transmission code, described in Annex A of CCITT Recommendation G. 703. The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of the HDB3 coding, all ones detection and loss of input (all zeros detection). In addition a loop back function is provided for terminal testing. The MV1442 may be selected to function in either internal or external clock recovery modes. Internal clock recovery mode may be selected for either 1.544MHz or 2.048MHz operation and in this mode an external 16.384MHz crystal (12.352MHz for 1.544MHz Operation) is required. External clock recovery mode may be selected for 1.544MHz, 2.048MHz or 8.448MHz operation.

FEATURES

- On–chip Digital Clock Regenerator
- HDB3 Encoding and Decoding to CCITT Recommendation G.703
- Asynchronous operation
- Simultaneous Encoding and Decoding
- Clock Recovery signal allows Off–chip Clock Regeneration
- Loop Back Control
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm
- Low Power Operation
- 2.048MHz or 1.544MHz Operation in External or Internal Clock Recovery mode
- 8.448MHz Operation in External Clock Recovery mode

ORDERING INFORMATION

MV1442/IG/DPAS DIL plastic package
MV1442/IG/DGAS DIL cerdip package
MV1442/IG/MPES Minature plastic package

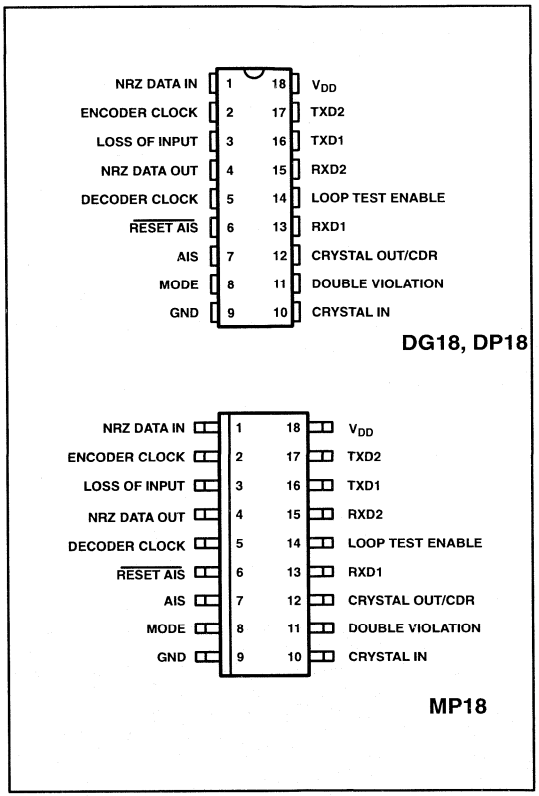


Fig. 1: Pin connections – top view

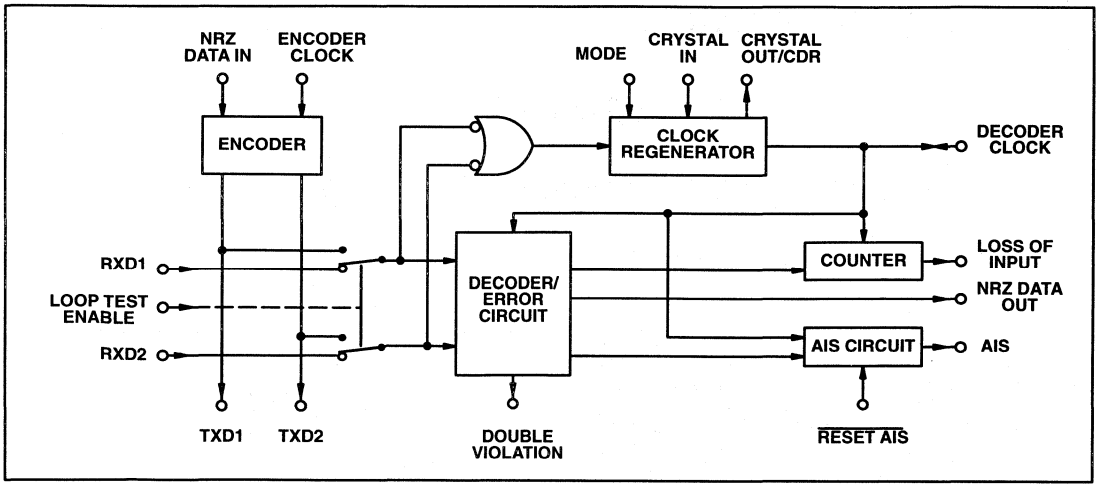


Fig. 2: Block diagram

FUNCTIONAL DESCRIPTION

High Density Bipolar 3 (HDB3) is a pseudo–ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to allow adequate clock recovery at the receiver. In any sequence of four consecutive binary zeros, the last zero is substituted by a mark of the same polarity as the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code, and ensures that successive violations alternate in polarity and as such introduce no DC component to the HDB3 signal.

The MV1442 consists of three main blocks, the HBD3 Encoder, the HDB3 Decoder and the Clock Regenerator. The function of each block is now described separately.

HDB3 ENCODER

The HDB3 Encoder is responsible for converting the incoming NRZ data into pseudo–ternary form for transmission over a PCM link. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703. The data to be encoded is input on the NRZ DATA IN pin and the encoding process is synchronised to the clock signal being input on the ENCODER CLOCK pin. The two TXD outputs, TXD1 and TXD2, represent the HDB3 data in pseudo–ternary form. If a mark is to be transmitted the output goes high after the rising edge of the clock. The length of the pulse is set by the positive clock pulse width. The timing diagram of the HDB3 Encoder is shown in Fig.3.

HDB3 DECODER

The HDB3 Decoder is responsible for decoding the HDB3 pseudo–ternary data on its inputs RXD1 and RXD2, into NRZ form to be output on the NRZ DATA OUT pin. In addition to this the decoder circuit provides three alarm outputs. The first of these alarms is DOUBLE VIOLATION. As its name suggests, a logic high on this output denotes that two successive violations have been received with the same polarity, thus violating the HDB3 coding laws. The second alarm, LOSS OF INPUT, is used to denote that 11 consecutive zeros have been received on the RXD inputs. The final alarm output is AIS (All ones). This alarm goes high if less than 3 decoded zeros have been detected in the preceding RESET AIS = 1 period (i.e. between RESET AIS = 0 pulses) and as such this alarm can be used as an all ones' detector. The decoding process and all the alarm circuitry is synchronised to the clock signal being input to this block on the DECODER CLOCK pin. This clock signal may be asynchronous with the ENCODER CLOCK signal. The timing diagrams of the HDB3 Decoder and alarm circuitry are shown in Figs. 4 to 7.

In addition to the normal mode of operation, a loop test mode is available for terminal testing. This mode is selected by taking the LOOP TEST ENABLE input high. In this mode, the HDB3 encoded pseudo–ternary data outputs of the Encoder block are fed back as the inputs to the Decoder block, which in turn decodes this data and outputs it in NRZ form.

CLOCK REGENERATOR

The Clock Regenerator block has two possible modes of operation. With the MODE pin high, internal crystal controlled clock regeneration is selected whilst with the MODE pin low, external clock regeneration is selected, using, for example, a tuned circuit.

In external clock regeneration mode, a logically 'OR'ed version of the HDB3 data, from the RXD inputs, is output to the external clock regeneration circuitry on the CRYSTAL OUT/CDR pin. The regenerated clock is then fed back into the MV1442 on the DECODER CLOCK pin. External clock regeneration may be used for operation with data rates of 1.544Mbits, 2.048Mbits or 8.448Mbits.

In internal clock regeneration mode, the logically 'OR'ed data is input to a digital regenerator, which constantly resynchronises a divide–by–8 counter to the incoming data stream. The clock thus regenerated is output to the decoder circuitry and to any external circuitry on the DECODER CLOCK pin. A crystal of frequency 8 times the required data rate must be connected between the CRYSTAL IN and CRYSTAL OUT/CDR pins. Thus the crystal frequency needs to be 16.384MHz or 12.352MHz for data rates of 2.048Mbits or 1.544Mbits respectively. Internal clock regeneration may not be used for operation at a data rate of 8.448Mbits.

The MV1442 is capable of withstanding up to 0.25UI of peak to peak input jitter at a jitter frequency of 2.048MHz without introducing errors into the decoded data. At lower jitter frequencies, the MV1442 is capable of withstanding much larger values of peak to peak input jitter. In the absence of input jitter, the MV1442 will produce an output jitter waveform in the form of a sawtooth ramping between 0UI and 0.125UI. The period of this waveform will be dependent upon the difference

in frequencies between the remote transmitters clock and the crystal controlled clock of the MV1442.

The MV1442 was originally designed as a pin compatible replacement for the MV1441 with a much improved internal clock recovery circuit and allowing operation at 8.448MHz with external clock recovery selected. However, there are certain minor differences between the two circuits which are described in a separate Applications Brief (AB33).

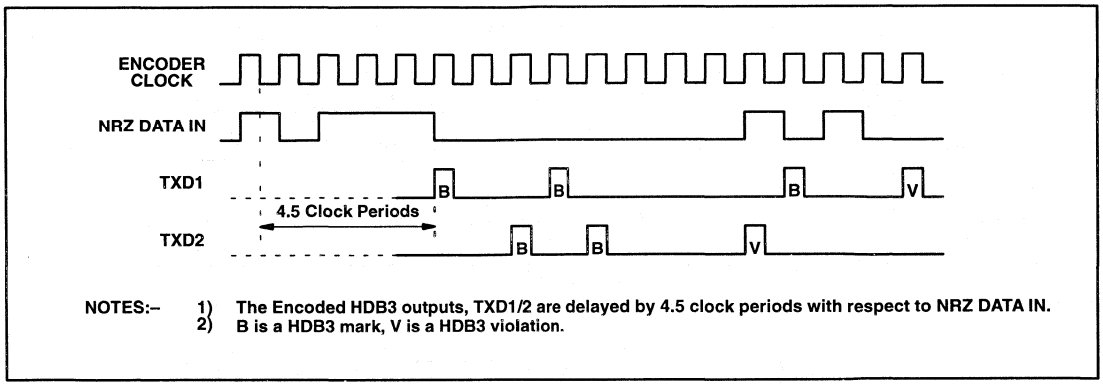


Fig. 3: Encoder waveforms

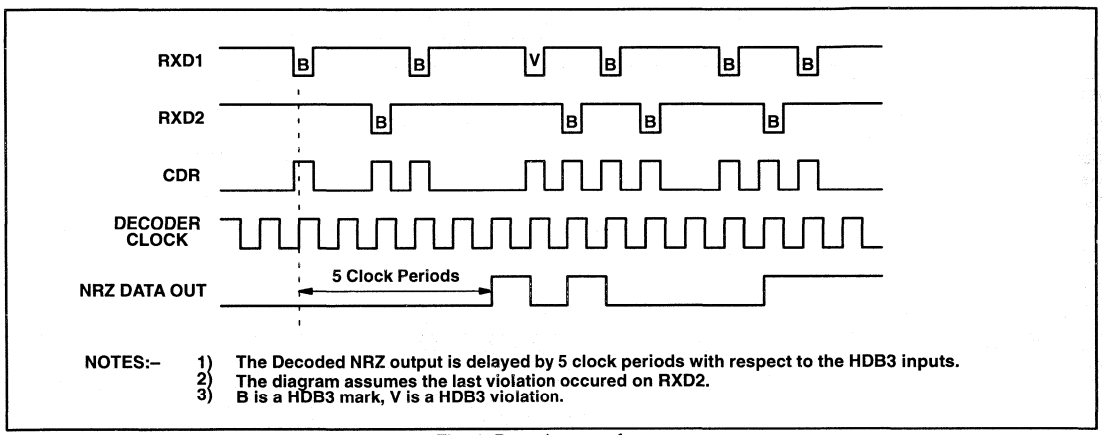


Fig. 4: Decoder waveforms

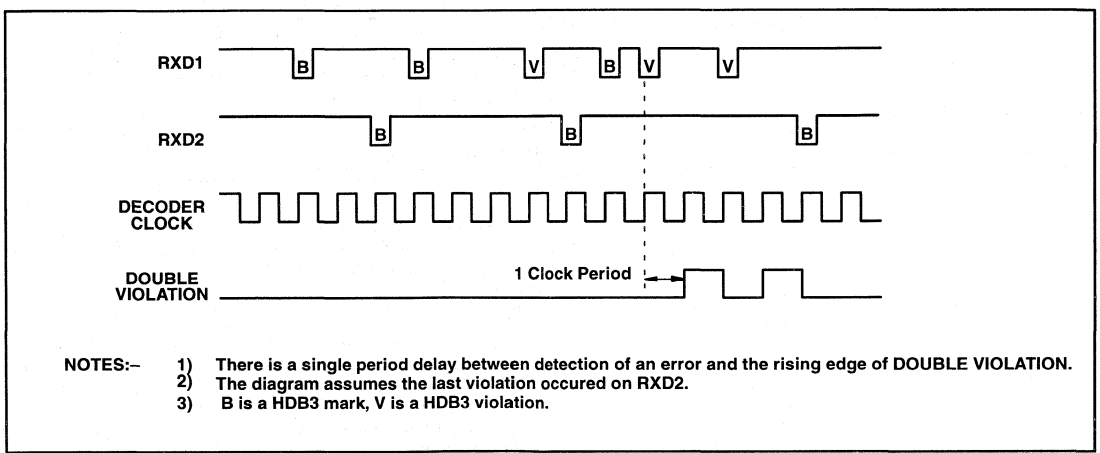


Fig. 5: HDB3 double violation waveforms

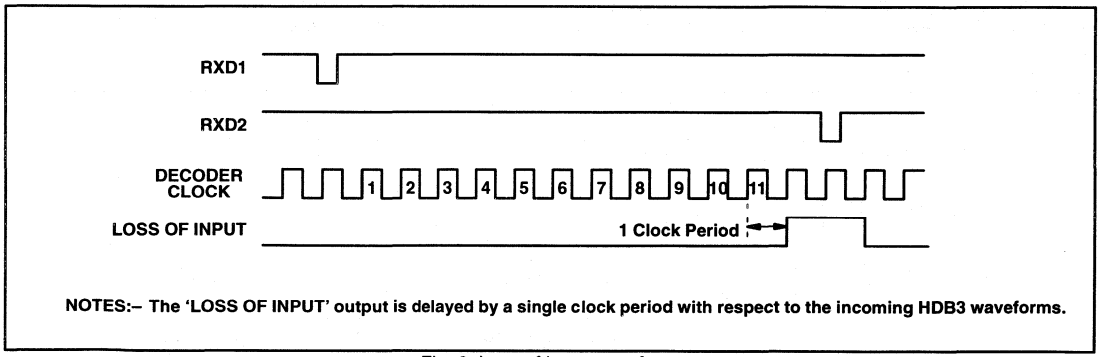


Fig. 6: Loss of input waveforms

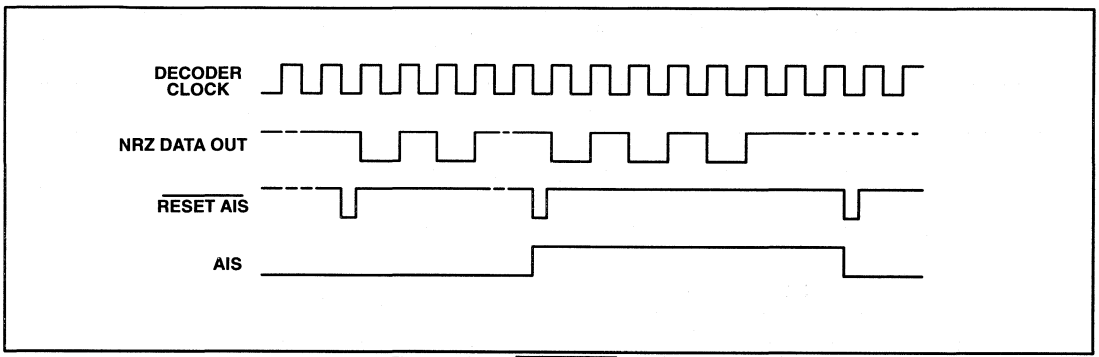


Fig. 7: AIS and RESET AIS waveforms

PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	NRZ DATA IN	Input pin for data to be encoded into pseudo–ternary HDB3 form. This data is clocked into the Encoder block by the falling edge of ENCODER CLOCK.
2	ENCODER CLOCK	Clock input for the encoding of data on pin 1.
3	LOSS OF INPUT	Output from the loss of input circuit. This output goes high one clock period after the detection of eleven consecutive zeros on the decoder inputs. Any logic '1' at the input (RXD1 or RXD2 = 0) resets this count after a single clock period delay.
4	NRZ DATA OUT	NRZ data output obtained from the decoding of the pseudo–ternary inputs to the Decoder block.
5	DECODER CLOCK	Clock input to the Decoder block, for decoding data on RXD1 and RXD2, or TXD1 and TXD2 in loop test mode. In internal clock regeneration mode, this pin is used to output the regenerated clock to external circuitry. In external clock regeneration mode, this pin is used to input the externally regenerated clock signal direct to the Decoder block.
6	$\overline{\text{RESET AIS}}$	Reset input to the decoded zero counter. A logic '0' on this input resets a decoded zero counter. It will also reset the AIS output to '0' provided 3 or more zeros have been decoded in the preceding $\overline{\text{RESET AIS}}$ = 1 period, or set AIS to '1' if less than 3 zeros have been decoded in the preceding $\overline{\text{RESET AIS}}$ = 1 period. This may be used to indicate loss of timeslot zero. A logic '1' on this pin enables the decoded zero counter.
7	AIS	Output from AIS circuit (see description for pin 6).

8	MODE	Input pin for selection of clock regeneration mode. A logic high on this input selects internal crystal controlled clock regeneration whilst a logic low selects external clock regeneration.
9	GND	Digital ground. 0 Volts.
10	CRYSTAL IN	Input to crystal oscillator amplifier when in internal clock regeneration mode, with the crystal connected between pins 10 and 12. Alternatively, this pin may be used as the 16.384/12.352MHz input to the internal clock regeneration circuitry if one oscillator is shared between several decoders. This pin has no function when external clock regeneration is selected and should be tied to GND.
11	DOUBLE VIOLATION	Output from the error detector circuit. This output goes high for one period of Decoder clock, one period after the detection of a HDB3 violation of the same polarity as the previous HDB3 violation.
12	CRYSTAL OUT/CDR	In external clock regeneration mode, this pin is used to output the OR function of the two HDB3 inputs, RXD1 and RXD2 (or TXD1 and TXD2 if loop test mode is selected), to an external clock regeneration circuit. In internal clock regeneration mode, this is the output which forms the crystal oscillator with pin 10.
13	RXD1	HDB3 input 1 to Decoder block. This input asynchronously latches the incoming HDB3 encoded data and is falling edge sensitive.
14	LOOP TEST ENABLE	Input pin for selection of normal or loop back operation. A logic low on this pin selects normal operation, with encoder and decoder being independant and asynchronous. A logic high on this pin internally connects TXD1 to RXD1 and TXD2 to RXD2. Note that in loop back mode, a decoder clock must be supplied (or regenerated from pin 12) along with the encoder clock.
15	RXD2	HDB3 input 2 to Decoder block. See pin 13 description.
16	TXD1	HDB3 Encoded output 1 from Encoder block. This output goes high after the rising edge of clock if a mark is to be transmitted. The length of the pulse is set by the positive clock pulse width.
17	TXD2	HDB3 Encoded output 2. See pin 16 description.
18	VDD	Digital supply voltage. 5Volt ±10%.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Supply Voltage V_{DD} = 5V ± 0.5V Ambient Temperature T_{amb} = −40°C to +85°C

STATIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0		0.8	Volts	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	Volts	
Low Level Output Voltage	V_{OL}			0.4	Volts	I_{SINK} = 2mA
High Level Output Voltage	V_{OHT} V_{OHC}	2.4 V_{DD} −1.0			Volts Volts	I_{SOURCE} = 2mA I_{SOURCE} =1mA
Input Leakage Current	I_{IN}	−10		+200	µAmp	V_{IN} = V_{DD} or GND
Supply Current	I_S			15	mAmps	1.544/2.048MHz Operation with Internal clock regeneration, Note 1.
				5	mAmps	1.544/2.048MHz Operation with External clock regeneration, Note 1.
				15	mAmps	8.448MHz Operation, Note 1.
Input Capacitance	C_{IN}		5		pF	All Inputs
Output Capacitance	C_{OUT}		5		pF	All Outputs

Notes:− 1. All supply currents specified with outputs unloaded. These currents are not tested but are guaranteed by characterisation and a static current test.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{DD} = 5V ± 0.5V Ambient Temperature T_{amb} = –0°C to +70°C

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Clock Period	T_{CP}	100			nS	Refer Fig. 8
Clock Rise/Fall Time	T_{CR}/T_{CF}			20	nS	Refer Fig. 8
Clock High/Low time	T_{CH}/T_{CL}	30			nS	Refer Fig. 8
Encoder Data Setup Time	T_{EDS}	10			nS	Refer Fig. 9
Encoder Data Hold Time	T_{EDH}	10			nS	Refer Fig. 9
TXD1/TXD2 Output Propagation Delay	T_{EPDR}/ T_{EPDF}			45	nS	Note 1, refer Fig. 9
CDR Propagation Delay	T_{CPDR}/ T_{CPDF}			40	nS	Note 1, refer Fig. 10
RXD1/2 Data Setup Time	T_{RS}	15			nS	Refer Fig. 10
RXD1/2 Pulse Width	T_{RW}	20			nS	Refer Fig. 10
Decoder Output Propagation Delay	T_{OPD}			45	nS	Notes 1 and 2, refer Fig. 10
$\overline{\text{RESET AIS}}$ Hold Off Time	T_{RAHO}	10			nS	Refer Fig. 10
$\overline{\text{RESET AIS}}$ Pulse Width	T_{RAW}	15			nS	Refer Fig.10
$\overline{\text{RESET AIS}}$ Setup Time	T_{RAS}	10			nS	Refer Fig. 10
AIS Output Propagation Delay	T_{APD}			45	nS	Note 1, refer Fig. 10

Notes:– 1. All propagation delays are measured with the relevant output loaded with a 50pF capacitor.
2. T_{OPD} applies to outputs NRZ DATA OUT, LOSS OF INPUT and DOUBLE VIOLATION, but does not apply to AIS.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{DD} = 5V ± 0.5V Ambient Temperature T_{amb} = –40°C to +85°C

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Clock Period	T_{CP}	100			nS	Refer Fig. 8
Clock Rise/Fall Time	T_{CR}/T_{CF}			20	nS	Refer Fig. 8
Clock High/Low time	T_{CH}/T_{CL}	35			nS	Refer Fig. 8
Encoder Data Setup Time	T_{EDS}	20			nS	Refer Fig. 9
Encoder Data Hold Time	T_{EDH}	20			nS	Refer Fig. 9
TXD1/TXD2 Output Propagation Delay	T_{EPDR}/ T_{EPDF}			50	nS	Note 1, refer Fig. 9
CDR Propagation Delay	T_{CPDR}/ T_{CPDF}			45	nS	Note 1, refer Fig. 10
RXD1/2 Data Setup Time	T_{RS}	20			nS	Refer Fig. 10
RXD1/2 Pulse Width	T_{RW}	25			nS	Refer Fig. 10

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Decoder Output Propagation Delay	T_{OPD}			50	nS	Notes 1 and 2, refer Fig. 10
$\overline{\text{RESET AIS}}$ Hold Off Time	T_{RAHO}	15			nS	Refer Fig. 10
$\overline{\text{RESET AIS}}$ Pulse Width	T_{RAW}	20			nS	Refer Fig.10
$\overline{\text{RESET AIS}}$ Setup Time	T_{RAS}	15			nS	Refer Fig. 10
AIS Output Propagation Delay	T_{APD}			55	nS	Note 1, refer Fig. 10

Notes:– 1. All propagation delays are measured with the relevant output loaded with a 50pF capacitor.
2. T_{OPD} applies to outputs NRZ DATA OUT, LOSS OF INPUT and DOUBLE VIOLATION, but does not apply to AIS.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

$+V_{DD}$	–0.5 to +7V
Inputs	V_{DD} + 0.5V to GND –0.5V
Outputs	V_{DD} +0.5V to GND –0.5V
Storage temperature	Plastic –55 to +125°C
	Ceramic –65 to +150°C

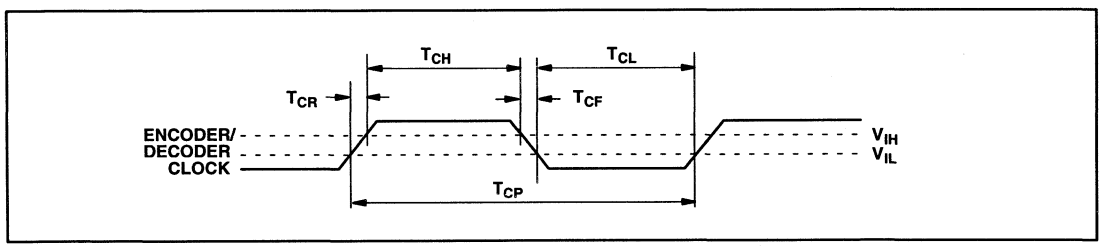


Fig. 8: Clock timing parameters

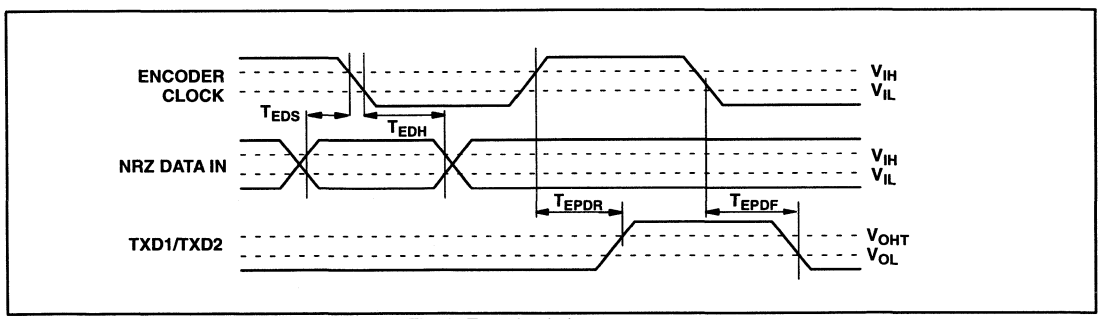


Fig. 9: Encoder timing parameters

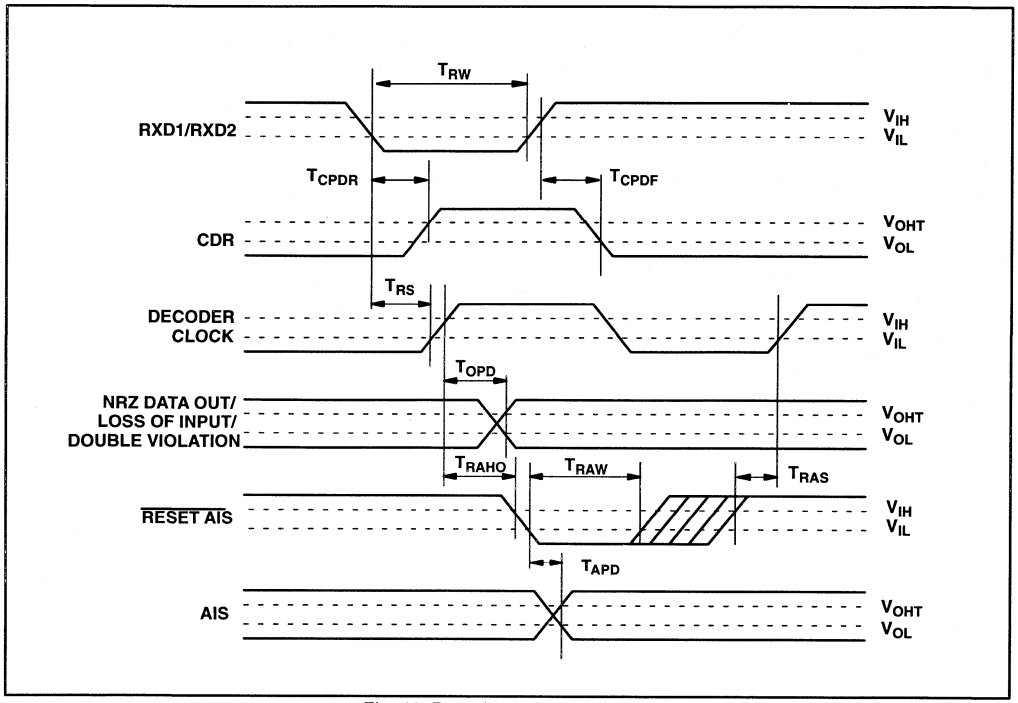


Fig. 10: Decoder timing parameters

MV1449

PCM HDB3 ENCODER/DECODER

The MV1449, along with other devices in the GPS 2Mbit PCM signalling series comprise a group of circuits which will perform the common channel signalling and error detection functions for a 2.048Mbit PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The MV1449 is also capable of operation at the next CCITT hierarchical bit rate of 8.448Mbit. The MV1449 circuit is fabricated in CMOS and operates from a single +5V supply with all inputs and outputs being TTL compatible.

The MV1449 is an encoder/decoder for the HDB3 pseudo-ternary transmission code, described in Annex A of CCITT Recommendation G.703. The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of the HDB3 coding, all ones detection and loss of input (all zero's detection). In addition a loop back function is provided for terminal testing.

FEATURES

- Single +5V supply.
- All Inputs and Outputs TTL compatible.
- HDB3 Encoding and Decoding to CCITT Recommendation G.703.
- Simultaneous Encoding and Decoding.
- Clock Recovery Signal allows Clock Regeneration from Incoming HDB3 Data.
- Loop Back Control.
- HDB3 Error Monitor.
- Alarm Indication Signal Monitor.
- Loss of Input Alarm.
- Low Power Operation.
- 2.048MHz or 8.448MHz Operation.

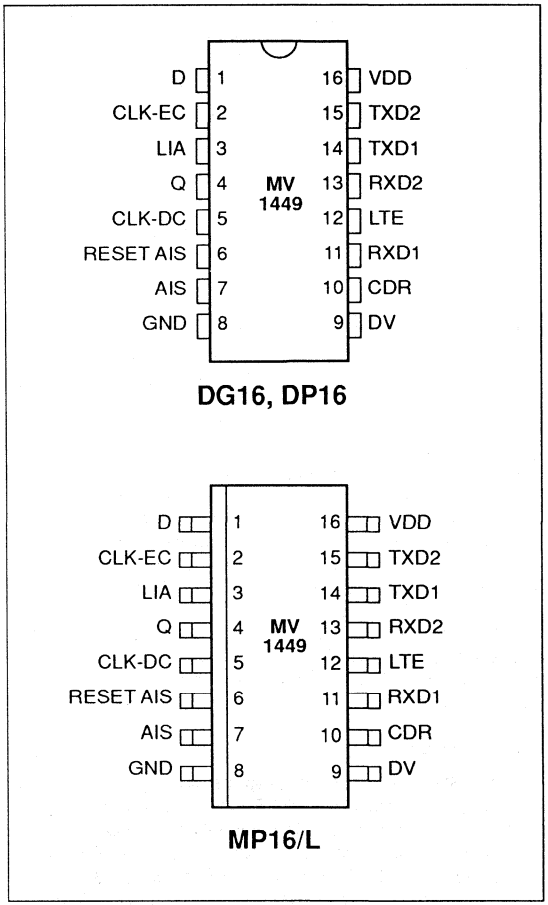


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

ELECTRICAL RATINGS

Supply Voltage	-0.5V to +7V
Input Voltage	-0.5V to VDD +0.5V
Output Voltage	-0.5V to VDD +0.5V

ORDERING INFORMATION

MV1449/IG/DGAS
MV1449/IG/DPAS
MV1449/IG/MPES

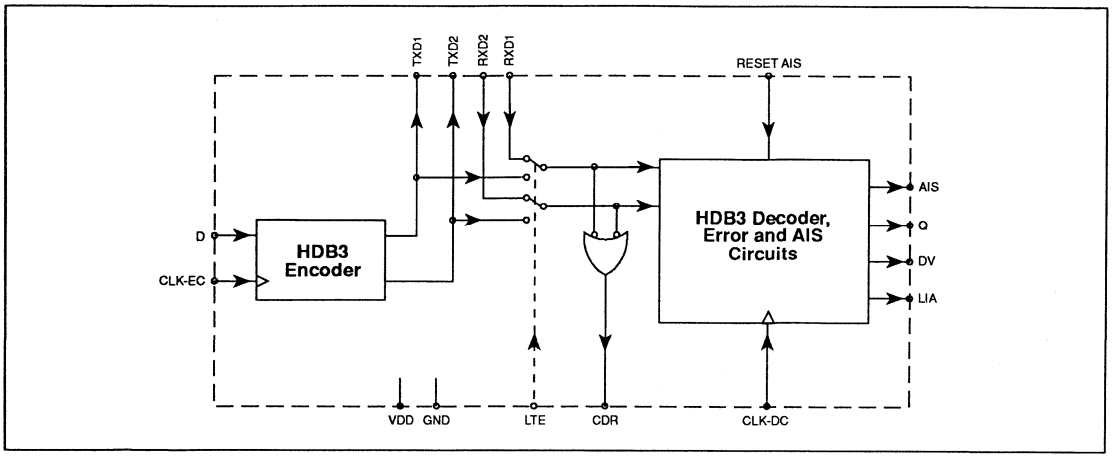


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

High Density Bipolar 3 (HDB3) is a ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to ensure adequate clock recovery at the receiver. In any sequence of four consecutive binary zero's, the last zero is substituted by a mark of the same polarity of the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code and ensures that successive violations alternate in polarity and as such introduce no DC component to the HDB3 signal.

The MV1449 consists of two main blocks, the HDB3 Encoder and the HDB3 Decoder, with the Block Diagram being shown in Fig. 2. The function of each block is now described separately.

HDB3 Encoder

The HDB3 Encoder is responsible for converting the incoming NRZ data into HDB3 Encoded pseudo-ternary form for transmission over a 2.048Mbit/8.448Mbit PCM link. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703, Annex A.

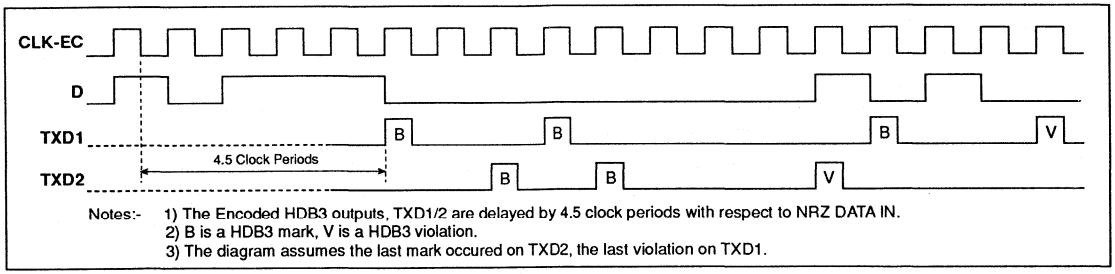
The data to be encoded is input on the D input pin and the encoding process is synchronised to the 2.048MHz/8.448MHz clock signal being input on the CLK-EC pin. The HDB3 Encoder has two outputs, TXD1 and TXD2, which represent the HDB3 encoded PCM data stream in pseudo-ternary form. If a mark or violation is to be transmitted the output pulses high after the rising edge of clock, with the length of the pulse set by the clock high pulse width. The timing diagram of the HDB3 Encoder is shown in Fig. 3.

HDB3 Decoder

The HDB3 Decoder circuit is responsible for converting the 2.048Mbit/8.448Mbit HDB3 encoded pseudo-ternary PCM data stream on its inputs, RXD1 and RXD2, into NRZ binary form to be output on the Q output pin. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703, Annex A. The HDB3 Decoder synchronously decodes the data on its RXD input pins into NRZ form under control of the 2.048MHz/8.448MHz clock being input on its CLK-DC pin. There is a 5 clock period delay between the HDB3 data being clocked in from the RXD inputs and the NRZ data appearing on the Q output. The Decoder clock must be externally regenerated from the incoming HDB3 data stream and in order to aid this clock recovery a logical 'OR' function of the inverted HDB3 inputs is output on the CDR pin.

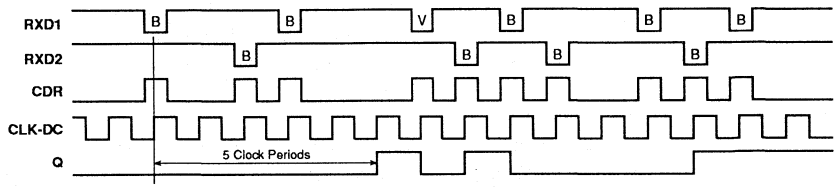
In addition to the basic HDB3 decoding the circuit also provides three alarm outputs. The first of these alarms is DV (Double Violation) and a logic high on this output denotes that two successive violations have been received with the same polarity, thus violating the HDB3 decoding laws. The second alarm, LIA (Loss of Input Alarm), is used to denote that 11 consecutive zero's have been received on the RXD inputs. The third alarm output is AIS (Alarm Indication Signal). This output will go high if less than 3 decoded zero's have been detected in the preceding RESET AIS=1 period (i.e. between RESET AIS=0 pulses) and as such this alarm can be used to detect the CCITT Alarm Indication Signal. All the alarm circuitry as well as the decoding process is synchronised to the clock signal being input on the CLK-DC pin. The clock signal may be asynchronous with the CLK-EC signal. The timing diagrams of the HDB3 Decoder circuit are shown in Fig. 4.

In addition to the normal mode of operation, a loop test mode is available for terminal testing. This mode is selected by taking the LTE (Loop Test Enable) input high. In this mode, the HDB3 encoded pseudo-ternary data outputs of the encoder block are inverted and fed back as the inputs to the decoder block, which in turn decodes this data and outputs it in NRZ form.



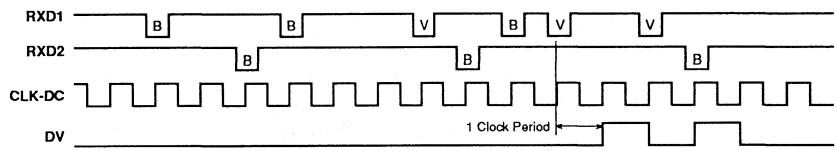
Notes:- 1) The Encoded HDB3 outputs, TXD1/2 are delayed by 4.5 clock periods with respect to NRZ DATA IN.
2) B is a HDB3 mark, V is a HDB3 violation.
3) The diagram assumes the last mark occured on TXD2, the last violation on TXD1.

Fig. 3 HDB3 Encoder waveforms



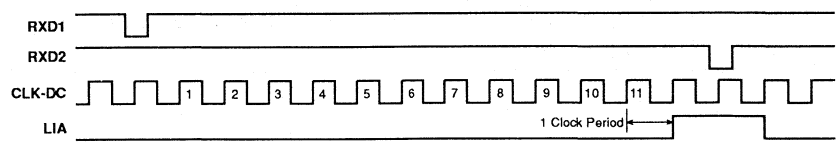
Notes:- 1) The Decoded NRZ output is delayed by 5 clock periods with respect to the HDB3 inputs.
2) The diagram assumes the last violation occured on RXD2.
3) B is HDB3 mark, V is a HDB3 violation.

Decoder waveforms



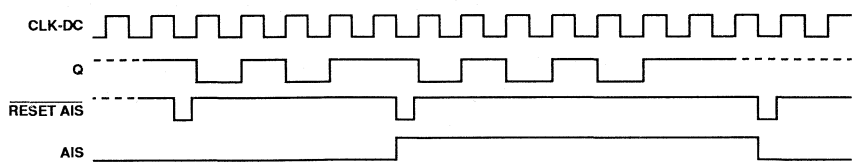
Notes:- 1)There is a single period delay between detection of an error and the rising edge of DOUBLE VIOLATION
2) The diagram assumes the last violation occured on RXD2.
3) B is HDB3 mark, V is a HDB3 violation.

HDB3 Double violation waveforms



Note:- 1)The 'LOSS OF INPUT' is delayed by a single clock period with respect to the incoming HDB3 waveforms.

Loss of input violations



AIS and RESET AIS waveforms

Fig. 4 HDB3 Decoder waveforms

PIN DESCRIPTIONS

Pin Name	Pin no.	Pin description
D	1	NRZ Data Input pin to HDB3 Encoder. The NRZ binary data on this pin is input to the HDB3 Encoder for conversion to HDB3 pseudo-ternary form under control of the CLK-EC signal. The D input is latched into the Encoder block by the falling edge of CLK-EC.
CLK-EC	2	2.048MHz/8.448MHz Clock Input to HDB3 Encoder. The clock signal on this input pin is used for the encoding of data on pin 1.
LIA	3	Loss of Input Alarm Output from HDB3 Decoder. This output goes high one period after the detection of 11 consecutive zeroes on the RXD inputs. Any HDB3 mark on the inputs (RXD1 or RXD2=0) resets this output low after a single clock period delay.
Q	4	NRZ Data Output from HDB3 Decoder. This output represents the HDB3 input data decoded back into NRZ binary form, with a 5 clock period delay from the HDB3 inputs to the NRZ output. This decoding process is carried out under control of the CLK-DC signal.
CLK-DC	5	2.048MHz/8.448MHz clock Input to HDB3 Decoder. The clock signal on this pin is used for the decoding of data on the RXD input pins, or the TXD pins in Loop Test Mode. This pin is used to input the externally regenerated clock signal recovered from the incoming HDB3 waveforms back to the Decoder block.
RESET AIS	6	Reset AIS Input to HDB3 Decoder. A logic '0' on this input resets a decoded zeros counter in the HDB3 Decoder. It will also reset the AIS output to '0' provided 3 or more zeros have been decoded in the preceding RESET AIS=1 period, or set AIS to '1' if less than 3 zeros have been decoded in the preceding RESET AIS=1 period. This may be used to detect the CCITT Alarm Indication Signal. A logic '1' on this pin enables the decoded zeros counter.
AIS	7	Alarm Indication Signal Output from HDB3 Decoder. See description for RESET AIS pin.
GND	8	Digital Ground. 0V
DV	9	Double Violation Alarm Output from HDB3 Decoder. This output goes high for one period of CLK-DC, one period after the detection of a HDB3 violation of the same polarity as the previous HDB3 violation.
CDR	10	Clock Recovery Output from HDB3 Decoder. This pin is used to output the logical 'OR' function of the inverted HDB3 inputs for the use of the external clock recovery circuit.

PIN DESCRIPTIONS (continued)

Pin Name	Pin no.	Pin description
RXD1	11	HDB3 Encoded Input 1 to HDB3 Decoder. This is one of the pair of 2.048Mbit pseudo-ternary HDB3 encoded PCM data stream inputs to the HDB3 Decoder. This input asynchronously latches the incoming HDB3 data and is falling edge sensitive. Since the input is asynchronously latched it is not necessary for the RXD pulse to straddle a rising clock edge.
LTE	12	Loop Test Enable Control Input. A logic low on this pin selects normal operation, with encoding and decoding being independent and asynchronous. A logic high on this pin internally connects TXD1 to RXD1 and TXD2 to RXD2. Note that in loop back mode, a decoder clock must be supplied (or regenerated from CDR) along with the encoder clock.
RXD2	13	HDB3 Encoded Input 2 to HDB3 Decoder. See description for pin RXD1.
TXD1	14	HDB3 Encoded Pseudo-Ternary Output 1 from HDB3 Encoder. The NRZ PCM data stream being input on the D pin is HDB3 encoded and output on this pin and pin TXD2. This output is always low during the low half cycle of clock and is only high during the high half cycle of clock if a mark is to be output. There is a 4.5 clock period delay from the falling edge of CLK-EC to TXD1.
TXD2	15	HDB3 Encoded Pseudo-Ternary Output 2 from HDB3 Encoder. See Pin TXD1 description.
VDD	16	Digital Supply Voltage. 5V

NOTES

1. All inputs have 100K on-chip pull down resistors.

ELECTRICAL CHARACTERISTICS

Test Conditions:
Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = -40°C to +85°C

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0.0		0.8	V	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	V	
Low Level Output Voltage	V_{OL}			0.4	V	Isink=2mA
High Level Output Voltage	V_{OHT}	2.4			V	Isource=2mA
	V_{OHC}	V_{DD}-1.0			V	Isource=lmA
Input Leakage Current	I_{IL}	-10		200	uA	$V_{IN}=V_{DD}$ or V_{SS}
Supply Current	I_S			5	mA	2.048MHz Operation, Note 1.
				15	mA	8.448MHz Operation, Note 1.
Input Capacitance	C_{IN}		5		pF	All Inputs
Output Capacitance	C_{OUT}		5		pF	All Outputs

NOTES

1. All supply currents measured with outputs unloaded.

DYNAMIC CHARACTERISTICS

Note: Two sets of dynamic characterisitics are supplied, for use over the Commercial and Industrial Temperature ranges. The parameter set for the Commercial temperature range is aimed at customers wishing to switch from either the MJ1440 or MV1448 devices to the MV1449 since both the older devices were specified over the Commercial temperature range.

Test Conditions:
Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = 0°C to +70°C

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock Period	t_{CP}	100			ns	See Fig. 5
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock High/Low Time	t_{CH}/t_{CL}	30			ns	See Fig. 5
ENCODER						
Encoder Data Setup Time	t_{EDS}	15			ns	See Fig. 6
Encoder Data Hold Time	t_{EDH}	15			ns	See Fig. 6
TXD1/TXD2 Output Propagation Delay	t_{EPDR}/ t_{EPDF}			45	ns	See Fig. 6, Note 1.
DECODER						
RXD1/2 Data Setup Time	t_{RS}	15			ns	See Fig. 7
RXD1/2 Pulse Width	t_{RW}	20			ns	See Fig. 7
CDR Propagation Delay	t_{CPDR}/ t_{CPDF}			40	ns	See Fig. 7, Note 1.
Decoder Output Propagation Delay.	t_{OPD}			45	ns	See Fig. 7, Notes 1 and 2.
RESET AIS Hold-Off Time	t_{RAHO}	15			ns	See Fig. 7
RESET AIS Pulse Width	t_{RAW}	15			ns	See Fig. 7
Reset AIS Setup Time	t_{RAS}	10			ns	See Fig. 7
AIS Propagation Delay	t_{APD}			45	ns	See Fig. 7, Note 1.

Test Conditions:
Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock Period	t_{CP}	100			ns	See Fig. 5
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock High/Low Time	t_{CH}/t_{CL}	35			ns	See Fig. 5
ENCODER						
Encoder Data Setup Time	t_{EDS}	20			ns	See Fig. 6
Encoder Data Hold Time	t_{EDH}	20			ns	See Fig. 6
TXDI/TXD2 Output Propagation Delay	t_{EPDR}/ t_{EPDF}			50	ns	See Fig. 6, Note 1.
DECODER						
RXD1/2 Data Setup Time	t_{RS}	20			ns	See Fig. 7
RXD1/2 Pulse Width	t_{RW}	25			ns	See Fig. 7
CDR Propagation Delay	t_{CPDR}/ t_{CPDF}			45	ns	See Fig. 7, Note 1.
Decoder Output Propagation Delay.	t_{OPD}			50	ns	See Fig. 7, Notes 1 and 2.
RESET AIS Hold-Off Time	t_{RAHO}	15			ns	See Fig. 7
RESET AIS Pulse Width	t_{RAW}	20			ns	See Fig. 7
Reset AIS Setup Time	t_{RAS}	15			ns	See Fig. 7
AIS Propagation Delay	t_{APD}			55	ns	See Fig. 7, Note 1.

NOTES

1. All output propagation delays are measured with a 50pF load.
2. The t_{OPD} parameter applies to outputs Q, LIA and DV, but does not apply to AIS.

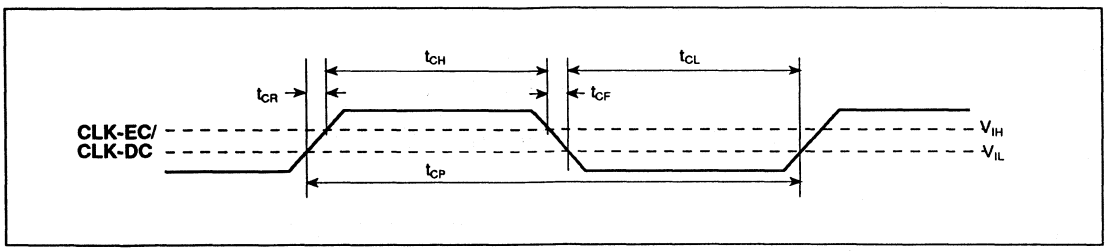


Fig. 5 Clock timing parameters

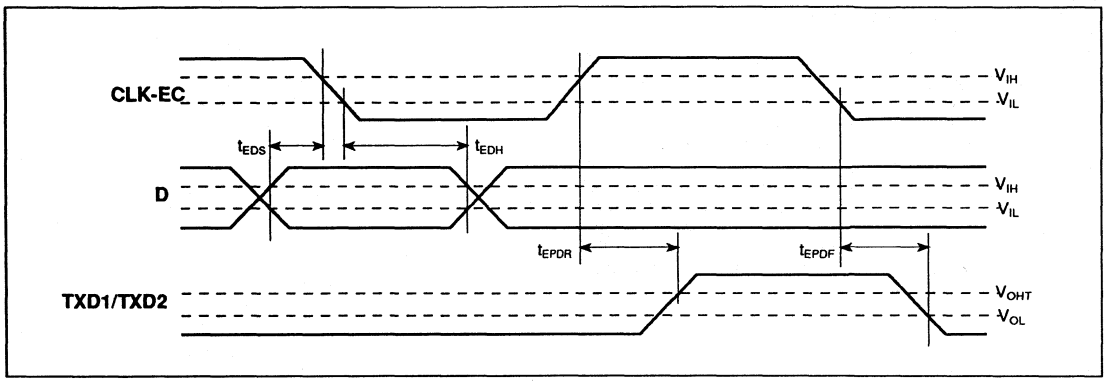


Fig. 6 Encoder timing parameters

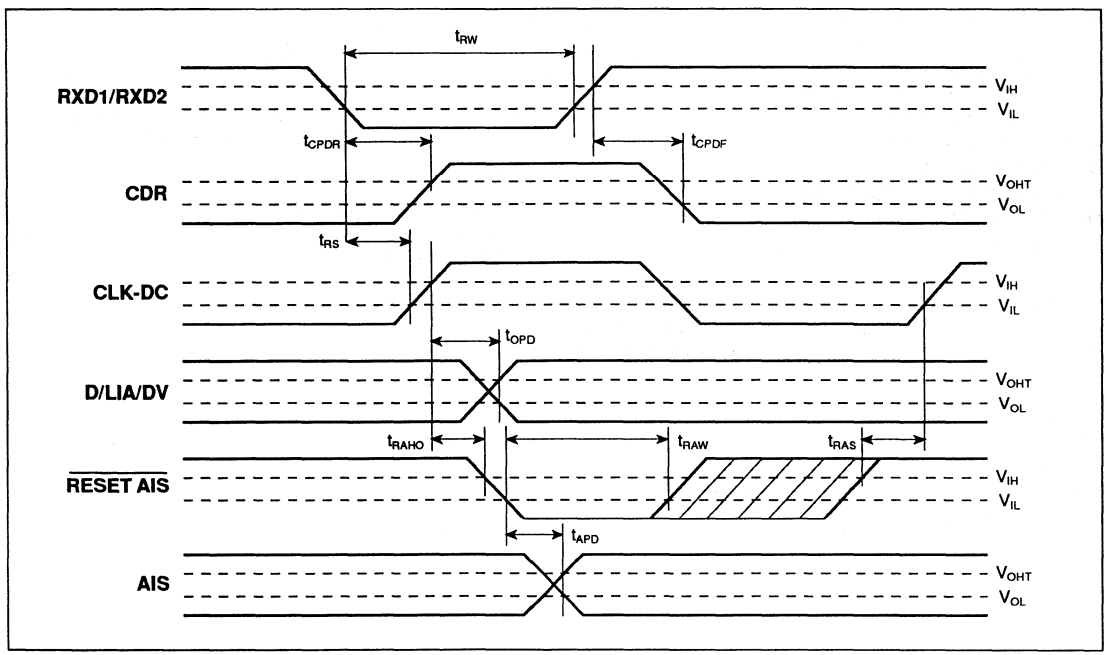


Fig. 7 Decoder timing parameters

MV1471

HDB3/AMI ENCODER/DECODER

The MV1471, along with other devices in the GPS 2Mbit PCM signalling series comprise a group of circuits which will perform the common channel signalling and error detection functions for a 2.048Mbit PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The MV1471 is also capable of operating at clock rates up to 10MHz. The MV1471 circuit is fabricated in CMOS and operates from a single +5V supply with all inputs and outputs being TTL compatible.

The MV1471 is an encoder/decoder for pseudo–ternary transmission codes. The code can be selected as either true Alternate Mark Inversion (AMI) code or AMI modified according to the HDB3 coding laws specified in Annex A of CCITT Recommendation G. 703. The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of the HDB3 coding and all ones detection. In addition a loop back function is provided for terminal testing.

FEATURES

- Single +5V supply
- All Inputs and Outputs TTL compatible
- Selectable HDB3 or AMI coding
- HDB3 Encoding and Decoding to CCITT Recommendation G. 703
- Simultaneous Encoding and Decoding
- Clock Recovery Signal allows Clock Regeneration from Incoming PCM data
- Loop Back Control
- HDB3 error monitor
- Alarm Indication Signal Monitor
- Low Power Operation
- 2.048MHz or 8.448MHz Operation

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Supply Voltage	–0.5V to +7V
Input Voltage	–0.5V to V_{DD} +0.5V
Output Voltage	–0.5V to V_{DD} +0.5V
Storage temperature (DP)	–55 to +150°C
Storage temperature (DG)	–65 to +150°C

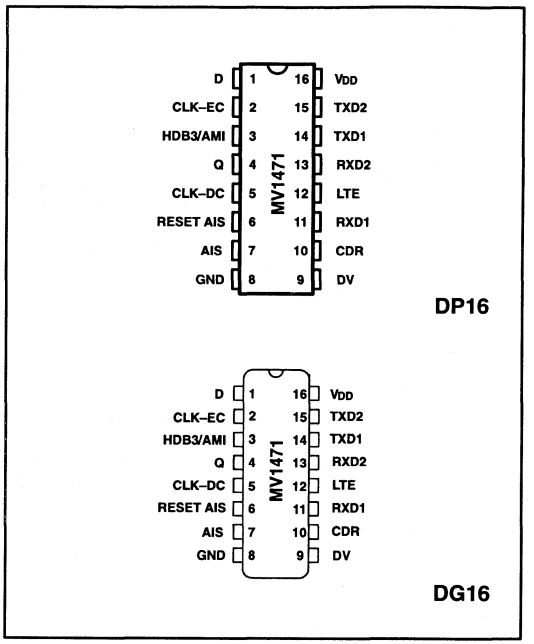


Fig. 1 Pin connections top view

ORDERING INFORMATION

MV1471/CG/DPAS
MV1471/CG/DGAS

Functional Description

High density bipolar 3 (HDB3) is a ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to ensure adequate clock recovery at the receiver. In any sequence of four consecutive binary zero's, the last zero is substituted by a mark of the same polarity as the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code and ensures that successive violations alternate in polarity and as such introduce no DC components to the HDB3 signal.

The MV1471 consists of two main blocks, the HDB3/AMI Encoder and the HDB3/AMI Decoder, with the block diagram being shown in Fig. 2. The function of each block is now described separately.

HDB3/AMI Encoder

The HDB3/AMI Encoder is responsible for converting the incoming NRZ data into pseudo–ternary form for transmission over a 2.048Mbit/8.448Mbit PCM link according to either the true AMI rules or AMI modified according to the HDB3 encoding rules. In HDB3 mode, this conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G. 703, Annex A. Selection between the two encoding schemes is controlled by the HDB3/AMI control input. A logic high on this pin will configure the device in HDB3 mode.

The data to be encoded is input on the D input pin and the encoding process is synchronised to the 2.048/8.448MHz clock signal being input on the CLK–EC pin. The HDB3/AMI Encoder has two outputs, TXD1 and TXD2, which represent the encoded PCM data stream in pseudo–ternary form. If a mark or HDB3 violation is to be transmitted the output pulses high after the rising edge of the clock, with the length of the pulse set by the clock high pulse width. The timing diagram of the HDB3/AMI Encoder is shown in Fig. 3.

HDB3/AMI Decoder

The HDB3/AMI Decoder circuit is responsible for converting the 2.048Mbit/8.448Mbit HDB3/AMI encoded pseudo–ternary PCM data stream on its inputs, RXD1 and RXD2, into NRZ binary form to be output on the Q output pin. In HDB3 mode this conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G. 703, Annex A. The HDB3/AMI decoder synchronously decodes the data on its RXD input pins into NRZ form under control of the 2.048MHz/8.448MHz clock being input on its CLK–DC pin. There is a 5 clock period delay between the encoded data being clocked in from the RXD inputs and the NRZ data appearing on the Q output. The Decoder clock must be externally regenerated from the incoming PCM data streams and in order to aid this clock recovery a logical 'OR' function of the decoder inputs is output on the CDR pin.

In addition to the HDB3/AMI decoding the circuit also provides two alarm outputs. The first of these alarms is DV (Double Violation) and a logic high on this output denotes that two successive violations have been received with the same polarity, thus violating the HDB3 decoding laws. The second alarm output is AIS (Alarm Indication Signal). This output will go high if less than 3 decoded zero's have been detected in the preceding two RESET AIS=1 periods (i.e. between two RESET AIS=0 pulses) and as such this alarm can be used to detect the CCITT Alarm Indication Signal. All the alarm circuit as well as the decoding process is synchronised to the clock signal being input on the CLK–DC pin. The clock signal may by asynchronous with the CLK–EC signal. The timing diagrams of the HDB3/AMI Decoder circuit are shown in Fig.4. In addition to the normal mode of operation, a loop test mode is available for terminal testing. This mode is selected by taking the LTE (Loop Test Enable) input high. In this mode, the HDB3/AMI encoded pseudo–ternary data outputs of the encoder block are fed back as the inputs to the decoder block, which in turn decodes this data and outputs it in NRZ form.

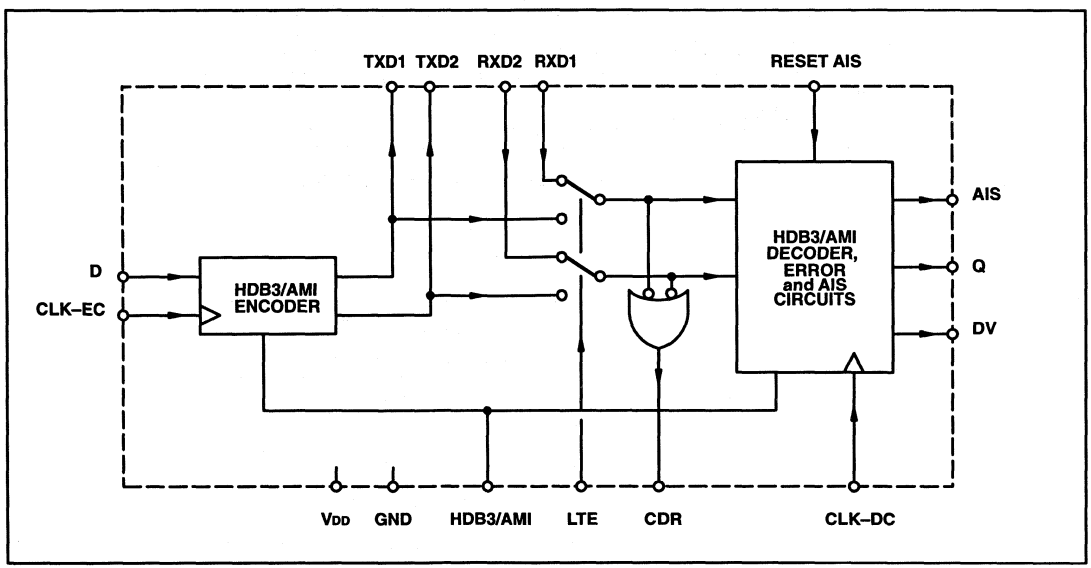
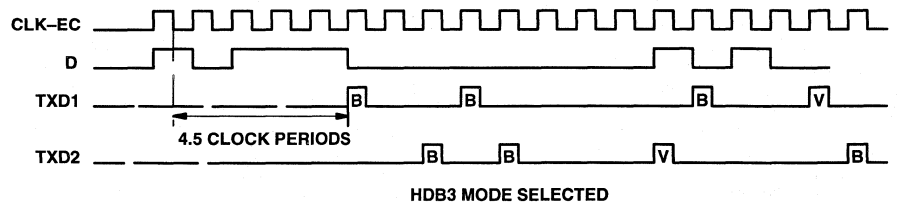
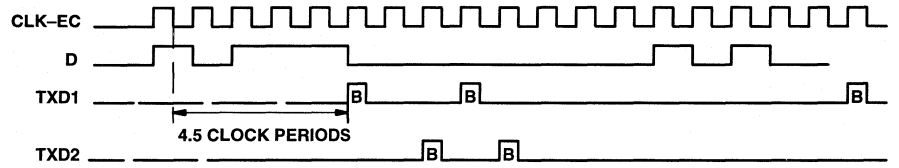


Fig. 2 Block diagram



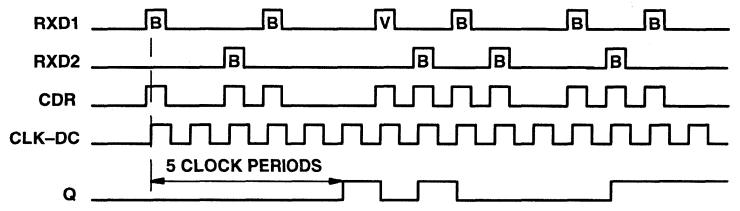
HDB3 MODE SELECTED



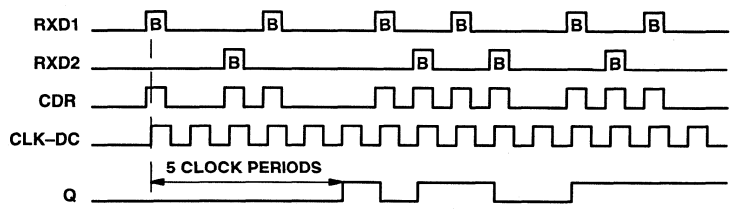
AMI MODE SELECTED

NOTES
1) The Encoder outputs, TXD1/2 are delayed by 4.5 clock periods with respect to D.
2) B is a HDB3 mark, V is a HDB3 violation.
3) Both diagrams assume the last mark occured on TXD2 and the last violation on TXD1.

Fig. 3 HDB3/AMI Encoder waveforms



DECODER WAVEFORMS – HDB3 MODE SELECTED



DECODER WAVEFORMS – AMI MODE SELECTED

NOTES
1) The decoder NRZ output is delayed by 5 clock periods with respect to the PCM inputs.
2) B is a HDB3 mark, V is a HDB3 violation.
3) The diagrams assume that the last mark and last violation both occured on RXD2.

Fig. 4 HDB3/AMI Decoder waveforms

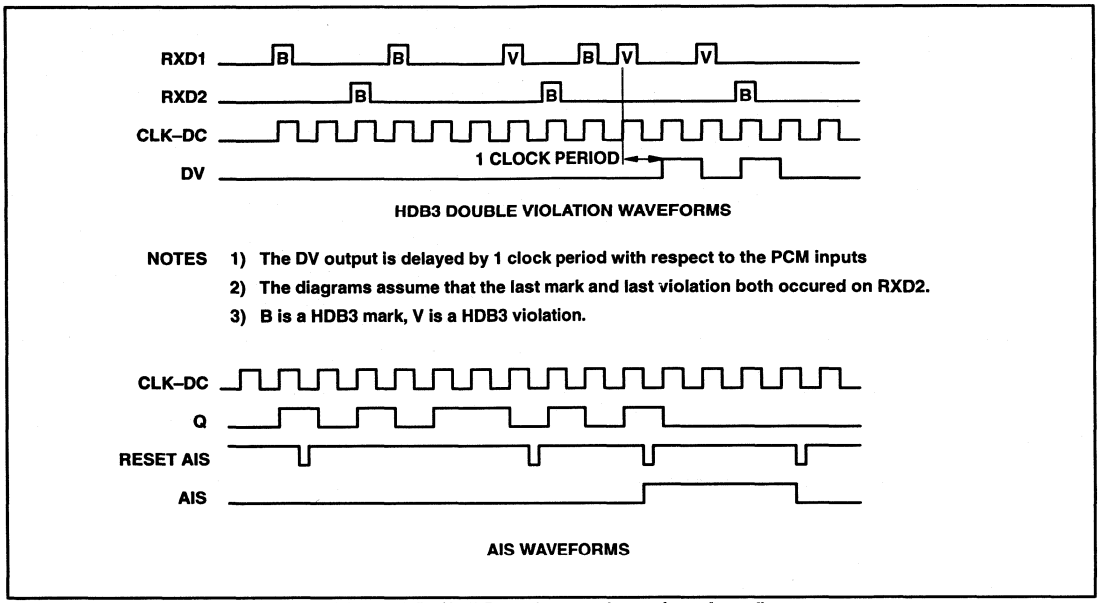


Fig. 4 HDB3/AMI Decoder waveforms ***(continued)***

PIN DESCRIPTION

Pin Name	Pin No	Description
D	1	NRZ Data Input pin to HDB3/AMI Encoder. The NRZ binary data on this pin is input to the HDB3/AMI Encoder for conversion to HDB3/AMI pseudo–ternary form under control of the CLK–EC signal. The D input is latched into the encoder block by the falling edge of CLK–EC.
CLK–EC	2	2.048MHz Clock Input to HDB3 Encoder. The clock signal on this input is used for the encoding of data on pin 1.
HDB3/AMI	3	HDB3/AMI Mode Select Input. A logic high on this pin selects HDB3 operation. A logic low selects AMI mode.
Q	4	NRZ Data Output from HDB3/AMI Decoder. This output represents the HDB3/AMI input data decoded back into NRZ binary form, with a 5 clock period delay from the PCM inputs to the NRZ output. This decoding process is carried out under control of the CLK–DC signal.
CLK–DC	5	2.048MHz Clock Input to HDB3/AMI Decoder. The clock signal on this pin is used for decoding of data on the RXD input pins, or the TXD pins in Loop Test Mode. This pin is used to input the externally regenerated clock signal recovered from the incoming HDB3/AMI waveforms back to the decoder block.
RESET AIS	6	Reset AIS Input to HDB3/AMI Decoder. A logic '0' on this input resets a decoded zeros counter in the HDB3/AMI decoder. It will also reset the AIS output to '0' provided 3 or more zeros have been decoded in the preceding RESET AIS=1 period, or set AIS to '1' if less than 3 zeros have been decoded in the preceding two RESET AIS=1 periods. This may be used to detect the CCITT Alarm Indication Signal. A logic '1' on this pin enables the decoded zeros counter.
AIS	7	Alarm Indicator Signal Output from HDB3/AMI Decoder. See description for RESET AIS pin.
GND	8	Digital Ground. 0V.
DV	9	Double Violation Alarm Output from HDB3/AMI Decoder. This output goes high for one period of CLK–DC, one period after the detection of a HDB3 violation of the same polarity as the previous HDB3 violation.
CDR	10	Clock Recovery Output from HDB3/AMI Decoder. This pin is used to output the logical 'OR' function of the PCM inputs for the use of the external clock recovery circuit.

RXD1	11	HDB3/AMI Encoded Input 1 to HDB3/AMI Decoder. This is one of the pair of 2.048Mbit/8.448Mbit pseudo–ternary PCM data stream inputs to the HDB3/AMI Decoder. This input asynchronously latches the incoming HDB3/AMI data and is rising edge sensitive. Since the input is asynchronously latched it is not necessary for the RXD pulse to straddle a rising clock edge.
LTE	12	Loop Test Enable Control Input. A logic low on this pin selects normal operation, with encoding and decoding being independent and asynchronous. A logic high on this pin internally connects TXD1 to RXD1 and TXD2 to RXD2. Note that in loop back mode, a decoder clock must be supplied.
RXD2	13	HDB3/AMI Encoded Input 2 to HDB3/AMI Decoder. See description for pin RXD1.
TXD1	14	HDB3/AMI Encoded Pseudo–Ternary Output 1 from HDB3/AMI Encoder. The NRZ PCM data stream being input on the D pin is HDB3/AMI encoded and output on this pin and pin TXD2. This output is always low during the low half cycle of clock and is only high during the high half cycle of clock if a mark is to be output. There is a 4.5 clock period delay from the falling edge of CLK–EC to TXD1.
TXD2	15	HDB3/AMI Encoded Pseudo–Ternary Output 1 from HDB3/AMI Encoder. See Pin TXD1 description.
VDD	16	Digital Supply Voltage. 5V.

NOTES

1. All inputs except HDB3/AMI have 100K on–chip pull down resistors. HDB3/AMI has a 100K on–chip pull–up resistor.

ELECTRICAL CHARACTERISTICS

Test Conditions

Supply Voltage V_{DD} = 5V ±0.5V Ambient Temperature T_{amb} = 0°C to + 70°C

STATIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low level input voltage	V_{IL}	0.0		0.8	V	
High level input voltage	V_{IH}	2.0		V_{DD}	V	
Low level output voltage	V_{OL}			0.4	V	I_{sink} = 2mA
High level output voltage	V_{OHT}	2.4			V	I_{source} = 2mA
	V_{OHC}	V_{DD}–1.0			V	I_{source} = 1mA
Input leakage current	I_{IL}	–10		200	µA	V_{in} = V_{DD} or GND
Supply current	I_S			5	mA	2.048MHz operation Note 1.
				15	mA	8.448MHz operation Note 1.
Input capacitance	C_{IN}		5		pF	All inputs
Output capacitance	C_{OUT}		5		pF	All outputs

NOTES

1. All supply currents measured with outputs unloaded. These currents are not tested but are guaranteed by characterisation and a static current test.

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock period	t_{CP}	100			ns	See Fig. 5
Clock rise/fall time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock high/low time	t_{CH}/t_{CL}	30			ns	See Fig. 5

(cont.)DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
ENCODER						
Encoder data setup time	t_{EDS}	15			ns	See Fig. 6
Encoder data hold time	t_{EDH}	15			ns	See Fig. 6
TXD1/TXD2 output propagation delay	t_{EPDR} t_{EPDF}			45	ns	See Fig. 6, Note 1.
DECODER						
RXD1/2 data setup time	t_{RS}	20			ns	See Fig. 7
RXD1/2 pulse width	t_{RW}	20			ns	See Fig. 7
CDR propagation delay	t_{CPDR}/ t_{CPDF}			45	ns	See Fig. 7, Note 1.
Decoder output propagation delay	t_{OPD}			45	ns	See Fig. 7, Note 1.and 2.
RESET AIS hold–off time	t_{RAHO}	15			ns	See Fig. 7
RESET AIS pulse width	t_{RAW}	15			ns	See Fig. 7
Reset AIS setup time	t_{RAS}	10			ns	See Fig. 7
AIS propagation delay	t_{APD}			55	ns	See Fig. 7, Note 1.

NOTES

1. All output propagation delays are measured with a 50pF load.
2. The t_{OPD} parameter applies to outputs Q, and DV, but does not apply to AIS.

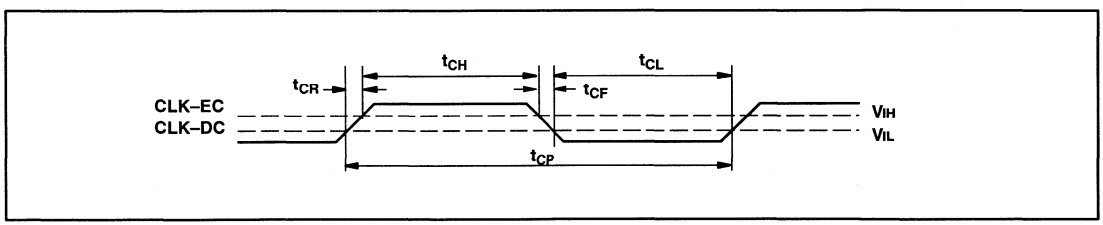


Fig. 5 Clock timing parameters

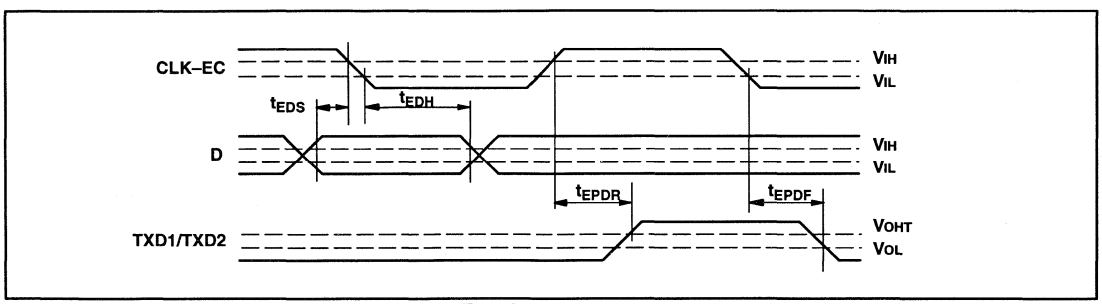


Fig. 6 Encoder timing parameters

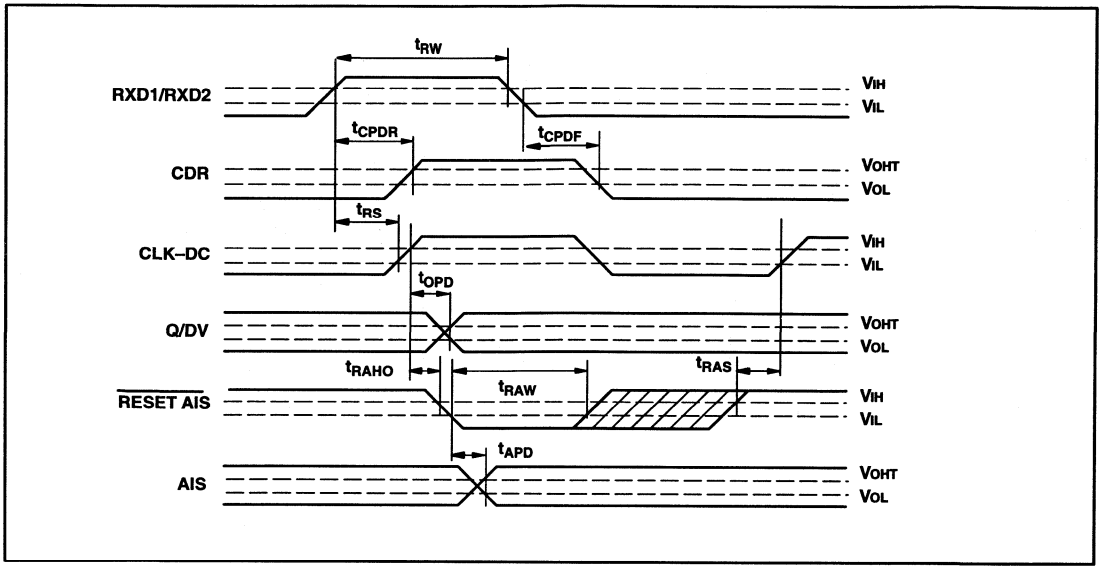


Fig. 7 Decoder timing parameters

Section 6

IF SAWs for GSM Digital Cellular Communications

GEC PLESSEY
SEMICONDUCTORS

DS3532-1.4

DW9241

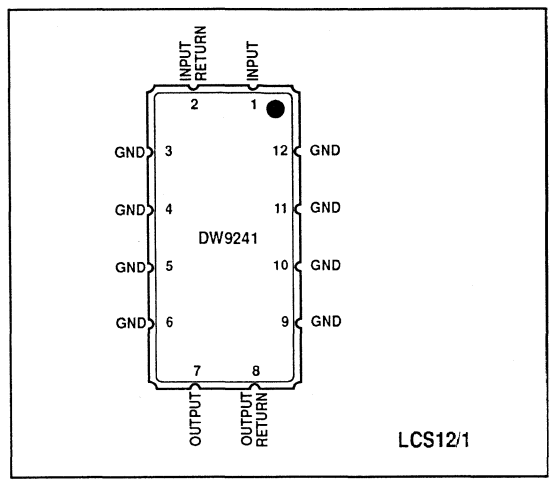
78.8125MHZ LOW LOSS SAW I.F. FILTER FOR GSM PERSONAL COMMUNICATIONS

(Supersedes version in February 1994 Microwave Products Handbook, HB3198-2)

The DW9241 has been specifically developed for the Personal Communications market, where the 1st I.F. stage filter is typically in the 60 to 80MHz range.

The filter is realised on ST-Quartz, using Uni-directional Transducer technology, which provides excellent insertion loss, and temperature stability.

The unique design odviates the need for distinct Roof & Channel filters, usually required to achieve a low shape factor, with maximum bandwidth. The filters can be used in single or cascade format, and are available in a low profile, leadless, surface mount package, which is compatible with most modern manufacturing techniques.



FEATURES

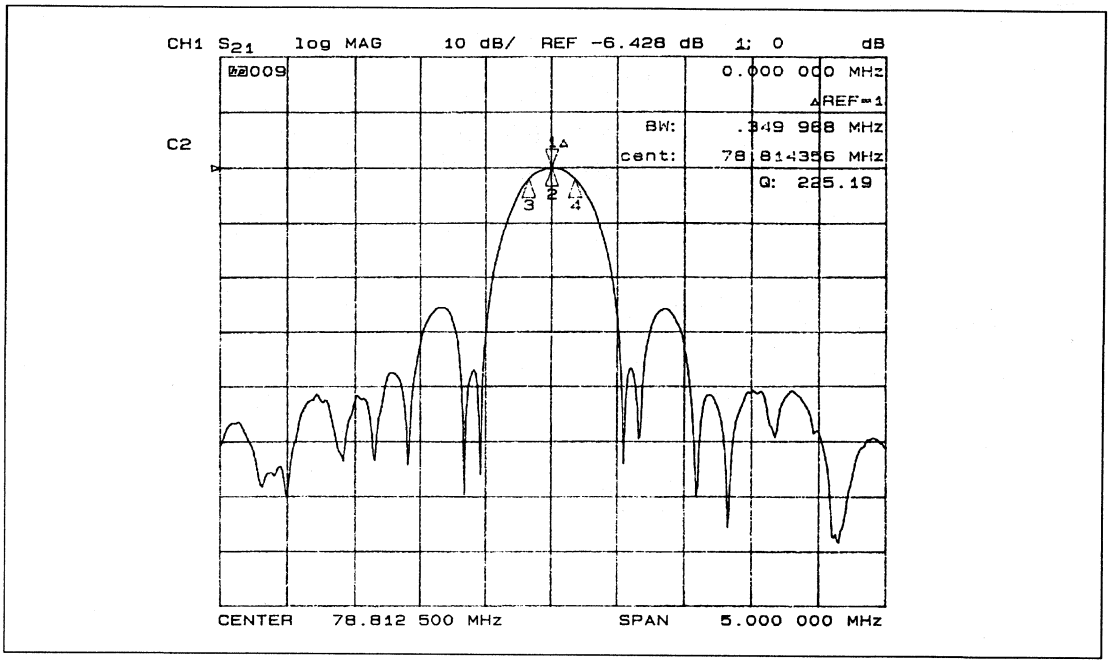
- 78.8125MHz Centre Frequency (f_o)
- Low Insertion Loss (<6dB Single <12dB Cascade)
- Excellent Sidelobe Suppression
- Low Profile, Leadless Surface Mount Package
- Hermetically Sealed Package

ABSOLUTE MAXIMUM RATINGS

DC Voltage	VDC	0V
Input Power Max.	PIN	10dBm

ORDERING INFORMATION

DW9241



ELECTRICAL CHARACTERISTICS

Parameter	Value	Units
Centre Frequency (f_O)	78.8125	MHz
Passband	±85 (Min)	kHz
Insertion Loss	< 6	dB
Passband Ripple	0.5 (Max)	dB
Group Delay	< 0.5	µs
Stopband Rejection: f_O ±200kHz	> 2	dB
f_O ±400kHz	> 12	dB
f_O ±600kHz	> 20	dB
f_O ±800kHz	> 20	dB
-1.625MHz (BW = 200kHz)	> 40	dB
Ultimate Rejection (±1MHz ~ ±25MHz)	> 30	dB
Operating Temperature	-20 to +85	dB

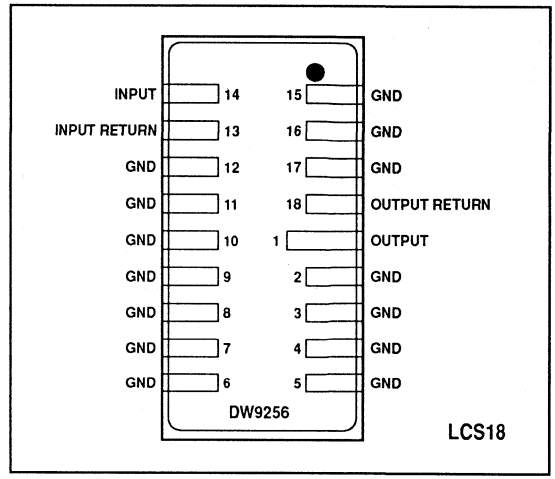
DW9256

133MHz IF SAW FILTER FOR GSM MOBILE PHONES

The DW9256 has been designed specifically for the Personal Communications market, as an IF filter with a centre frequency of 133MHz. The filter utilises GPS's low loss Transversal filter technology based on a Quartz substrate for excellent temperature stability.

A minimum 3dB passband of ±75kHz is combined with a high shape factor to give good adjacent channel rejection.

The device is available in a surface mount, ceramic leadless chip carrier, suited to high volume automated assembly systems.



FEATURES

- 133MHz Centre Frequency (fo)
- Low Insertion Loss (7dB maximum)
- 3dB Passband ±75kHz (minimum)
- Quartz Temperature Stability
- Low Profile Ceramic LCC Package

ABSOLUTE MAXIMUM RATINGS

DC Voltage	VDC	0V
Input Power Max.	PIN	10dBm

NOMINAL IMPEDANCE

Input: 520Ω // 20pF
Output: 200Ω // 30pF

50Ω GPS TEST BOARD COMPONENTS

Input: Series Ind. 180nH, Shunt Ind. 100nH, Shunt Cap. 2.2pF
Output: Shunt Ind. 68nH, Series Ind. 82nH

Components: Coilcraft 1008CS Inductors : Murata 0805 Capacitors

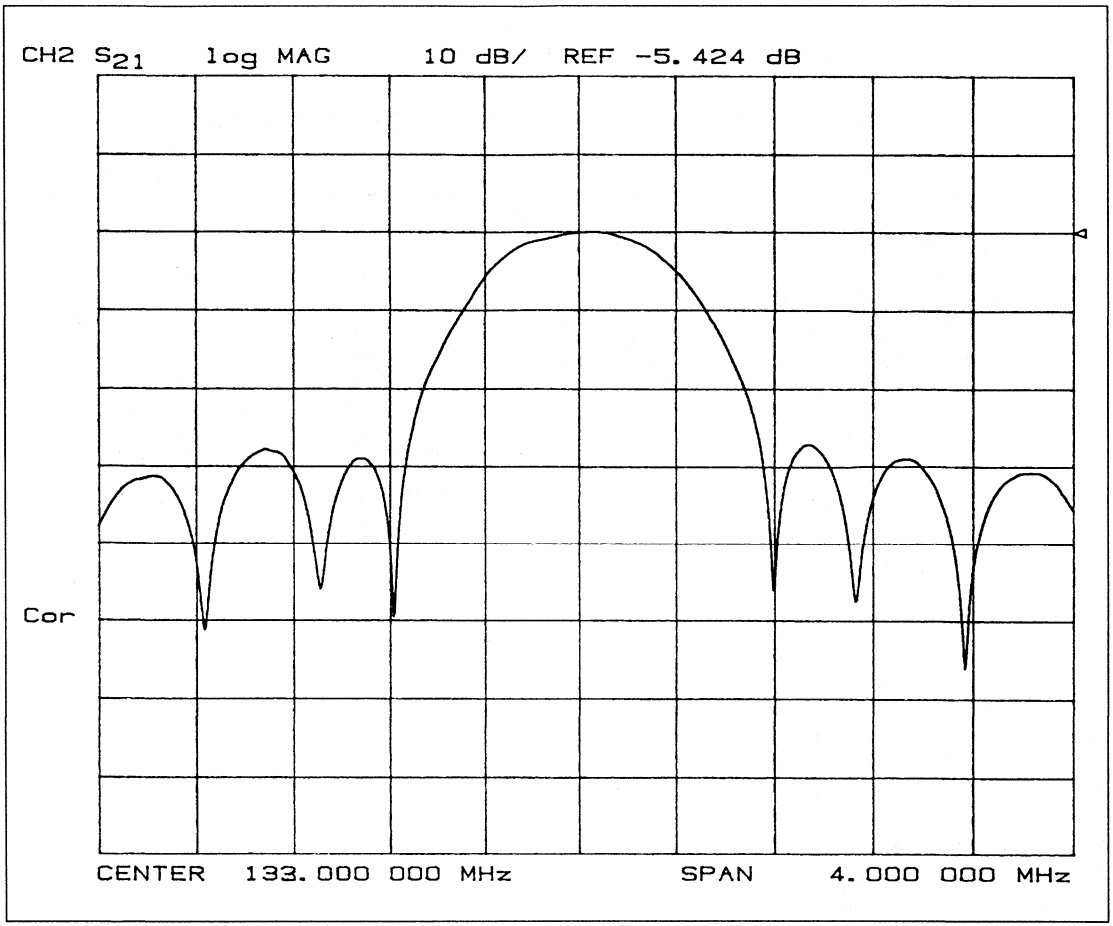
ORDERING INFORMATION

DW9256

ELECTRICAL CHARACTERISTICS @ 25°C

Parameter	Min	Typ	Max	Units
Centre Frequency	-	133	-	MHz
1dB Bandwidth	±75	±170	-	kHz
3dB Bandwidth	±75	±300		kHz
Insertion Loss	4	5	7	dB
Amplitude Ripple	-	0.5	2	dB
Group Delay Ripple	-	150	1000	ns
Stopband Rejection:				
fo ± 400 - 600 kHz	3	5	-	dB
fo ± 600 - 800 kHz	10	15	-	dB
fo ± 800 - 1500 kHz	20	30	-	dB
fo - 1500 kHz - 50 MHz	30	35	-	dB
fo + 1500 kHz + 200 MHz	30	35	-	dB
Operating Temperature Range	-20	-	+80	°C

PLOT

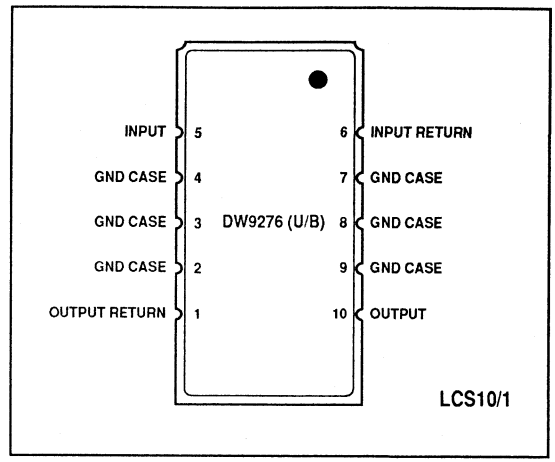

CH2 S21 log MAG 10 dB/ REF -5.424 dB
Cor
CENTER 133.000 000 MHz
SPAN 4.000 000 MHz

DW9276

71MHz IF SAW FILTER FOR GSM MOBILE PHONES

The DW9276 is a 71MHz IF SAW filter which has been specifically designed for cellular radio architectures using the highly integrated 'Sceptre'™ hardware platform for GSM from AT&T Microelectronics.

Based on quartz for excellent temperature stability, the DW9276 provides very high channel selectivity, low Group Delay Ripple and Insertion Loss. Packaged in a Surface Mount, low profile leadless chip carrier, the DW9276 is ideally suited to high volume automatic assembly systems.



ABSOLUTE MAXIMUM RATINGS

DC Voltage	VDC	0V
Input Power Max.	PIN	10dBm

NOMINAL IMPEDANCE

Input: 648Ω // 25pF
Output: 1177Ω // 19pF

50Ω GPS TEST BOARD COMPONENTS

Input : Series Cap. 11pF, Shunt Ind. 150nH
Output : Shunt Ind. 180nH, Series Cap. 10pF

Components : Coilcraft 1008CS Inductors : Murata 0805 Capacitors

ORDERING INFORMATION

For balanced order DW9276B
For unbalanced order DW9276U

ELECTRICAL CHARACTERISTICS @ 25°C

Parameter	Min.	Typ.	Max.	Units
Centre Frequency (fo)	-	71.0	-	MHz
3dB Bandwidth	±85	±160	-	kHz
Insertion Loss	-	6.0	7.0	dB
Group Delay Ripple	-	200	350	ns
Amplitude Ripple*	-	0.2	0.5	dB
Stopband Rejection:				
fo ±400 - 600kHz	22	25	-	dB
fo ±600 - 1600kHz	28	30	-	dB
fo ±1600 - 3000kHz	38	40	-	dB
fo >±3000kHz	50	53	-	dB
Operating Temperature	-25	-	+80	°C
Temperature Delta	-8.5	-	-	kHz

*Adjacent minima to maxima in 3dB bandwidth.

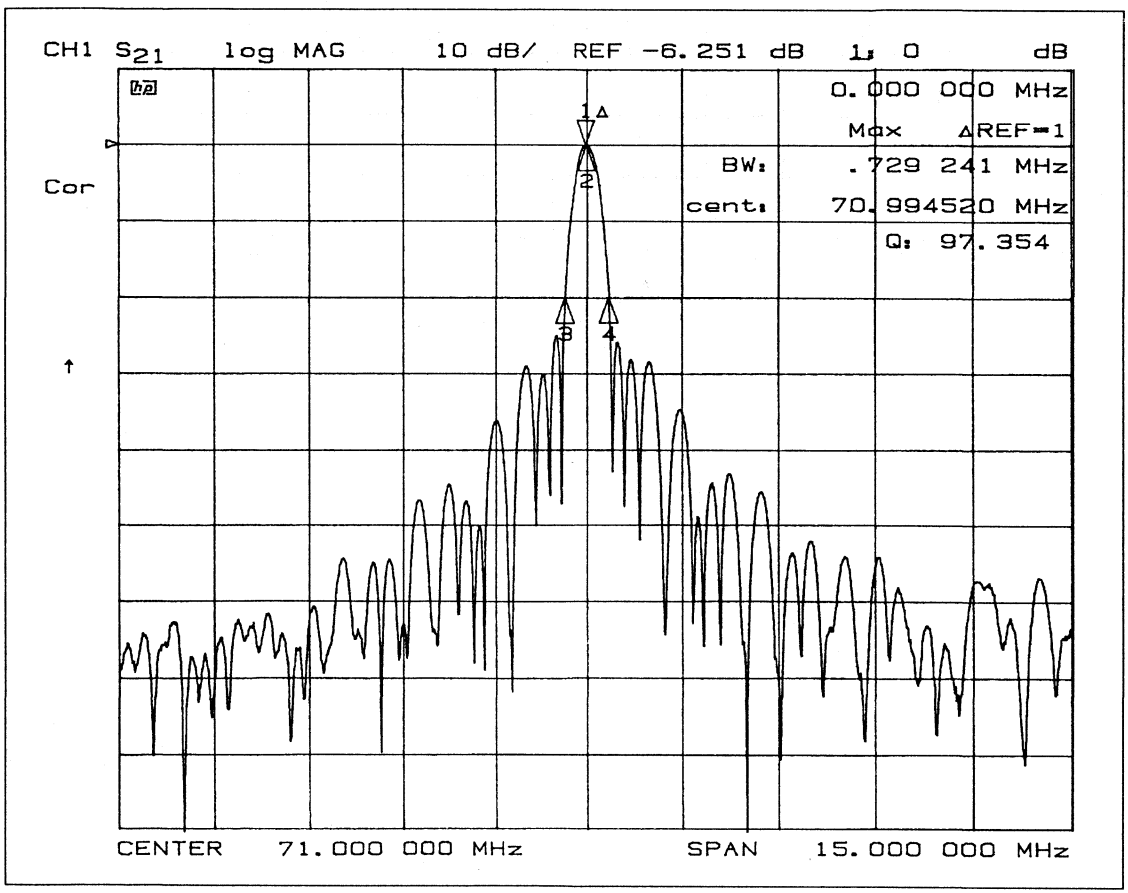


Figure 1: Amplitude Characteristics

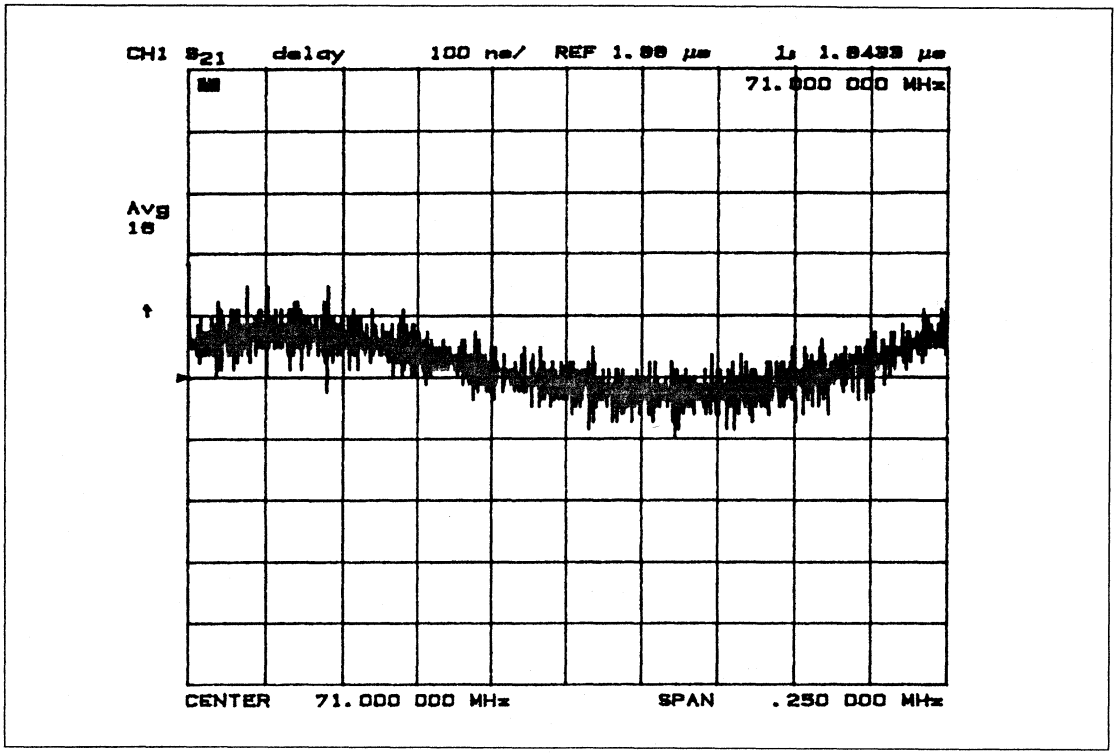


Figure 2: Group Delay Ripple Characteristics

Section 7

IF SAWs for Analog Cellular Communications

GEC PLESSEY
SEMICONDUCTORS

DW9274

92.025MHz IF SAW FILTER FOR E-TACs CELLULAR MOBILE PHONES

The DW9274 SAW filter is a Quartz based device offering narrow band, highly selective performance with excellent temperature stability characteristics, which make it an ideal choice for E-TACs cellular mobile phone requirements.

The device is available in a Surface Mount leadless, ceramic chip carrier suitable for high volume, automated assembly systems.

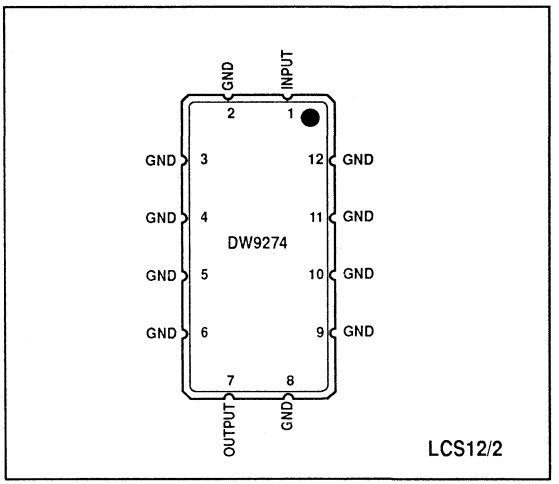


Figure 1

FEATURES

- 92.025MHz Centre Frequency (fo)
- Insertion Loss 3dB (Typ)
- 3dB Bandwidth 30kHz (Min)
- Quartz Temperature Stability
- Low Profile Ceramic SMT Package

ABSOLUTE MAXIMUM RATINGS

DC Voltage VDV	0V
Maximum Input Level	0dBm

ORDERING INFORMATION

DW9274

ELECTRICAL SPECIFICATION @25°C

Parameter	Spec	Typ	Units
Nominal Frequency (fo)	92.025	92.025	MHz
Passband			
Insertion Loss (IL)	4 Max	3	dB
3dB Bandwidth	30 Min	63	kHz
Ripple (fo±15kHz)	1 Max	0.5	dB
Group Delay (fo±15kHz)	-	<4	µs
Stopband			
fo±50kHz	5	7	dB
fo±100kHz	35	40	dB
fo+200kHz to fo +500kHz	25	45	dB
fo+500kHz to fo +1000kHz	40	55	dB
fo-300kHz to fo -900kHz	60	70	dB
fo-900kHz to fo -920kHz	70	75	dB
fo-920kHz to fo -1000kHz	60	70	dB
Maximum Input Level	0	-	dB
Operating Temperature Range	-10 to +65°C		
Package	12 Lead Ceramic LCC 13.6 x 6.8 x 1.93mm (Max).		
Terminating Impedance	850Ω//-2pf		

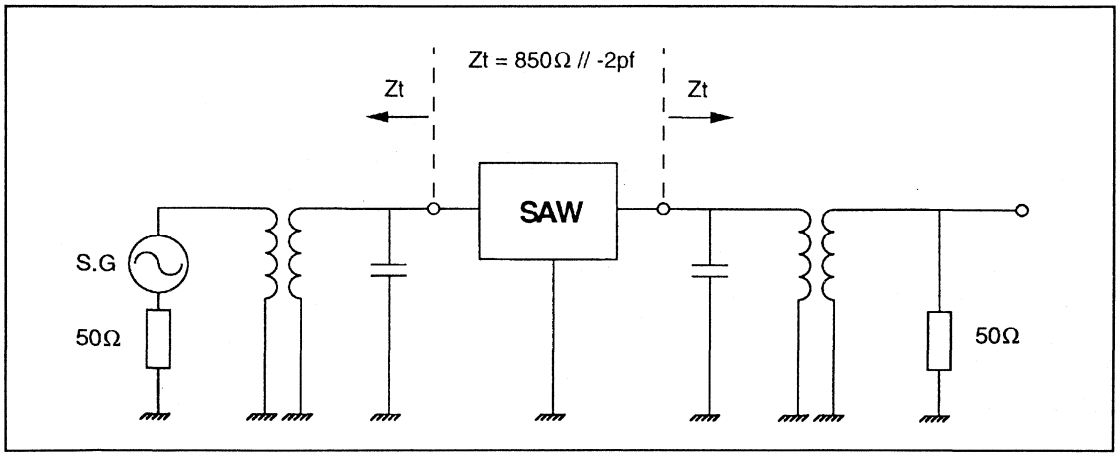


Figure 2: 50Ω Test Circuit

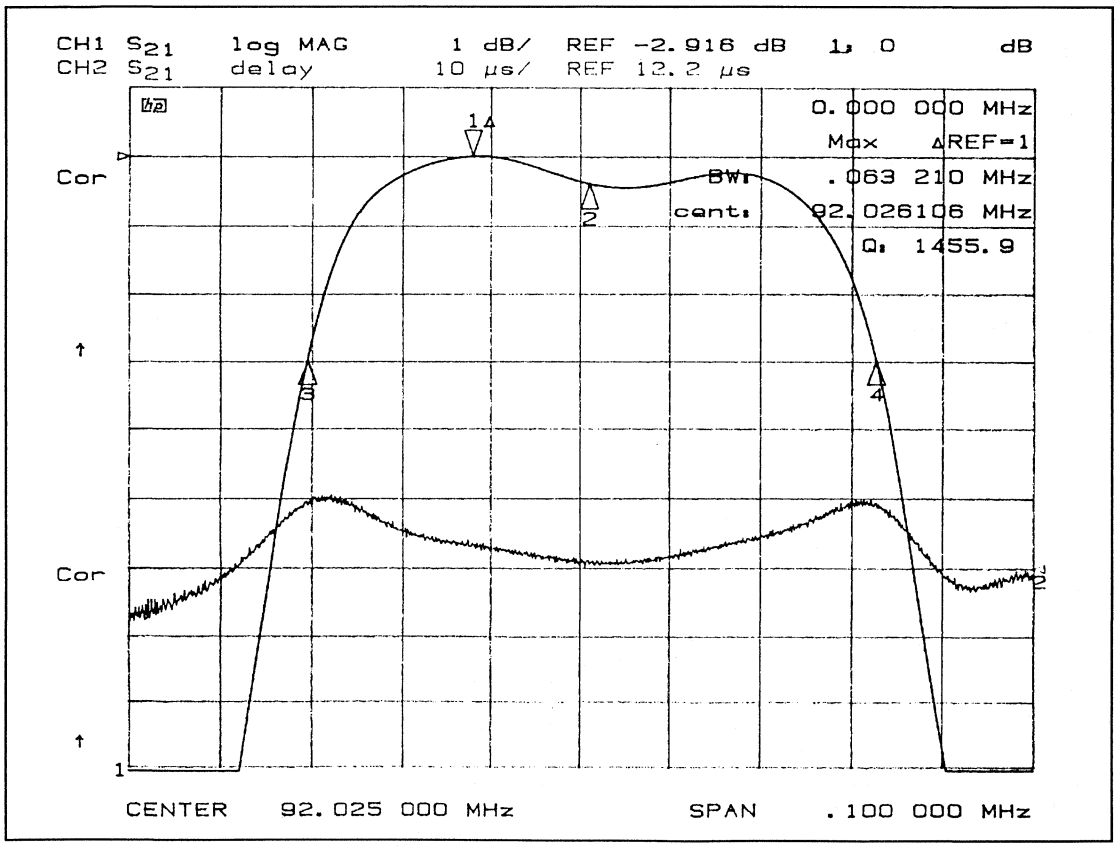


Figure 3: Passband and Group Delay Characteristics

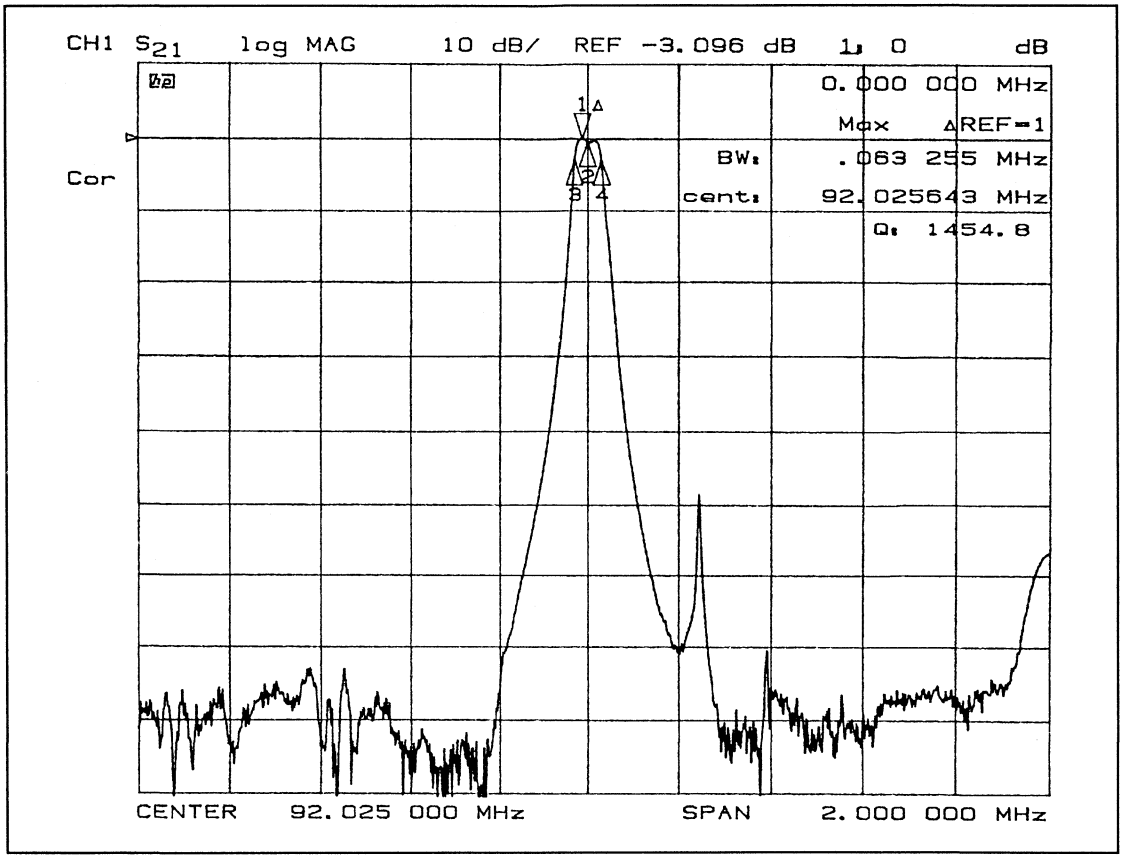


Figure 4: Stopband Rejection Characteristics

Section 8

IF SAWs for Digital European Cordless Telecommunications (DECT)

GEC PLESSEY
SEMICONDUCTORS

PRELIMINARY INFORMATION

DS3811-3.4

DW9249

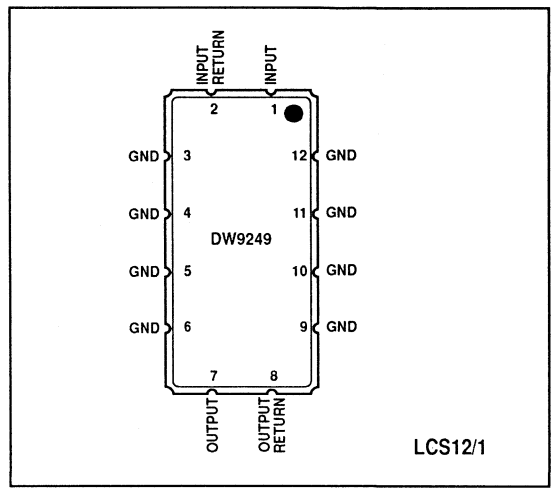
112.32MHz SAW I.F. FILTER FOR DECT PERSONAL COMMUNICATIONS

(Supersedes version in February 1994 Microwave Products Handbook, HB3198-2)

The DW9249 112.32MHz SAW I.F. filter has been specifically developed for the Digital European Cordless Telephone (DECT) market.

By using a centre frequency of 112.32MHz, the DW9249 overcomes the potential problems of 6th and 8th harmonic interference often associated with filters centred at 110.592MHz.

The filter offers excellent temperature stability, (ST-Quartz substrate) plus low Group Delay Ripple (±100ns max.) and is available in the latest, low profile ceramic surface mount package technology.



FEATURES

- Extremely Low Group Delay Ripple
- Wide Operating Temperature
- High Co-channel rejection
- High Adjacent Channel Rejection
- Highly Reproduceable Impedance Characteristics
- Balanced or Unbalanced Drive
- Low Profile Leadless Ceramic Surface Mount Package Suitable for Automated Assembly

ABSOLUTE MAXIMUM RATINGS

DC Voltage	VDC	0V
Input Power Max.	PIN	10dBm

NOMINAL IMPEDANCE

Input: 1.1kΩ // 9.25pF
Output: 1.2kΩ // 12pF

50Ω GPS TEST BOARD COMPONENTS

Input: Series Ind. 180nH, Shunt Cap. 60.7pF
Output: Series Ind. 100nH

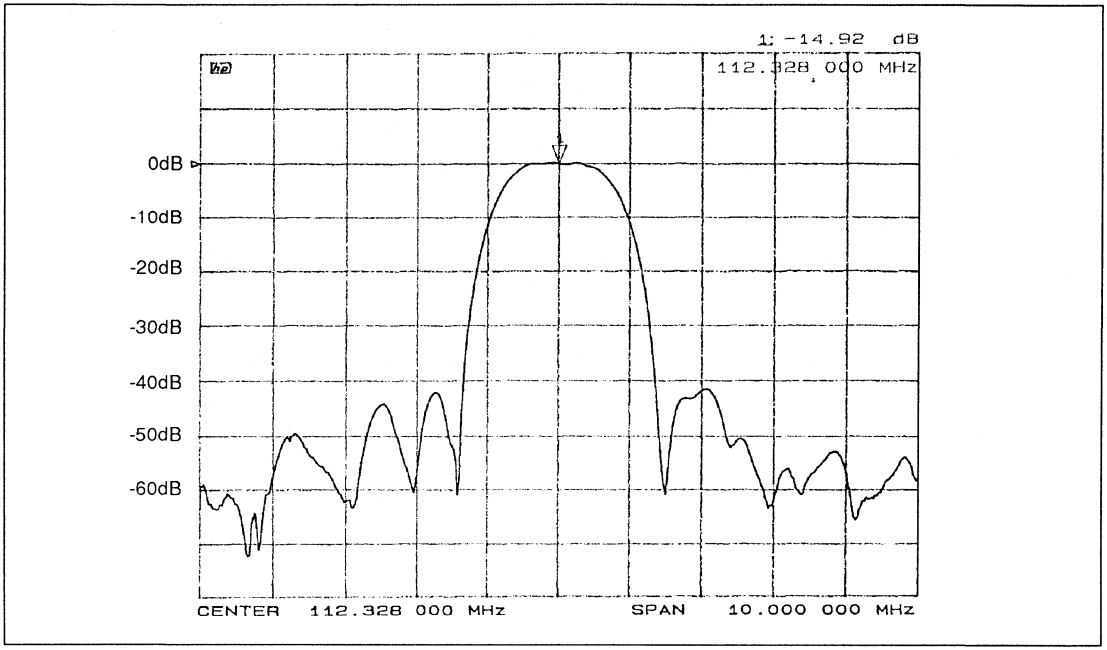
Components: Coilcraft 1008CS Inductors : Murata 0805 Capacitors

ORDERING INFORMATION

DW9249

REFERENCE APPLICATION NOTE:

DW9249 - SAW Bandpass Filter for D.E.C.T.



Typical Response of DW9249

ELECTRICAL CHARACTERISTICS @ 25°C

Parameter	Typ		Units
Centre Frequency (F_O)		112.320	MHz
-3dB Bandwidth	±720	±576	KHz
Group Delay Ripple (F_O±576kHZ)	±80	±100 (Max)	ns
Insertion Loss	15	16 (Max)	dB
Stopband Attenuation:			
F_O ±1.152MHz	20	>15	dB
F_O ±1.728MHz	40	>30	dB
F_O ±3.556MHz	45	>40	dB
F_O ±5MHz	50	>45	dB
Amplitude Ripple (pk to pk)	±0.4	±0.6	dB
Operating Temperature Range		-20 to +85	°C

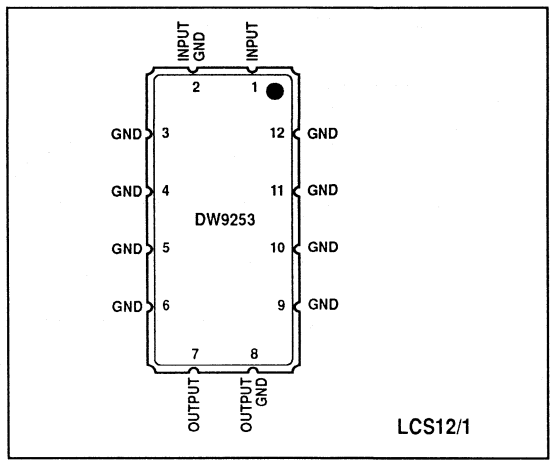
GPS reserves the right to modify these 'datasheets' when necessary to provide optimum performance and cost.

DW9253

110.592MHz SAW I.F. FILTER FOR DECT PERSONAL COMMUNICATIONS

The DW9253 110.592MHz SAW I.F. filter has been specifically developed for the Digital European Cordless Telephone (DECT) market.

The filter offers excellent temperature stability, (ST-Quartz substrate) plus low Group Delay Ripple (±125ns max.) and is available in the latest, low profile ceramic surface mount package technology.



FEATURES

- Extremely Low Group Delay Ripple
- Wide Operating Temperature
- High Co-channel rejection
- High Adjacent Channel Rejection
- Highly Reproduceable Impedance Characteristics
- Balanced or Unbalanced Drive
- Low Profile Leadless Ceramic Surface Mount Package Suitable for Automated Assembly

ABSOLUTE MAXIMUM RATINGS

DC Voltage	VDC	0V
Input Power Max.	PIN	10dBm

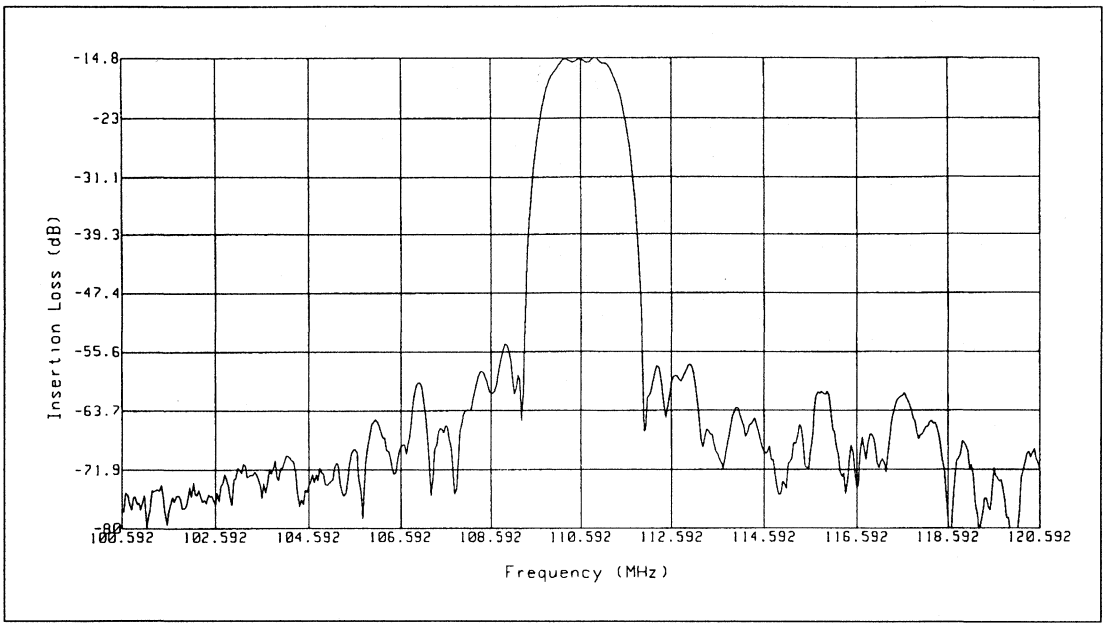
50Ω GPS TEST BOARD COMPONENTS

Input: Series Ind. 180nH, Shunt Cap. 72pF
Output: Series Ind. 100nH

Components: Coilcraft 1008CS Inductors : Murata 0805 Capacitors

ORDERING INFORMATION

DW9253



Typical Response of DW9253

ELECTRICAL CHARACTERISTICS @ 25°C

Parameter	Typ	Min	Units
Centre Frequency (F_O)	110.592		MHz
-3dB Bandwidth	±700	±576	KHz
Group Delay Ripple (F_O±576kHZ)	±95	±125 (Max)	ns
Insertion Loss	15	16 (Max)	dB
Stopband Attenuation:			
F_O ±1.152MHz	20	>15	dB
F_O ±1.728MHz	40	>30	dB
F_O ±3.556MHz	45	>40	dB
F_O ±5MHz	46	>42	dB
Amplitude Ripple (pk to pk)	±0.4	±0.6	dB
Input Impedance		1.1KΩ // 9.25pF	
Output Impedance		1.2KΩ // 12pF	
Operating Temperature Range		-20 to +85	°C

GPS reserves the right to modify these 'datasheets' when necessary to provide optimum performance and cost.

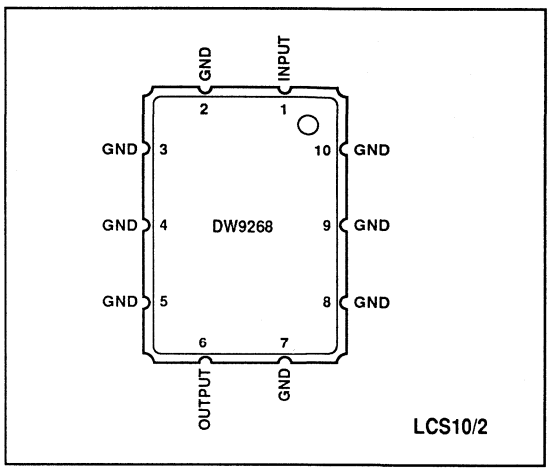
DW9268

240.192MHz IF SAW FILTER FOR CORDLESS DIGITAL PERSONAL COMMUNICATION SYSTEMS

The DW9268 has been designed specifically for the Digital Cordless Personal Communications market as an IF filter with a centre frequency of 240.192MHz. The filter utilises GPS's low loss (7dB typical), Transversal filter technology based on a Quartz substrate for excellent temperature stability.

A 3dB passband of 1.3MHz (typical) is maintained whilst providing rejection to adjacent and alternate interferers compliant to the DECT Common Interface specification Part 2 - The Physical Layer. The device also exhibits excellent close-in and ultimate rejection, which combined with a Group Delay Ripple of 200ns maximum makes the DW9268 and ideal IF filter for Digital Cordless Personal Communications systems.

The device is packaged in a surface mount, leadless ceramic chip carrier, suited to high volume automated assembly systems.



FEATURES

- 240.192MHz Centre Frequency (fo)
- Low Insertion Loss (8dB maximum)
- 3dB Passband 1.3MHz (typical)
- Quartz Temperature Stability
- Low Profile Ceramic LCC Package

ABSOLUTE MAXIMUM RATINGS

DC Voltage	VDC	0V
Input Power Max.	PIN	10dBm

NOMINAL IMPEDANCE

Input: 500Ω // 16pF
Output: 625Ω // 14pF

50Ω GPS TEST BOARD COMPONENTS

Input: Shunt Cap. 45pF, Series Ind. 47nH
Output: Series Ind. 47nH, Shunt Cap. 34pF

Components: Coilcraft 1008CS Inductors : Murata 0805 Capacitors

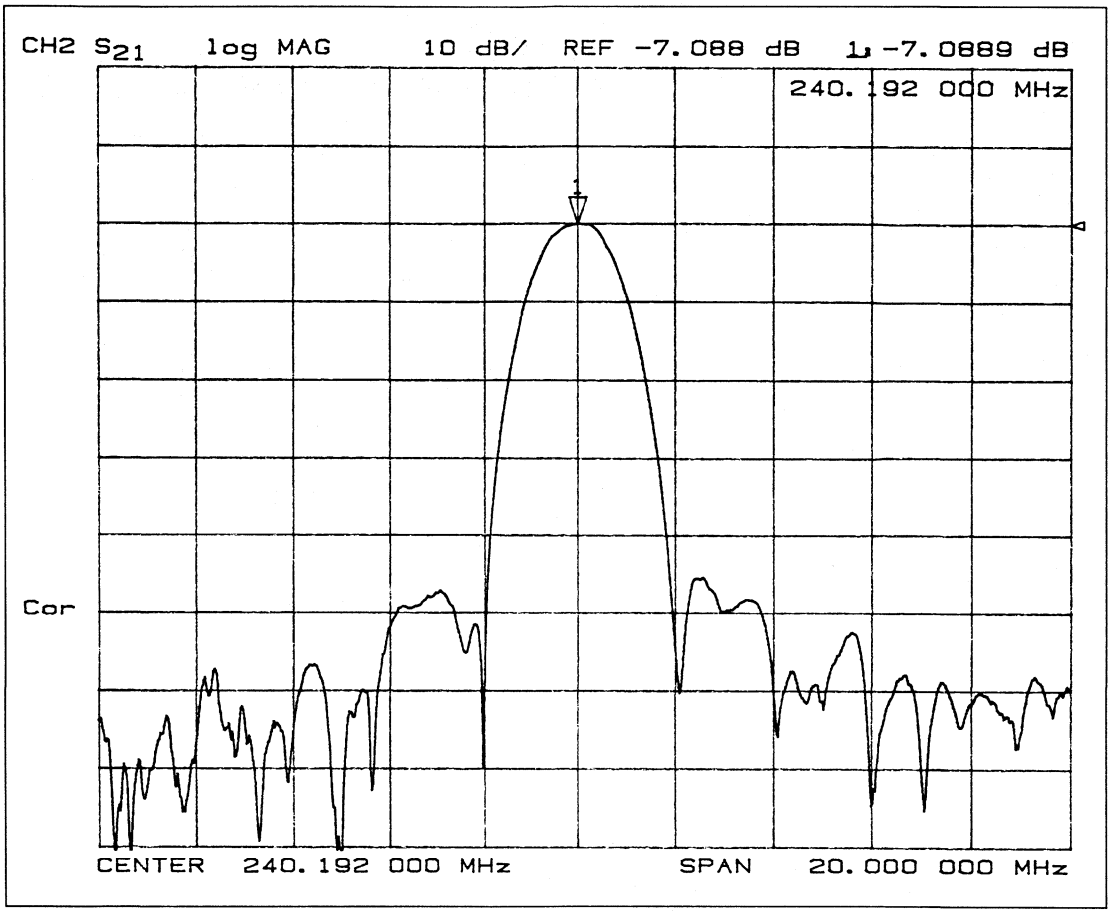
ORDERING INFORMATION

DW9268

ELECTRICAL CHARACTERISTICS @ 25°C

Parameter	Min	Typ	Max	Units
Centre Frequency	-	240.192	-	MHz
3dB Bandwidth	1260	1300	1340	kHz
Insertion Loss	-	7	8	dB
Amplitude Ripple	-	0.2	1	dB
Group Delay Ripple	-	100	200	ns
Stopband Rejection				
fo ± 1.152 MHz	10	12	-	dB
fo ± 1.728 MHz	30	32	-	dB
fo ± 2.880 MHz	40	50	-	dB
fo ± 5.0 MHz	50	55	-	dB
Operating Temperature Range	-20	-	+80	°C

PLOT


CH2 S21 log MAG 10 dB/ REF -7.088 dB 1: -7.0889 dB
240.192 000 MHz
Cor
CENTER 240.192 000 MHz
SPAN 20.000 000 MHz

DW9282

110·592MHz SAW IF FILTER FOR DECT PERSONAL COMMUNICATIONS

The DW9282 is a 110·592MHz SAW filter which has been designed for the first IF section in Digital European Cordless Telephones (DECT).

The filter design has resulted in an insertion loss of 12dB (max.), low group delay ripple of 100ns (typ.), with quartz temperature stability.

The DW9282 is available in a 9mm×7mm outline surface mount package to ensure optimum PCB usage for designers of DECT radios.

FEATURES

- Low Group Delay Ripple
- Low Insertion Loss
- Quartz Temperature Stability
- Balanced or Unbalanced Drive
- Low Profile Surface Mount Package

ABSOLUTE MAXIMUM RATINGS

DC voltage	V_{IN}	0V
Maximum input power	P_{IN}	10dBm

NOMINAL IMPEDANCE

Input:	1420Ω//9·7pF
Output:	1470Ω//9·3pF

50Ω GPS TEST BOARD COMPONENTS

Input (balanced): Series capacitor 8pF, shunt inductor 180nH
Output: Shunt inductor 180nH, series capacitor 3·7pF
Components Inductors: Coilcraft 1008CS
Capacitors: Murata 0805

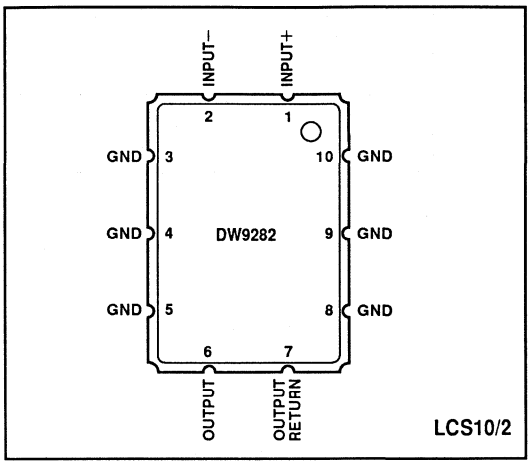


Fig. 1 Pin connections - top view

ORDERING INFORMATION

DW9282

ELECTRICAL CHARACTERISTICS AT 25°C

Characteristic	Value			Units
	Min.	Typ.	Max.	
Centre frequency	110·557	110·592	110·627	MHz
3dB bandwidth	1000	1080		kHz
Insertion loss		10	12	dB
Amplitude ripple		0·2	1	dB
Group delay ripple		100	400	ns
Stopband Rejection				
$f_C \pm 1{\cdot}185$MHz	12	18		dB
$f_C \pm 1{\cdot}223$MHz	13	19		dB
$f_C \pm 1{\cdot}738$MHz	35	50		dB
$f_C \pm 1{\cdot}960$MHz	45	50		dB
$f_C \pm 2{\cdot}304$MHz	45	50		dB
$f_C \pm 4{\cdot}608$MHz	45	50		dB
Operating temperature range	−10		+60	°C

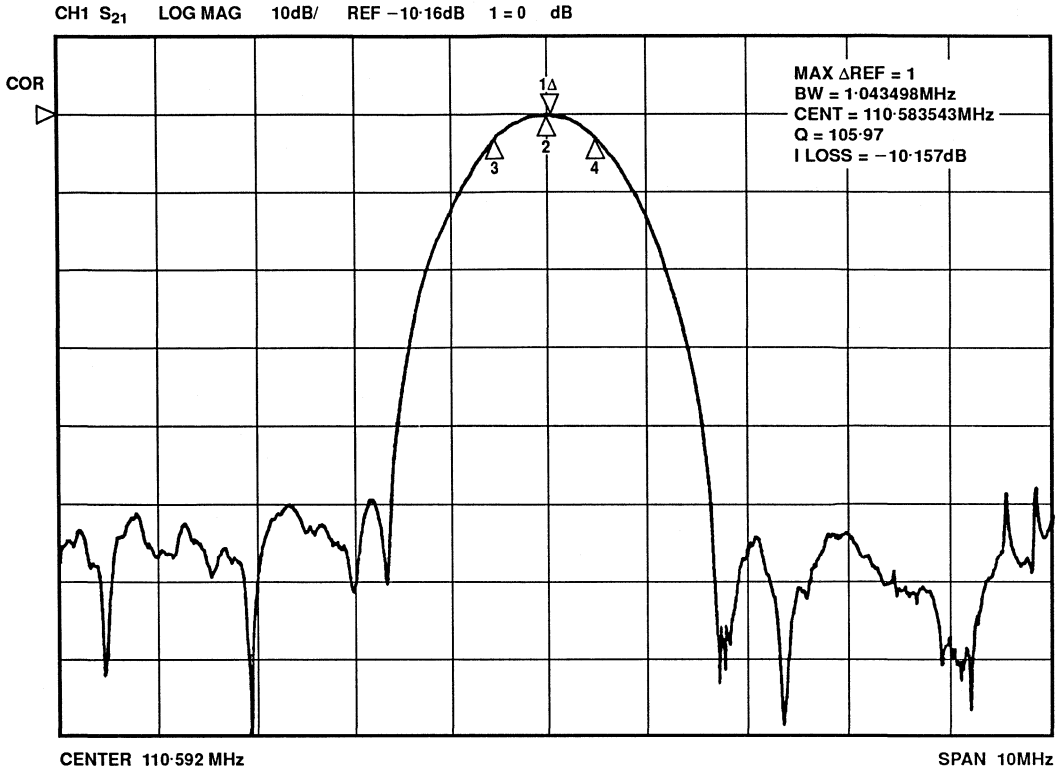


Fig. 2 DW9282 response

Section 9

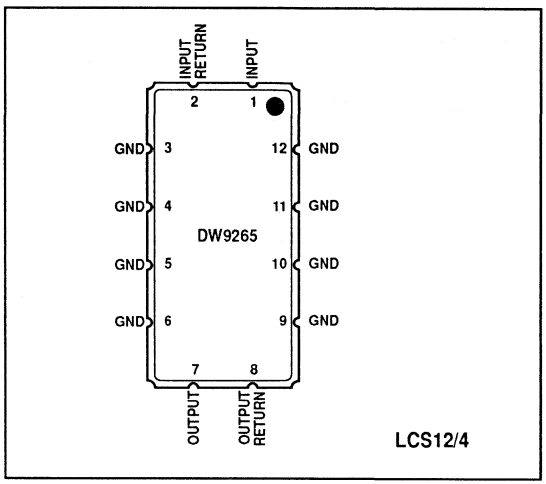
IF SAWs for Personal Communications Systems (PCS)

GEC PLESSEY
SEMICONDUCTORS

DW9265

196.99MHZ IF SAW FILTER FOR DIGITAL COMMUNICATIONS

The DW9265 is a 196.99MHz IF SAW filter for Wireless Digital Personal Communications Systems. A transversal structure, based on quartz, has been utilised to provide a design with excellent temperature stability over -10° to +60°C. With a typical 3dB passband of 576kHz, and in excess of 50dB rejection at fc ±2.0MHz, the filter provides good adjacent channel performance and low inter-symbol interference. The DW9265 also exhibits a low Group Delay Ripple (100ns typ.) and an in-band Amplitude Ripple of 0.2dB, thus making it the ideal choice for Digital Communications, especially for the unlicensed PCS, low range voice and data services market.



FEATURES

- 196.99MHz Centre Frequency (fc)
- Low Insertion Loss (9dB max.)
- 3db Passband 560kHz (min.)
- Quartz Temperature Stability
- Low Profile Ceramic LCC Package

ABSOLUTE MAXIMUM RATINGS

DC Voltage	VDC	0V
Input Power Max.	PIN	10dBm

NOMINAL IMPEDANCE:

Input : 500Ω//16pF
Output : 625Ω//14pF

50Ω GPS TEST BOARD COMPONENTS

Input : Series Cap. 10pF, Shunt Ind. 27nH
Output : Series Ind. 56nH, Shunt Cap. 33pF

Components : Coilcraft 1008CS Inductors : Murata 0805 Capacitors

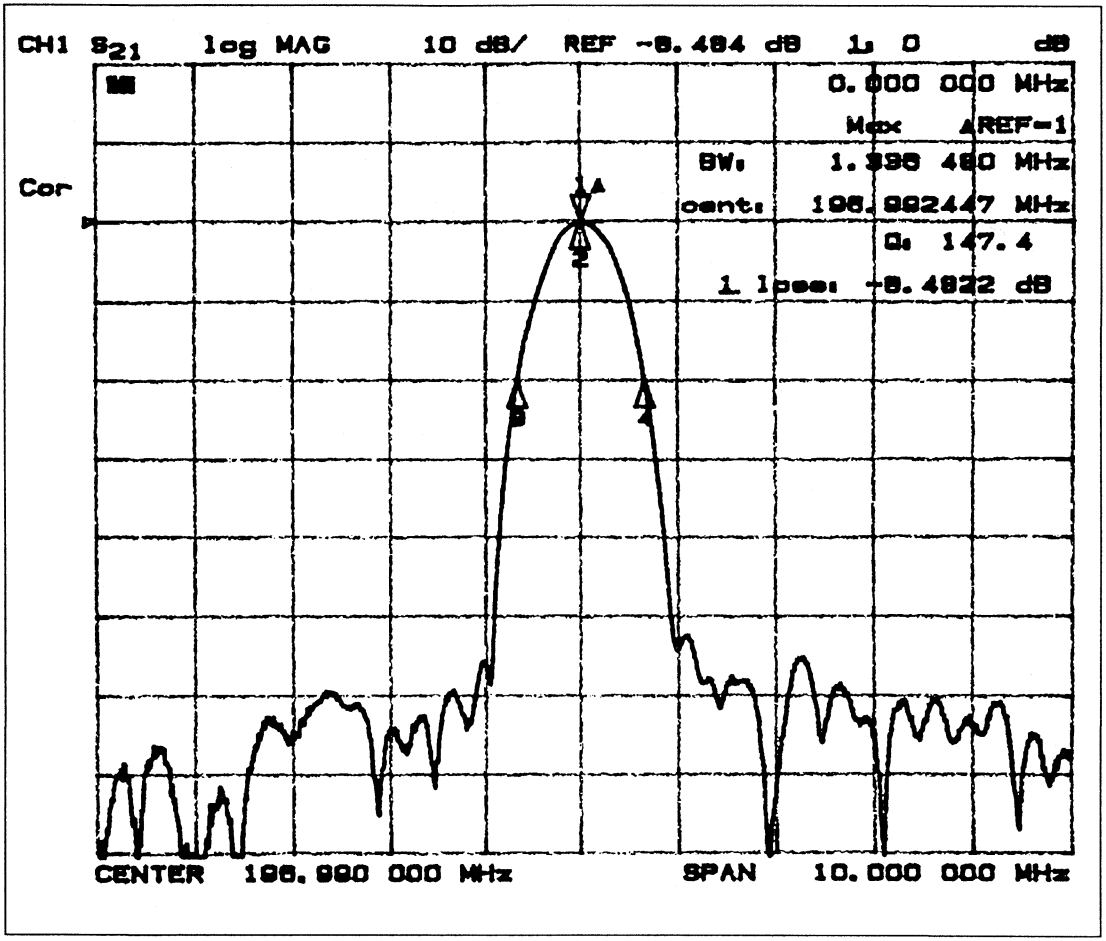
ORDERING INFORMATION

DW9265

ELECTRICAL CHARACTERISTICS @ 25°C

Parameter	Min.	Typ.	Max.	Units
Centre Frequency (fc)	196.96	196.99	197.02	MHz
3dB Bandwidth	560	576	592	kHz
Insertion Loss	-	8.0	9.0	dB
Group Delay Ripple	-	100	200	ns
Amplitude Ripple	-	0.2	1.0	dB
Stopband Rejection:				
fc ±0.750MHz	20	25	-	dB
fc ±1.550MHz	55	60	-	dB
fc ±3.1 - ±8MHz	55	60	-	dB
Over 1MHz bandwidths centred at		55	-	dB
fc - 10.0MHz	55	60	-	dB
fc - 20.0MHz	55	70	-	dB

Operating Temperature Range: -10 to +50°C



Typical Response of DW9265

Section 10

IF SAWs for Wireless Local Area Networks (WLAN)

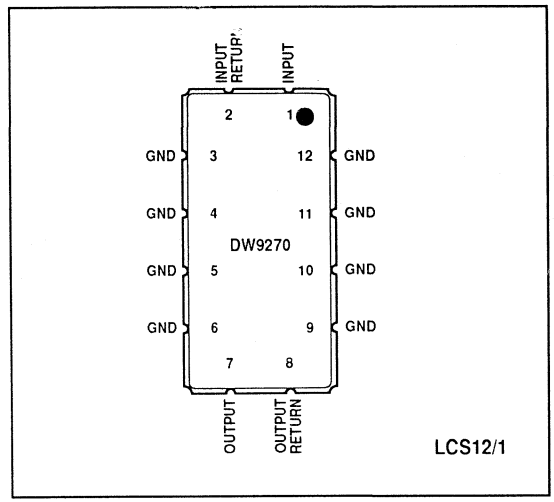
DW9270

240MHz IF SAW FILTER FOR DIGITAL WIRELESS COMMUNICATIONS

The DW9270 has been designed specifically for the Digital Wireless Communications market, as an IF filter with a centre frequency of 240MHz. The filter utilises GPS's low loss (8.5dB typical), Transversal filter technology based on a Quartz substrate for excellent temperature stability.

With a typical 3dB passband of 1MHz, and an adjacent channel rejection of 12dB (min.) the device exhibits excellent close-in and ultimate rejection, which combined with a Group Delay Ripple of 200ns (max.) makes the DW9270 an ideal IF filter for Digital Wireless Communications systems.

The device is available in a surface mount ceramic chip carrier suited to high volume automated assembly systems.



FEATURES

- 240MHz Centre Frequency (fo)
- Low Insertion Loss (10dB max.)
- 3dB Passband 1.05MHz (typ.)
- Quartz Temperature Stability
- Low Profile Ceramic LCC Package

ABSOLUTE MAXIMUM RATINGS

DC Voltage	VDC	0V
Input Power Max.	PIN	10dBm

NOMINAL IMPEDANCE

Input: 255Ω // 14pF
Output: 400Ω // 11.5pF

50Ω GPS TEST BOARD COMPONENTS

Input: Shunt Cap. 27pF, Series Ind. 47nH, Shunt Cap. 1.5pF
Output: Shunt Cap. 1.5pF, Series Ind. 47nH, Shunt Cap. 30pF

Components: Coilcraft 1008CS Inductors : Murata 0805 Capacitors

PACKAGE

13.5mm x 6.5mm : 12 Lead SMD

OPERATION

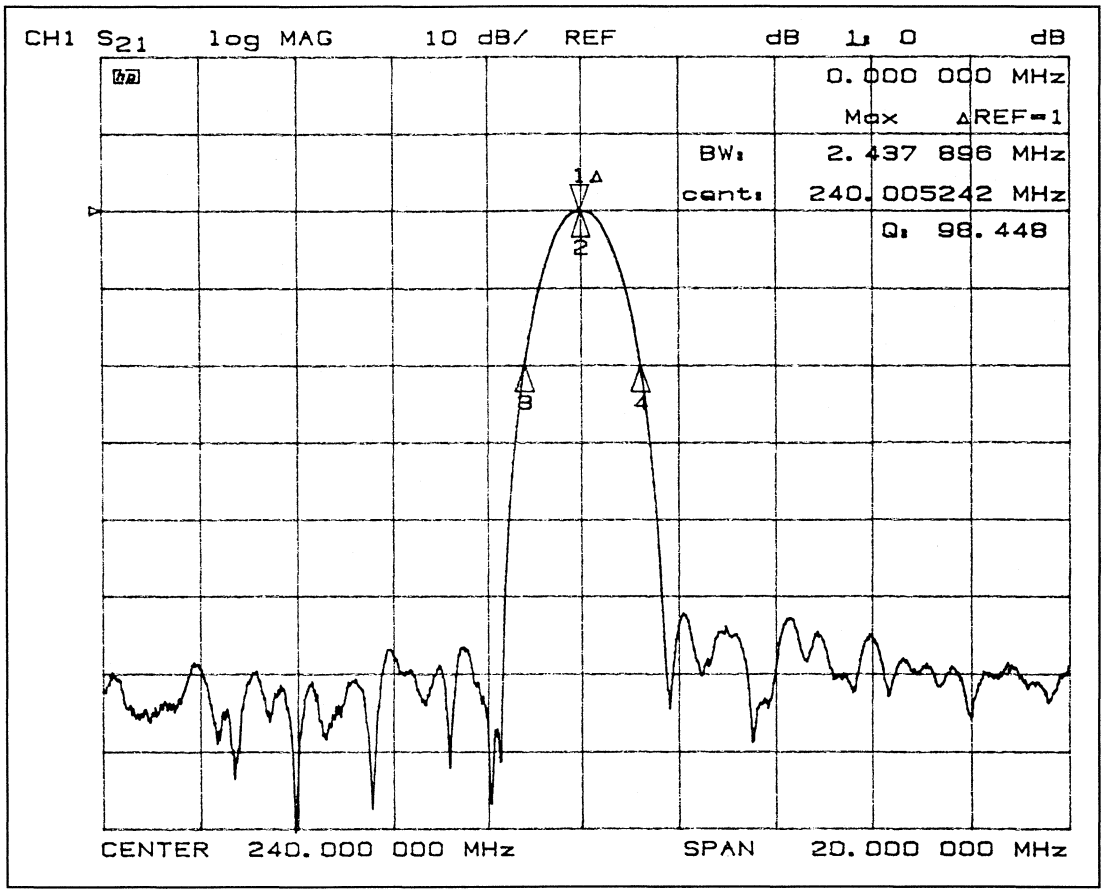
Balanced or Unbalanced configuration available.

ORDER INFORMATION

DW9270

ELECTRICAL CHARACTERISTICS @ 25°C

Parameter	Min	Typ	Max	Units
Centre Frequency	239.96	240	240.40	MHz
3dB Bandwidth	1000	1050		kHz
Insertion Loss	-	8.5	10	dB
Amplitude Ripple	-	0.2	1	dB
Group Delay Ripple	-	50	200	ns
Stopband Rejection				
fc ± 1.0 MHz	11.0	13	-	dB
fc ± 1.75 - 2.5 MHz	44	55	-	dB
fc ± 2.50 - 3.50 MHz	48	55	-	dB
fc ± 3.50 - 50.0 MHz	50	60	-	dB
Operating Temperature Range	-20	-	+60	°C


CH1 S21 log MAG 10 dB/ REF dB 1: 0 dB
0.000 000 MHz
Max ΔREF=1
BW: 2.437 896 MHz
cent: 240.005242 MHz
Q: 98.448
CENTER 240.000 000 MHz
SPAN 20.000 000 MHz

Section 11
Application Notes

GEC PLESSEY
SEMICONDUCTORS

AN-94

USING THE NJ88C33 PLL SYNTHESISER

Abstract:

A tutorial intended to assist with the understanding of the basic parameters of a single-loop, phase-feedback frequency locked oscillator. Since the uses of phase-locked loops are many and varied, only a sample of their uses and design equations have been given here. Some mathematical ability is necessary to deal with the ideas expressed. To assist, all working has been shown for the derivation of the formulae. The aim of this note is to encourage manipulation of the variables and build confidence with phase-locked loop parameters in general. It is recommended that all formulae derivations are followed through with pencil and paper to gain a full understanding of their function. The NJ88C33 has been used as the particular example.

Introduction

The NJ88C33 is a single chip solution for VHF PLL Synthesis, capable of lower levels of phase-noise than earlier PLL ICs since it uses current source outputs from the phase detector to charge pump a passive loop filter, rather than the active types favoured previously. The simplest type of practical loop using this phase detector is of "the third order, type two". An analysis of these loops is not generally available from control theory books, prompting the generation of this Tutorial Note.

In Part A we introduce the NJ88C33. The implementation of a third order charge pumped phase-locked loop is examined in Part B where the loop equations are developed using standard control theory to predict the time and frequency responses for the basic loop. Part C is devoted to bench measurements of the parameters involved to prove the equations of Part B and explains the use of the evaluation card and a simple programming board to gain an insight into how the device works with its programming sequences. This section also covers a discussion of commonly encountered problems when designing circuits using synthesiser ICs, along with an examination of the sensitive areas of the NJ88C33. Last, but not least, is a series of Appendices which deal with the derivation of the basic concepts behind the formulae used in the loop analysis.

Please contact your local GPS Customer Service Centre for copies of this Application Note.

DW9249 Application Note

SAW BANDPASS FILTER FOR D.E.C.T.

SELECTION OF IF FREQUENCY:

The DW9249 is a S.A.W. Bandpass Filter designed specifically for use in Digital European Cordless Telephones (D.E.C.T.). A circuit schematic of a typical DECT receiver architecture is shown in Fig. 1. In this design a superhet philosophy is employed, using an Intermediate frequency (I.F.) at typically 110 to 112 MHz. Early designs of DECT receivers used 110.592 MHz but more recently this has been avoided owing to 6th or 8th harmonic leak through from either an 18.432MHz or 13.824 MHz reference oscillator. For this reason 112.32 MHz has now become a preferred standard.

DECT DESIGN CONSIDERATIONS:

The DW9249 operates at 112.32MHz and has an minimum operating 3dB bandwidth of 1200 KHz. The modulation rate and type specified within DECT demand an operating bandwidth of ±576 KHz under all conditions. Furthermore the DECT standard specifies a co-channel performance of 10dB and 15dB adjacent channel interference performance. These two requirements should be met allowing for all manufacturing, ageing and temperature tolerances. Overall allowance for these parameters, translates into a tight specification on the filter roll-off (shaping) characteristics.

An operating temperature range of -20°C to +85°C is recommended with a minimum requirement of 0°C to +40°C. It is for this reason that ST Quartz is used by GEC Plessey Semiconductors as the substrate medium. Lithium Niobate based devices have extremely poor temperature performance with Lithium Tantalate being only marginally better. If the latter of these materials were to be employed then operational performance could only be guaranteed over the restricted temperature of 0°C to 40°C. For this reason Lithium Tantalate based devices have been primarily restricted to use in Test Systems enjoying a controlled climatic environment. On the other hand, the advantages from the use of Quartz as a substrate medium substantially improves the device manufacturability and co-channel/adjacent channel interference performance.

SAW FILTER DESIGN OPTIONS:

The next issue in the choice of design of Filter for DECT filtering has been the trade-offs between the demands for low Insertion Loss and low Group Delay ripple. Unlike many pure analogue communications systems, particular attention must be paid in digital communications to the phase or group delay ripple parameters of components. Phase distortion will

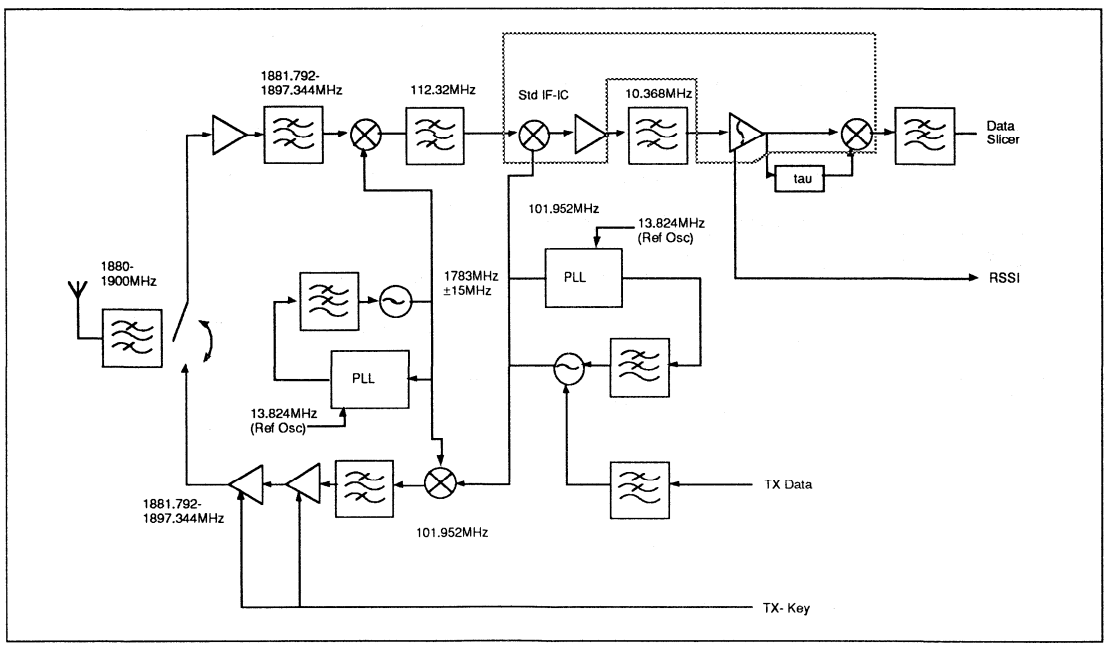


Figure 1: Block Diagram of a Typical 2GHz Radio

contribute directly to system Bit Error Rate (BER). Most DECT system designers have settled on an upper limit of allocation to the SAW filter group delay ripple at 300nS.

The choice is all the more complicated by the fact that SAW fillers can be realised in fundamentally one of two different ways: as Resonator filters or as Transversal filters. A comparison of the relative performance of SAW resonator and transversal filters is given in Table 1.

In brief, SAW Resonators can provide DECT system designs with low insertion loss filters hence reducing the gain and associated current consumption. This is achieved however at considerable expense overall on the system performance and manufacturability. Group delay ripple for a DECT based design resonator filter is typically five to ten times higher than that for a typical transversal filter at ambient. This figure can degrade further under full operating temperature conditions and time; matching impedances are highly sensitive; impedance matching networks are complicated by the need commonly to interface into an unbalanced mixer; co-channel rejection can be marginal against specification over the operating temperature range.

Saw bi-directional transversal filters on the other hand have an insertion loss of typically 14-16dB, and may require additional gain. However the filter has many compensating features including:

1. Excellent co-channel characteristics
2. Time and temperature stable matching impedances permitting simple, single element, fixed value matching components
3. Option for balanced or unbalanced drive networks
4. Exceptionally low group delay ripple
5. Operation over either the full or extended DECT temperature range
6. Good third order intercept point

In conclusion, GEC Plessey Semiconductors recommend the adoption of a ST cut Quartz Transversal filter - DW9249 for use as an 112.32MHz IF filter in DECT receivers.

	ADVANTAGES	DISADVANTAGES
TRANSVERSAL FILTER DESIGN	V.Low Group Delay Ripple Stable Matching Impedances Balanced/Unbalanced Drive Good Stopband Rejection	Increased Insertion Losses Restricted Minimum Fraction Bandwidth >0.3% Increased Size
RESONATOR FILTER DESIGN	V.Low Insertion Loss V.Narrow Fractional Bandwidths Good Co-Channel Selectivity	V.Poor Group Delay Ripple Unbalanced Drive Option Only Mediocre Stop Band Rejection

Table 1: SAW Filter Technology Comparison

CIRCUIT MATCHING NETWORK:

Significantly, the SAW filter is designed asymmetric with the input and output impedances configured independently. Furthermore, the SAW frequency response is purposefully designed to have an asymmetric amplitude characteristic when measured unmatched in 50 ohms, but a symmetric amplitude when appropriately matched into the correct impedances. Two options for matching configurations are presented here:

1. Input: 50 ohms / Unbalanced drive
   Output: High Impedance IF Downconversion chip / Balanced drive

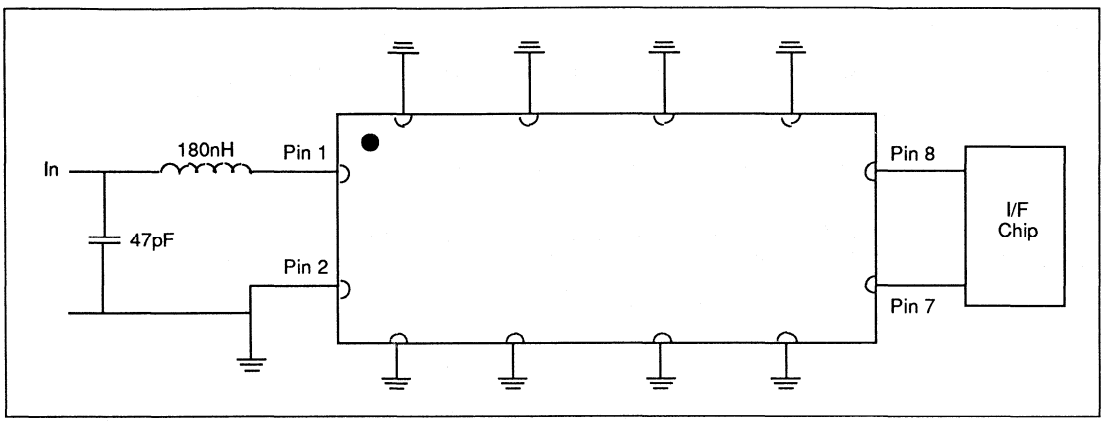


Figure 2

2. Input: 50 ohms / Unbalanced
   Output: 50 ohms / Unbalanced drive

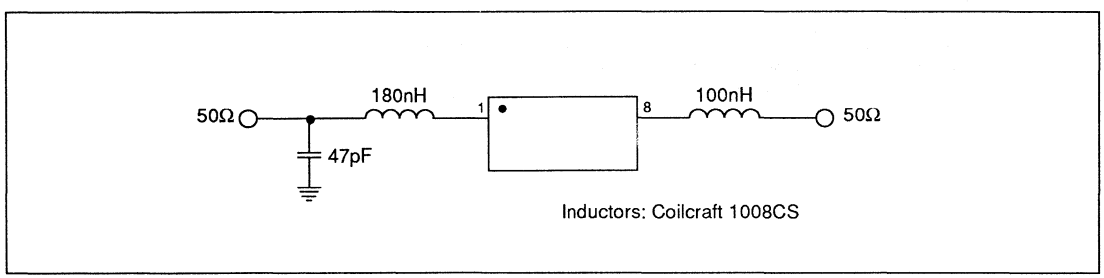


Figure 3

UPGRADING AN SL6609 DESIGN TO USE THE SL6609A

The SL6609 direct conversion paging receiver has been superseded with the improved performance SL6609A. The new SL6609A is 100% pin compatible with the SL6609.

The main improvements to the SL6609A are:

1. Improved RF mixer noise figure allowing better IP3 and Adjacent Channel Rejection for the same Sensitivity.
2. Improved internal VR Voltage Reference (pin 6) amplifier stability.

If an SL6609 is replaced with an SL6609A in the standard application circuit shown in Fig.1, then a 1dB increase in Sensitivity will typically be observed.

If the RF amplifier gain is reduced, by decreasing the value of R13 as described in the adjustment procedure below, then a Sensitivity of -126 dBm at 1200bps should be achieved with IP3 and Adjacent Channel Rejection figures as below :

58 dB IP3 (5 dB improvement on SL6609 figure)

72 dB Adjacent Channel Rejection (3 dB improvement)

SL6609A Optimum Adjustment Procedure Referring to Fig.1

1. The RF INPUT should be checked for a good 50ohm match.
2. Apply an RF signal of -73 dBm, offset from the local oscillator by the deviation frequency, to the RF INPUT.
3. Reduce the value of R13 until the level measured at pin 1 (TPX) is 120mV ± 10mV peak to peak, measured with a high impedance 10:1 scope probe.
4. Check for good quadrature between the two test points pin 1 (TPX) and pin 7 (TPY) and an amplitude imbalance of less than 10%. If the amplitude balance between the two pins requires correction, then the value of C5 should be slightly increased and the value of C2 slightly decreased.

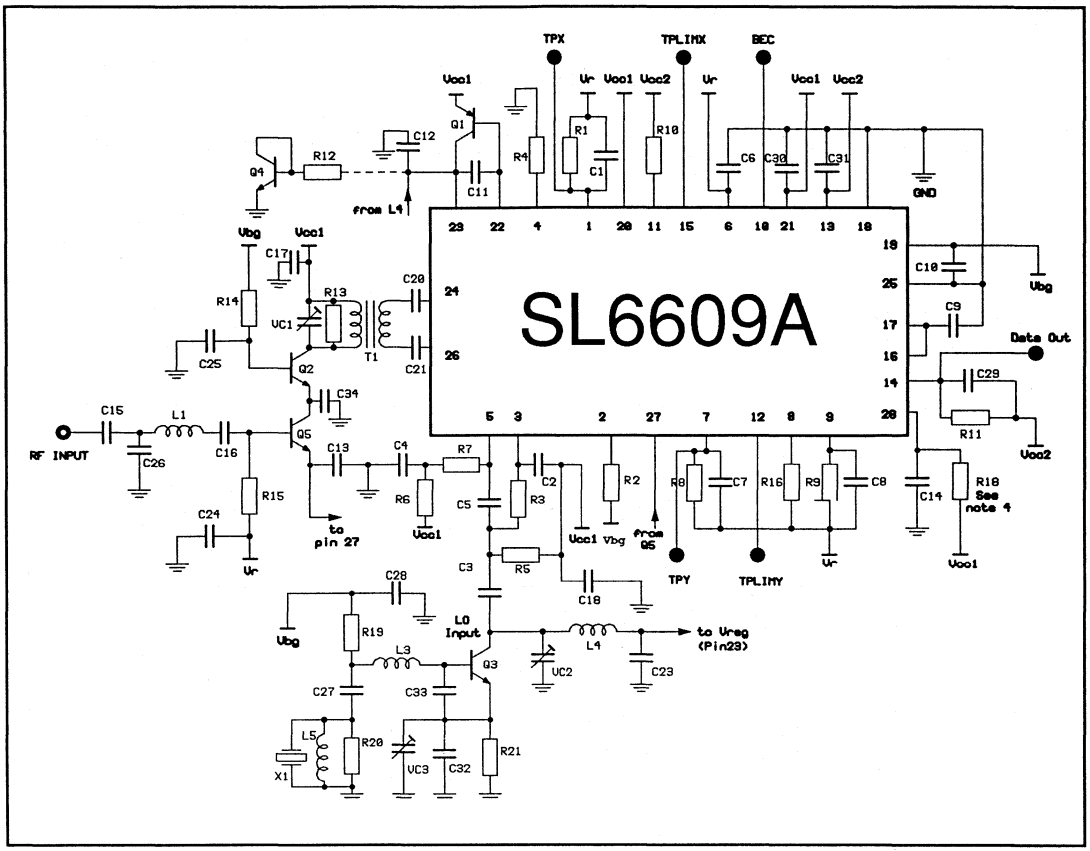


Fig.1 Application circuit board

SL6609A

ADVICE ON USING THE SL6609A DIRECT CONVERSION RECEIVER

Introduction

This application note outlines a basic circuit for the SL6609A Direct Conversion Pager Receiver for use in standard paging applications at 153MHz, 282MHz and 450MHz.

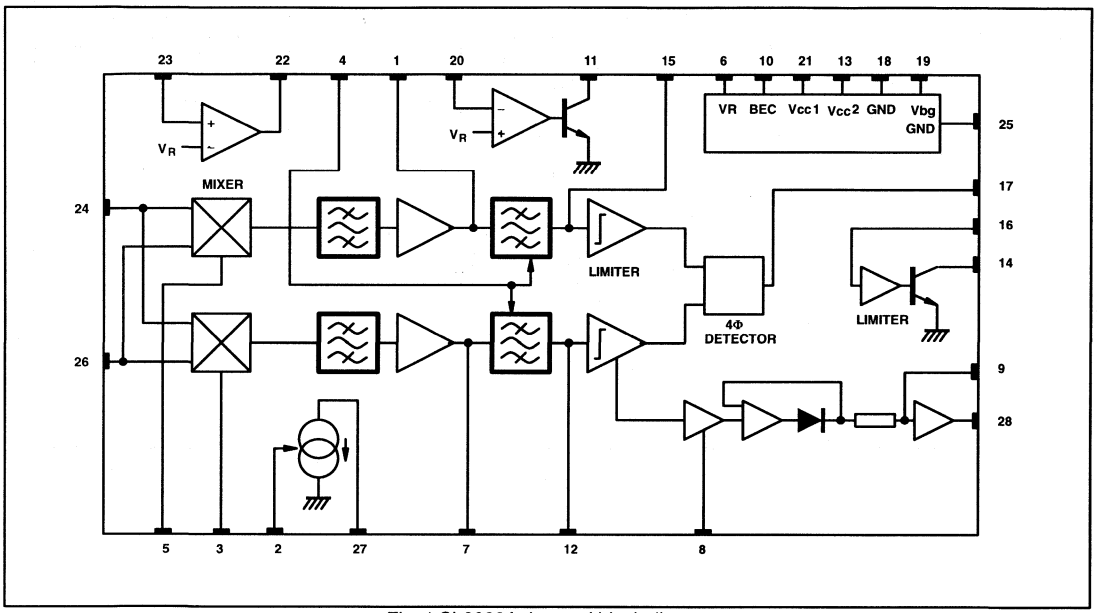


Fig. 1 SL6609A Internal block diagram

SL6609A Pin Description

A schematic of the SL6609A is shown in Fig. 1. This shows the pin allocation and the internal structure of the device.

Pin No	Pin Name	Pin Description	Pin Details
1	TPX	Channel X test point	Channel X internal amplifier output/Gryrator filter input. This pin is used to measure the receiver signal level during receiver set–up. It may also be used in conjunction with Pin 15 (TPLIMX) to measure the response of the Gyrator filters. It can be used to add additional filtering in the channel in the form of an additional external capacitor.
2	RFIADJ	Current Source ADJ	Pin 2 allows adjustment of the current source which is designed for use with the external RF amplifier. See "Circuit Facilities".
3	LOY	Mixer L.O. input	The local oscillator signal is applied to Pin 3 in phase quadrature to Pin 5. For the phase quadrature circuit see "RF Amplifier and Local Oscillator Network". The L.O. input of the mixers require a bias path to Vcc1 (see R5 & R6 on the Applications Circuit in Fig.2).
4	GYRI	Gryrator Filter Adjust	The bandwidth of the on–chip gyrator filter can be adjusted using a resistor from Pin 4 to GND. For values see "Set–up for Optimum Performance".
5	LOX	Mixer L.O. Input	See Pin 3
6	VR	Voltage reference VR	1V internal reference voltage. It may be used for the bias of external RF Amplifier and L.O. circuits. It is also a reference for Pins 1,7,8, and 9.
7	TPY	Channel Y.	Channel Y internal amplifier output/Gyrator filter input. This pin is used to measure the received signal level during receiver set–up. It may also be used in conjunction with Pin 12 (TPLIMY) to measure the response of the gyrator filters. It can be used to add additional filtering in the channel in the form of an additional external capacitor.
8	GTHADJ	Audio AGC Level ADJ.	Level adjustment for the external AGC drive. See Fig. 5. The voltage at Pin 8 is dictated by an external resistor (R16 in Applications Circuit) and an internal current source driven by the wanted audio (baseband) signal level. With no signal input to the receiver, the output of current source 1 tends to zero and so the voltage at Pin 8 is VR. This gives the result that the output of current source 2 (Pin 28) tends to ~0μA. (i.e. the AGC is disabled). With a signal incident on the receiver, current source 1 driving Pin 8 is turned on and there is a voltage drop across the external resistor (R16). The value of the external resistor (R16) dictates the voltage drop and hence the sensitivity of the AGC circuit. For a value of the external resistor (R16), see the Application Circuit.
9	TCADJ	Audio AGC Time Constant	The attack (turn on) and decay (duration) times of the Audio AGC are set by an RC network connected to Pin 9. See Application Circuit for details.
10	BEC	Battery Economy	The battery economy facility allows the device to be powered down by pulling Pin 10 to GND. If not required this should be connected to Vcc2.
11	BATTFL	Low Battery Flag O.P	The battery flag is the output of an on–chip comparator with VR as the reference voltage. When VBATT (Pin 20) > VR, Battery Flag O/P is Low. BATTFL is an open collector output.
12	TPLIMY	Channel Y Gyrator Filter Output	See Pin 7. Pin 12 provides a monitor of the gyrator filter output of channel Y to enable the response of the filter to be accurately measured and adjusted using Pin 4. For details refer to "Set–up for Optimum Performance".

Pin No	Pin Name	Pin Description	Pin Details
13	Vcc2	Vcc2	Vcc2 supply. This pin requires adequate audio decoupling to GND. If a DC–DC converter is used to generate this voltage care must be taken to prevent power supply noise reducing the sensitivity of the device.
14	DATAOP	Data Output	Open collector data output. This requires a pull–up resistor to a suitable voltage reference.e.g. Vcc2.
15	TPLIMX	Channel X Gyrator Filter Output	See pin 1. Pin 15 provides a monitor of the gyrator filter output of channel X, to enable the response of the filter to be accurately measured and adjusted using Pin 4. For details refer to"Set–up for Optimum Performance".
16	BRF2	Data Buffer Input	Input to the data limiter. This pin is normally connected directly to Pin 17.
17	BRF1	Phase Detector Output	Output of the phase detector. For optimum performance a Bit Rate filter can be applied to this pin. This is achieved by applying a capacitor between Pin 17 and GND. The value of this capacitor is dependent on the data rate. For the value of this capacitor see "Set–up for Optimum Performance".
18	DIGGND	Digital GND	This is the ground for the digital circuits in the receiver.
19	VBG	Bandgap Voltage VBG	Bandgap voltage reference (1.2V). This may be used to bias an external RF amplifier. See "Application Circuit Requirements" for details.
20	VBATT	Battery Flag Input	Connect this pin to Pin 21 (Vcc1) if a 1 volt threshold is required. Alternative thresholds may be determined using an external potential divider. See "Application Circuit Requirements" for details.
21	Vcc1	Vcc1	Vcc1 supply. This requires adequate Audio and RF decoupling if optimum device sensitivity is to be achieved.
22	REGCNT	Voltage Regulator Control OP	1V on–chip voltage regulator output. Used to drive a suitable PNP transistor. See "Set–up for Optimum Performance". For stability purposes a capacitor should be applied between Pin 22 and Pin 23. The regulator is only specified for Vcc1 $\geq$ 1.1V.
23	VREG	Voltage Regulator Sense	This should be connected to the load of the regulator. If the regulator is not required, and no active components are connected to Pin 22 and Pin 23, then Pin 23 should be connected to Vcc2.
24	MIXB	Mixer RF Input B	Input to the device from an external RF amplifer. The signal should be applied differentially between Pin 24 and Pin 26. The differential signal to the mixers may be DC coupled if no DC voltage is applied, otherwise AC coupling should be used.
25	GND	Receiver ground	Ground for receiver RF circuits.
26	MIXA	Mixer RF input A	Differential input from an external RF amplifier. See Pin 24.
27	IRFAMP	Current Source Output IRF	An on chip current source for use in RF amplifier designs. This allows the current in the RF amplifier to be independent of supply voltages. See "Application Circuit Requirements" for details. It is very important to use the current source with the RF amplifier. The current source incorporates an RF signal AGC. This ensures optimum operation of the device for high input signal levels.
28	IAGCOUT	Audio AGC Output Current	See Fig. 5. A current source controlled by the Audio signal level and the AGC threshold adjust (Pin 8). The current source is intended to sink current from an PIN diode on the RF input and hence reduce the RF signal incident on the RF amplifier input.

Application Circuit Requirements

The example application circuit is shown in Fig. 2. To achieve optimum performance of the device it is necessary to incorporate a Low Noise RF amplifier at the front end receiver. This is easily biased using the on–chip facilities provided.The receiver also requires a local oscillator input at the wanted channel frequency.

RF Amplifier and Local Oscillator Network

The design of the RF amplifier is simplified by the on–chip current source and the two voltage references VBG and VR.

A suitable circuit is shown in Fig. 3. The current through the load and hence the gain of the amplifier is controlled by the on chip current source IRF. This ensures that the gain of the amplifier is independent of the supply voltage. Also, as VR and VBG are independent of supply voltage it ensures that the bias points of the transistors are also stable and independent of supply voltage, with each transistor simply biased via a series resistor to the appropriate voltage reference.

The RF amplifier current source (Pin 27) may be adjusted with the use of an external resistor connected between Pin 2 and a voltage reference or ground. For details see "RF Amplifier Current Source Adjustment". Also the RF amplifier current source forms part of the RF AGC circuitry reducing the RF amplifier current if excessive signal is incident on the mixer inputs. It is very important to use the current source in the design of the RF amplifier. This ensures that the SL6609A will operate with high level input signals.

The differential input required by the mixers is applied from the RF amplifier via a suitable transformer (TI). This forms a tuned load with the variable capacitor (VC1). This load is tuned to the operating frequency of the device. The normal operating gain of the RF amplifier is also controlled by the load resistor (R13) in parallel with the transformer.

The input to the amplifier is an LC network (C26, L1 and C27) designed for optimum noise figure of the RF amplifier in order to give best overall device sensitivity.

For optimum sensitivity, adjacent channel and third order intermodulation performance refer to "Set–up for Optimum Performance" for the gain distribution requirements of the receiver chain.

The local oscillator signal is applied to the device in phase quadrature. This can be achieved with the use of two RC networks operating at their –3dB/45° transfer characteristic at the local oscillator frequency, giving a full 90° phase differential between the LO ports of the device. (see Fig. 4). Each LO port of the device also requires an equal level of drive from the oscillator. In this applications circuit the local oscillator is supplied by a signal generator with a source impedance of 50 Ohms hence the total RC network (including mixer bias) is designed to have this input impedance.

Note: All voltage and current sources used for bias of the RF amplifier and receiver mixers should be decoupled at RF and Audio frequencies using suitable capacitors. RF decoupling should be as close as possible to the RF circuit.

RF Amplifier to Mixer Transformerless Matching Circuit

An LC coupling network can be used to replace the transformer TI in the applications circuit. This couples the RF amplifier output to the SL6609A mixer inputs MIXA (Pin 26) and MIXB (Pin 24). The circuit is shown in Fig. 10.

Regulator Requirements

The on–chip regulator must be used in conjunction with a suitable PNP transistor to achieve reliable regulation. As the transistor forms part of the regulator feedback loop, the transistor should exhibit the following characteristics:

$$H_{FE} \geq 100 \text{ for } V_{CE} \geq 0.1V$$

A suitable transistor is specified in the application circuit.

RF and Audio decoupling Requirements

All voltages and references should be adequately decoupled at audio (baseband) frequencies. Also, where a voltage reference or current source is used to bias the RF or LO circuits it is necessary to apply RF decoupling to the supply at the point of connection.

Open Collector Outputs

The Data Output and the Battery Flag output are open collector and require a pull up resistor to a suitable voltage reference. Care must be taken to ensure that the pull–up resistor is adequate to supply sufficient current to the load.

CIRCUIT FACILITIES

Audio AGC Circuit

Fig. 5 shows the internal structure associated with the Audio AGC facility.

The Audio AGC facility consists of a current sink which is controlled by the audio (baseband) signal amplitude. It has three parameters that may be controlled by the user; the Attack (turn on) time, Decay (duration) time and threshold level.

Attack time

The Attack time is simply determined by the value of the external capacitor connected to Pin 9 (TCADJ). The external capacitor is in series with an internal 100k Ohm resistor and the time constant of this circuit dictates the attack time of the AGC.
i.e. $T_{ATTACK} \propto 100k * C_{TC}$. (*=multiplied by)

Decay Time

The decay time is determined by the external resistor R_{DECAY} connected in parallel to the capacitor C_{TC}. The Decay time is simply $T_{DECAY}=R_{DECAY}*C_{TC}$

Threshold level

When a large audio (baseband) signal is incident on the input to the AGC circuit (see Fig. 5) the variable current source is turned on. This causes a voltage drop across R16. The voltage potential between VR and the voltage on Pin 8 causes a current to flow from Pin 9. This charges up C_{TC} through the 100k internal resistor. As the voltage across the capacitor increases, current source 2 is turned on and this sinks current from Pin 28.

The current sink on Pin 28 can be used to drive the external AGC circuit by causing a pin diode to conduct, reducing the signal to the RF amplifier.

The relationship between the incident audio signal and current source 1 is shown in Fig. 8. This can be used in conjunction with the value of R16 to set the voltage at Pin 8 for any particular signal level.

The relationship between the voltage at Pin 8 and the output of current source 2 is given in Fig. 9.

Using both figures, the value of R16 can be selected to give the required output current at Pin 28 for any particular input signal level. Note, however, that the maximum Audio signal and hence the Audio AGC current (Pin 28) is limited in practice by a typical receiver gain distribution to approximately 45μA.

Disabling the Audio AGC Circuits

The audio AGC may be simply disabled by connecting Pin 8 (GTHADJ) to VR. Alternatively the audio AGC may be disabled by connecting Pin 28 (IAGCOUT) to Vcc2 and connecting Pin 9 (TCADJ) directly to VR (pin 6). This would then allow the use of the voltage drop across R16, when connected to Pin 8, to be used as a RSSI (Received Signal Strength Indicator).

R.F. Current Source Adjustment.

With Pin 2 open circuit and with Pin 27 connected to a potential of 0.2V (i.e. the emitter of a transistor with the base voltage V_b = 1V (i.e. VR)), the current is nominally set to give IRF=500μA.

The current source may be adjusted by connecting Pin 2 via a suitable resistor to a voltage reference or ground.

The value of the resistor is determined by the required increase or decrease in IRF from the nominal 500μA. (i.e. Pin 2 Open Circuit).

The nominal voltage of Pin 2 is 0.7V.

To decrease IRF, connect Pin 2 to ground using a resistor R where;

$$R = \frac{0.7V}{\left(\frac{500\mu A - I_{req}}{5}\right)}$$

I_{req} = Required IRF

To increase IRF connect Pin 2 to a voltage reference (e.g VBG) using a resistor R where;

$$R = \frac{V^* - 0.7V}{\left(\frac{I_{req} - 500\mu A}{5}\right)}$$

I_{req} = Required IRF

V*=Voltage reference used.

Notes

i) VBG should not be used to sink current

ii) The on–chip voltage Reference VR should not be used as a reference for Pin 2 as it is not capable of sourcing the required current.

On Chip Voltage References.

The on–chip voltage reference VBG (1.2V) may be used to bias an external RF amplifier and as a reference for the on–chip RF AGC (see Pin 2). VBG can source a maximum current as specified in the device Data Sheet. VBG should not be used to sink current.

The on–chip voltage reference VR (1.0V) may be used to bias an external RF amplifier and as a reference for Pins 1,7, 8 and 9. VR can source or sink a maximum current as specified in the device Data Sheet.

Battery Flag Input

The battery flag threshold may be simply increased by using a suitable potential divider so that at the required battery threshold voltage, the voltage at Pin 20 (VBATT) is 1V.

Set–up for Optimum Performance

To obtain optimum receiver sensitivity it is necessary to have a Low Noise RF Amplifier at the front end of the receiver (see "RF Amplifier and Local Oscillator Network"). However to achieve optimum Third Order Intermodulation rejection it is essential to ensure that the amplifier gain is not greater than the value necessary to achieve good sensitivity. Similarly to achieve optimum Adjacent Channel rejection it is necessary to limit the internal gain of the device to that required to obtain sensitivity. Increasing the internal or the RF Amplifier gain beyond these points will degrade the receiver performance.

The procedure outlined here represents a method of obtaining optimum performance under the following operating conditions:

Frequency of Operation	282MHz
Deviation Frequency	4kHz
Local Oscillator Input Power	–15dBm (50Ohm source impedance, see Fig. 4)
Power Supply Vcc1	1.3V
Power Supply Vcc2	2.7V
Nominal Gyrator Pin 4	100kOhm
R1	Open Circuit
R8	Open Circuit
C1–C7	1nF

If the proposed frequency of operation is different to that stated above, the signal levels stated should be used as a guide to obtaining the optimum gain distribution within the receiver and RF amplifier.

Note: The following set up procedure was undertaken using the RF Amplifier specified in Fig. 2 and should only be used as guidance if alternative RF amplifiers are proposed.

Note: Having obtained the component values for optimum performance for a specified RF amplifier, circuit layout, and operating conditions then provided the RF amplifier design is not device dependent, it should not be necessary to undertake the set–up procedure for each individual circuit.

Please note that the local oscillator drive level and receiver gain used can be optimised if required by the user to trade off sensitivity with the receiver interferer performance (ie IP3). The receiver gain level specified below is considered by GPS to achieve a good balance between sensitivity and receiver interferer performance.

Sensitivity can be increased, to the detriment of receiver interferer performance, by increasing the LNA gain. Fig 11 and Fig.12 show typical trends.

Increasing the local oscillator drive level, whilst reducing the LNA gain to keep the same gain to the receiver test points (TPX and TPY) can be used to increase the receiver interferer performance whilst maintaining a near constant sensitivity level. This is typically true for local oscillator signals in the range 10mVrms to 50mVrms as measured at the receiver local oscillator inputs pins LOX and LOY.

Set – up procedure

If the Audio AGC function of the SL6609A is being used in a particular application it must be disabled before undertaking the following steps. To disable the Audio AGC function connect pin GTHADJ directly to pin VR, leaving all existing circuitry connected to pins GTHADJ and VR connected.

a) Apply a signal with a frequency of LO + 4kHz, –73dBm, with no modulation on, to the input of the RF amplifier.

b) Monitor test point TPX (pin 1) with an oscilloscope. Determine that the signal is at a frequency of 4kHz. Adjust LO or RF frequency to achieve this. Adjust VC1 on the RF amplifier load until the 4kHz signal level is maximum. (This should be >200mV pk–pk).

Note: If the level of the signal is above 260mV pk–pk the signal will not be sinusoidal due to the saturation of the receiver.

c) Use the parallel load resistor (R13) on the RF amplifier to reduce the gain of the RF amplifier to obtain a level of 160mV ±10mV pk–pk at TPX. Ensure that the signal at TPY (Pin 7) is also at a level within 10mV of that at TPX (Pin 1).

R13 will typically be:–
1k2 for 153MHz
1k8 for 282MHz
3k9 for 470MHz

d) Apply a capacitor between Pin 16 and GND in accordance with the following table

Data Rate	Capacitor required
512	2nF
1200	1nF
2400	470pF

Fine adjustment of the Gyrator Filter

Due to the tolerance of the manufacturing process the gyrator response may vary by ±15% for a given value of resistor connected between Pin 4 and GND. For accurate alignment the filter will require adjustment. This is simply achieved by undertaking the following procedure:

Note: For the following levels to apply the procedure below should follow "Set–up for Optimum Performance".

a) Set the input RF frequency to LO+4kHz, (No Modulation).

b) Monitor the signal at the test point TPX (Pin 1). Check that the signal frequency is 4kHz. Adjust the LO or RF frequency to obtain this. Adjust the RF signal input level until a signal of 40mV pk–pk is measured.

c) Monitor the test point TPLIMX (Pin 15) and note the pk–pk signal level (this should be approximately 170mV pk–pk but not limiting).

d) Adjust the RF signal generator frequency until the signal level drops to 70.8% (–3dBs) of the level noted in step c.

e) Note the frequency of the RF signal generator. The difference between the LO frequency and the RF input frequency represents the –3dB response of the filter.

Using a 100k Ohm resistor to set the Gyrator filters will give a nominal –3dB cut of 7.5kHz. Changing this resistor value causes a linear change in the frequency of the filter cutoff. For example, if a 100k Ohm resistor results in a filter –3dB cut off equal to 7.5kHz then a 136k Ohm resistor will give a 5.5kHz –3dB cut off.

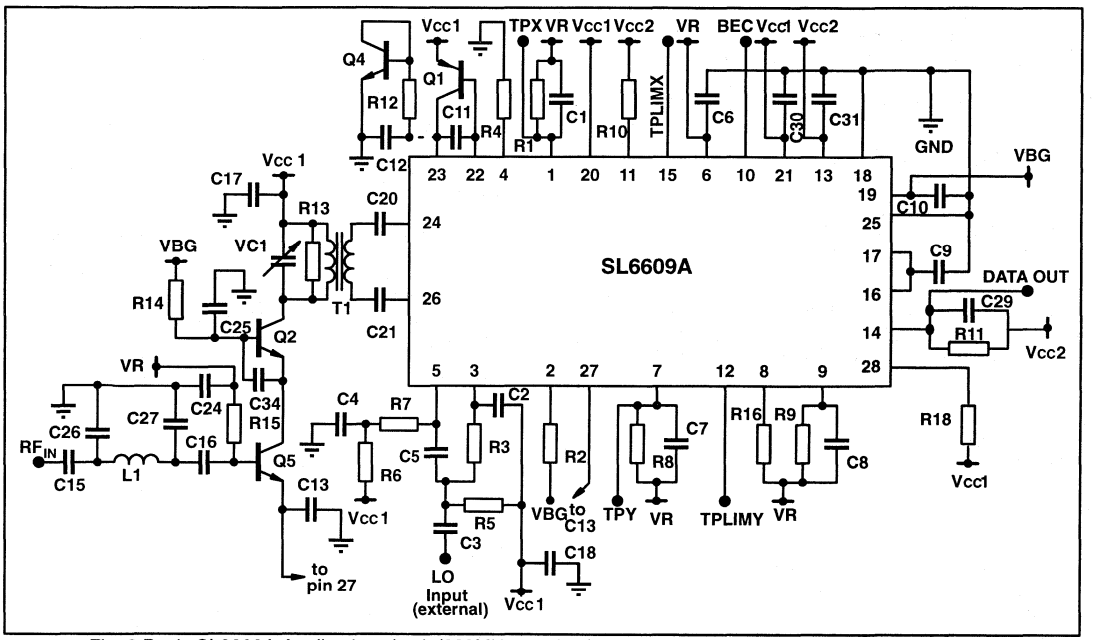


Fig. 2 Basic SL6609A Application circuit (282MHz receiver), showing RF amplifier with external injected LO (no Audio AGC)

Component Values (for general demonstration circuit (282MHz))

Resistors		Capacitors				Inductors	
R1	open circuit	C1	1n	C19	not used	L1	68n (4) (6)
R2	open circuit	C2	5p6(6)	C20	1n	T1	1:1 30nH transformer
R3	100	C3	1n	C21	1n	e.g Coilcraft M1686–A	
R4	100k	C4	1n	C22	not used		
R5	100	C5	5p6(6)	C23	not used		
R6	100	C6	2µ2	C24	1n		
R7	100	C7	1n	C25	1n	Active Components	
R8	open circuit	C8	100n	C26	6p8 (4) (6)		
R9	220k	C9	2n(2)	C27	open circuit (4) (6)	Q1	Zetex FMMT58
R10	1M	C10	2µ2	C28	not used	Q2	Toshiba 2SC5065
R11	100k(5)	C11	100n	C29	100p	Q3	Not Used
R12	330(3)	C12	1n	C30	2µ2	Q4	Philips BFT25A(3)
R13	see note (1)	C13	1n	C31	2µ2	Q5	Toshiba 2SC5065
R14	4k7	C14	not used	C34	2p2		
R15	4k7	C15	1n	VC1	1–10p		
R16	33k	C16	1n				
R17	not used	C17	1n				
R18	12k	C18	1n				

Note:
The full list of Audio AGC components are not included here.

NOTES

(1) The value of this component is determined by the set up procedure. See "Set up for Optimum Performance".

(2) The value of C9 is determined by the output data rate. Use 2nF for 512bps, 1nF for 1200bps and 470pF for 2400bps.

(3) R12 and Q4 form a dummy load for the regulator. Permitted load currents for the regulator are 250µA to 3mA

(4) L1, and C26 form the low noise matching network for the RF amplifier. The values given are for the RF amplifier specified in the Applications Circuit with no Audio AGC connected. If the Audio AGC circuitry is connected the values will require a small change to achieve a good match.

(5) The value of R11 is dependent on the data output load. R11 should allow sufficient current to drive the data output load.

(6) The values of these components are dependent on the frequency of operation.

(7) Values for R16, R9, C8 and R18 are included so that the open loop action of the audio AGC circuitry can be observed. If this is not required it can be disabled as described in the section "Disabling the audio AGC Circuits.

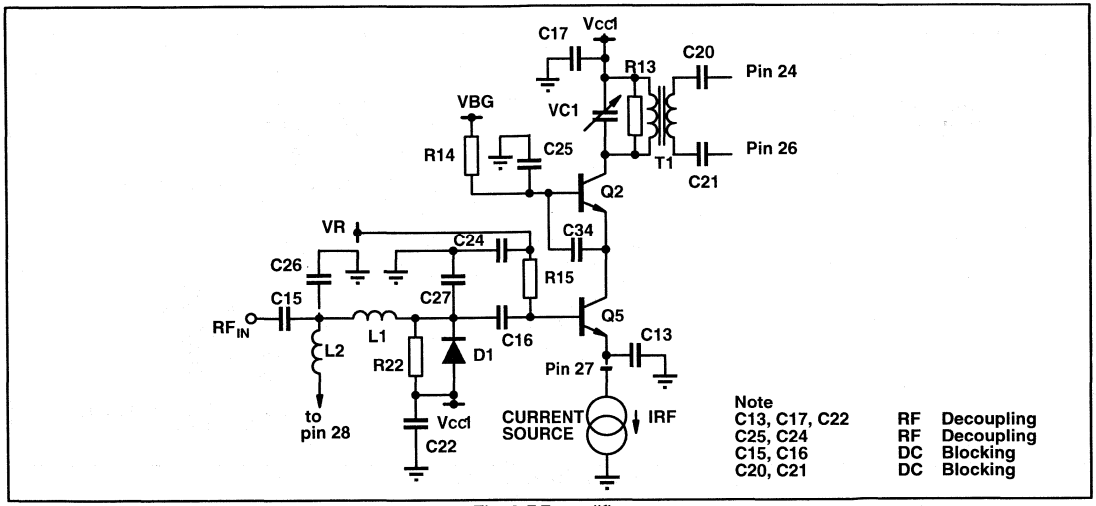


Fig. 3 RF amplifier

RF Amplifier Component Values

Resistors		Capacitors		
R14, R15	4k7	C13, C15	1nF	Active components
R13	see note 1	C16, C17	1nF	D1 MA862 (Panasonic)
R22	47k	C20, C21	1nF see note 2	
		C24, C25	1nF	
		L2	820nH	

Notes:
(1) The value of R13 is determined by the set up procedure (See "Set up for optimum performance").

(2) C20 and C21 are purely for demonstration purposes. Pin 24 and Pin 26 may be DC coupled provided that no DC voltage is applied to the mixer inputs.

Frequency Dependent Components

	153MHz	280MHz	450MHz
C26	not used	6.8p	not used
C27	not used	not used	not used
L1	150nH	68nH	39nH
C34	3p3	2p2	1p5
T1	100nH	30nH	16nH
	Coilcraft N2261–A	Coilcraft M1686–A	Coilcraft Q4123–A
VC1	1–10pF	1–10pF	1–3pF
Q4, Q5	Toshiba 2SC5065	Toshiba 2SC5065	Philips BFT25A
(See also LO drive Network)			

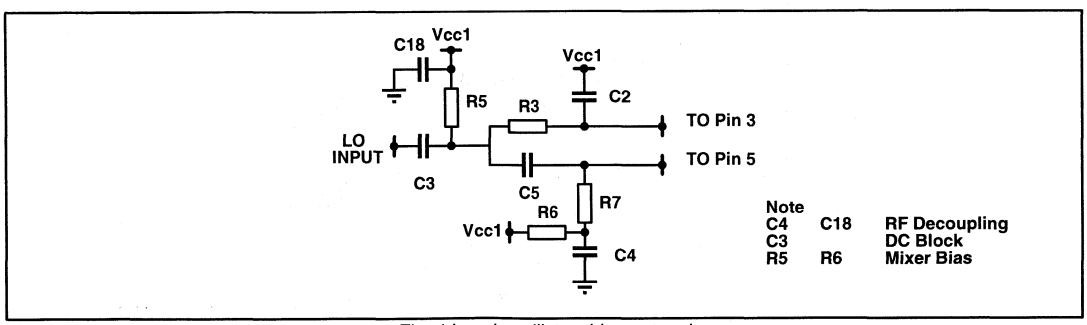


Fig. 4 Local oscillator drive network

LO Drive Network Component Values

50Ohm input impedance (External LO injection)

	153MHz	280MHz	450MHz
C2	10p	5p6	3p3
C5	10p	5p6	3p9

C3, C4, C18 = 1n
R3, R5, R6, R7 = 100Ohms.

Higher Input Impedance (crystal oscillator input)

	153MHz	280MHz	450MHz
C3	Set by load allowable on crystal oscillator (typical 4p7)		
C2	10p	5p6	3p3
C5	10p	5p6	3p9
R3	100	100	100
R7	100	100	100

R5, R6, = 1k
C4, C18 = 1n

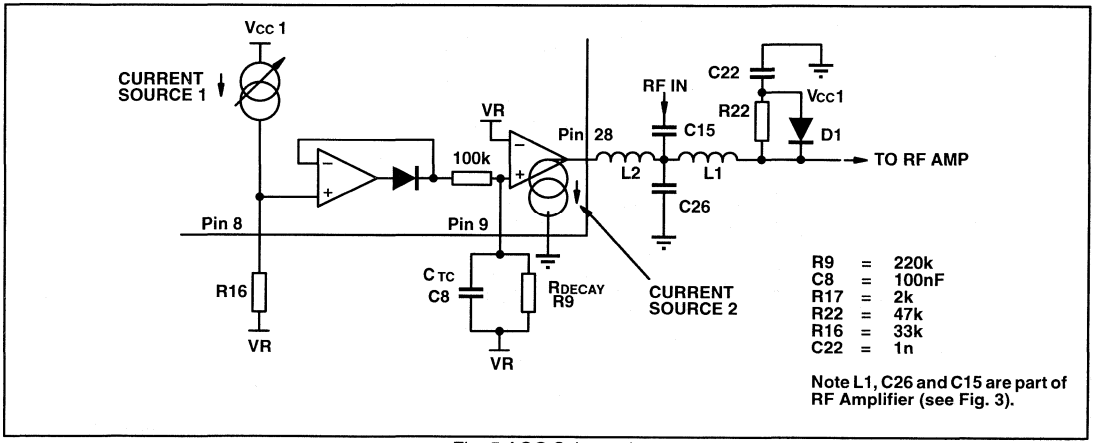


Fig. 5 AGC Schematic

AGC Components Values (282MHz RF amplifier)

R9	220K	C15	1n	L1	47n
R15	4k7	C16	1n	L2	820n
R16	see note	C26	4p7		
R22	47k	C8	see note		
		C30	1n	D1	MA862 (Panasonic)

Notes:

(1) R16 sets the gain (sensitivity) of the audio AGC. If R16 is increased then the audio AGC will become active for a lower wanted signal level. Increasing R16 can cause the Audio AGC loop to become unstable. C8 should be increased to increase the turn on/off time to prevent oscillation occuring.

Fig. 6 shows a typical response of the AGC with wanted and unwanted rejection level.

If the AGC is required to become active earlier it is possible to use the circuit shown in Fig. 7 to replace R16. However, it should be noted that the AGC has a fixed dynamic range.

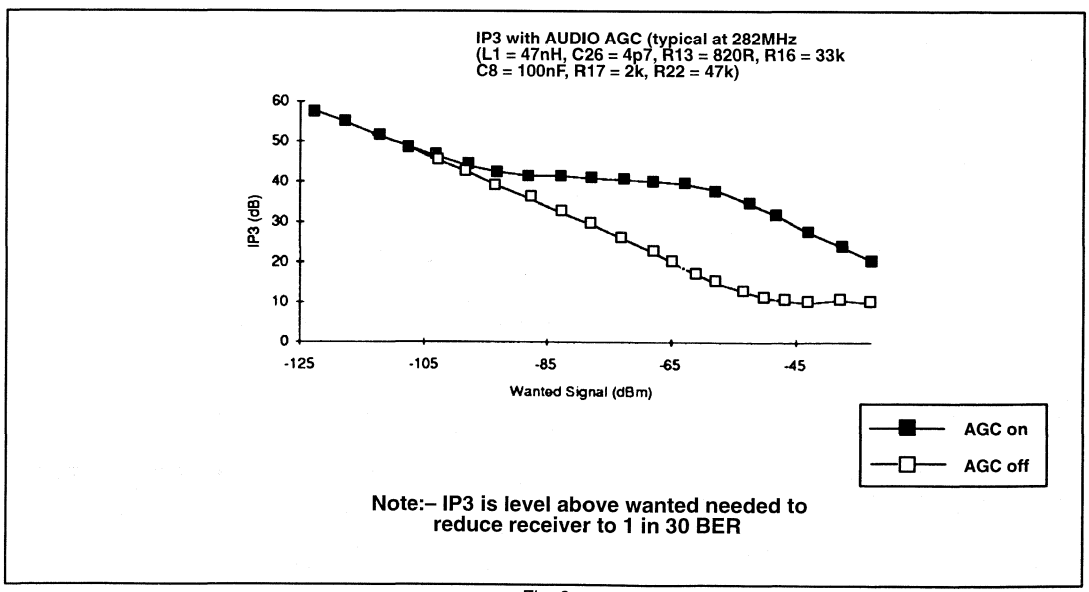


Fig. 6.

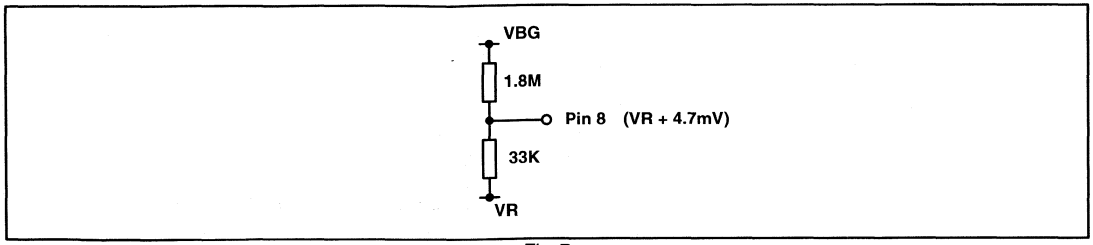


Fig. 7.

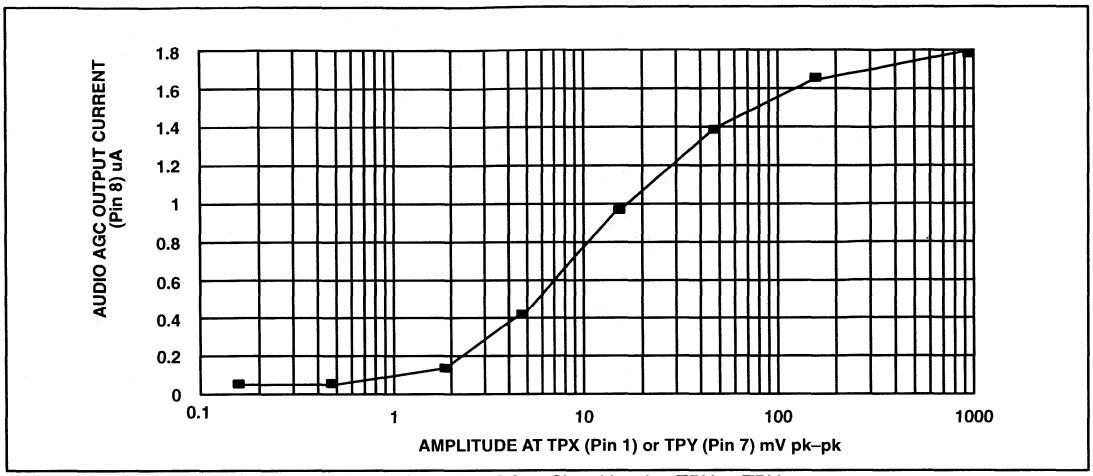


Fig. 8 RSSI Audio AGC vs Signal level at TPX or TPY

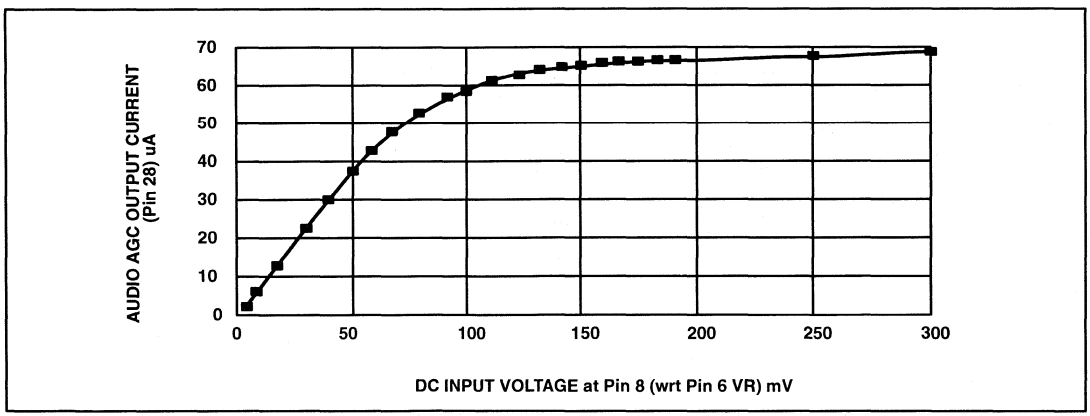


Fig.9 Audio Output Current at Pin 28 vs DC Voltage at Pin 8 (GTHADJ)

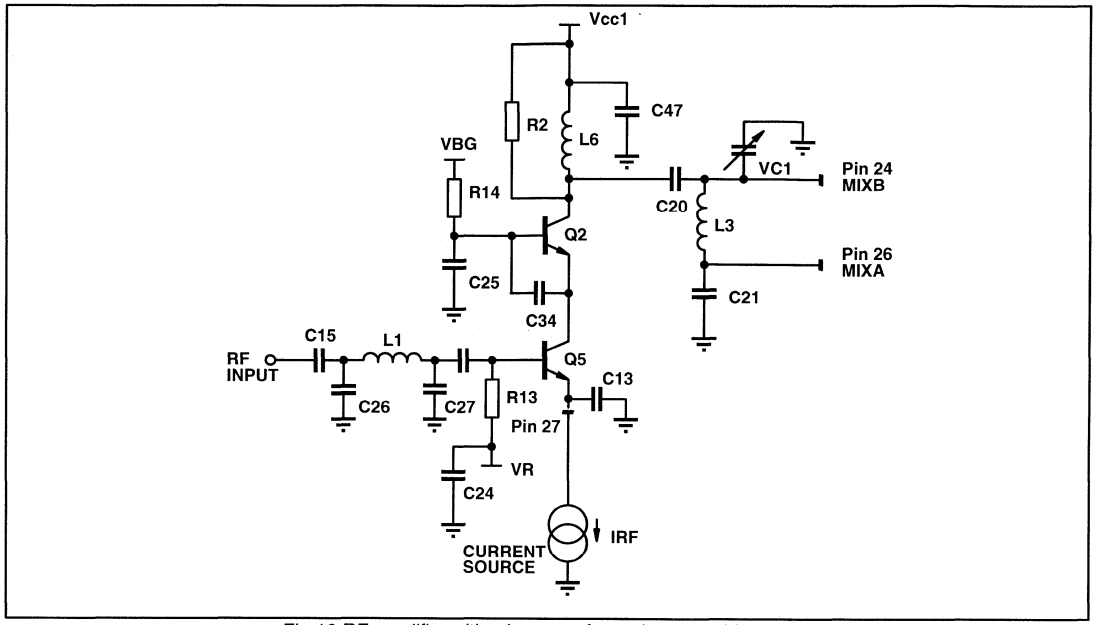


Fig.10 RF amplifier with mixer transformerless matching circuit

RF Amplifier Component Values

Resistors		Capacitors		Transistors
R13, R14	4k7	C13, C15	1nF	Q2, Q5 Toshiba 2SC5065 see note 2.
R2	see note 1	C16	1nF	
		C24, C25	1nF	

Notes
(1) The value of R2 is determined by the set up procedure (See "Set up for Optimum Performance")
(2) Q2, Q5 BFT25A for 470MHz

Frequency Dependant Components

	153MHz	**282MHz**	**470MHZ**
C26	not used	6p8	not used
L1	150nH	68nH	39nH
C27	not used	not used	not used
C34	3p3	2p2	1p5
L6	150nH	82nH	47nH
VC1	1 –10pF	1 – 5pF	not used
L3	330nH	100nH	39nH
C21	2p7	3p3	10p
C20	1nF	1nF	1 – 5pF

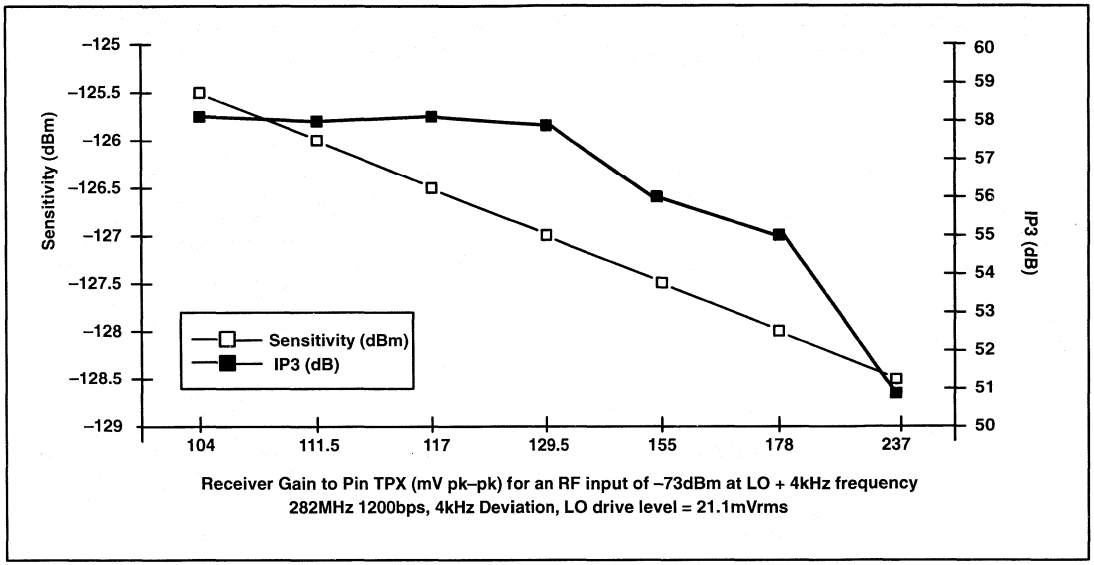


Fig. 11 Sensitivity, IP3 vs Receiver Gain

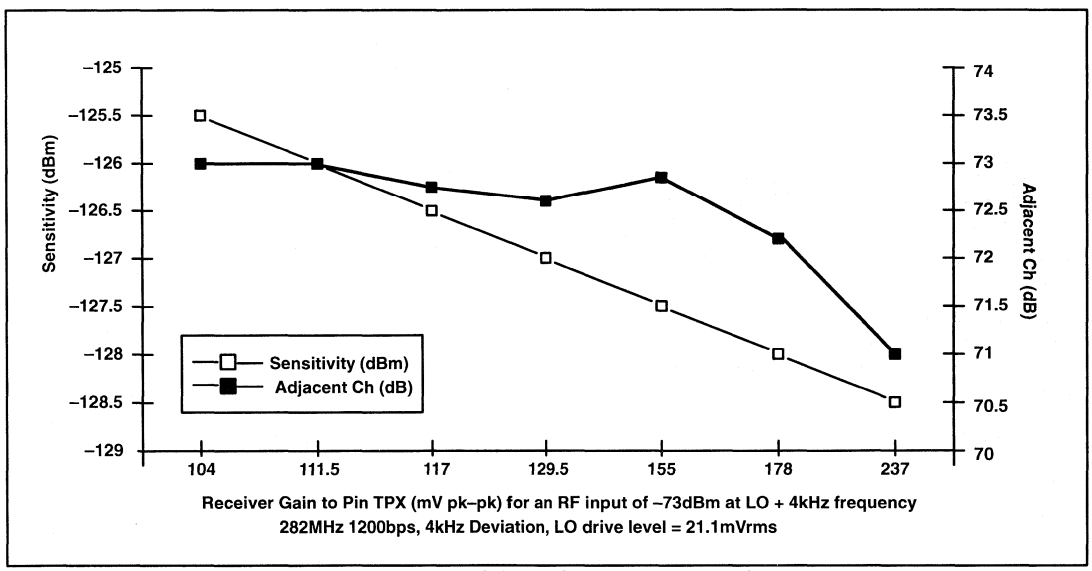


Fig. 12 Sensitivity, Adjacent Channel vs Receiver Gain

USER GUIDELINES TO OBTAIN OPTIMUM PERFORMANCE WITH AN SL6609A PAGING RECEIVER INTEGRATED CIRCUIT

INTRODUCTION

This application note describes a set-up check list which should be used to ensure that the optimum performance is being obtained from the SL6609A in a given application. Potential practical performance limiting factors are described, with suggestions on how they can be overcome so that they do not limit the SL6609A performance.

Mention is also made of how to trade off receiver sensitivity performance with receiver interferer performance (i.e. IP3).

Details of an SL6609A receiver board developed by GPS to work with a standard pager digital board design are included to illustrate the recommendations given.

SL6609A Set-up Check List

This section is a procedure to follow to ensure that optimum performance is achieved with the SL6609A. It is assumed that the measurements will be carried out under the following conditions:

a) Vcc1 = 1.3V
b) Vcc2 = 2.7V
c) Temperature = room temperature

Other operating conditions will slightly alter the expected measured values specified below.

Please note that the local oscillator drive level and receiver gain can be optimised by the user to trade off sensitivity with receiver interferer performance (i.e. IP3), please see Fig. 1a and Fig. 1b. Sensitivity can be increased, to the detriment of receiver interferer performance, by increasing the LNA gain. The receiver gain level specified below is considered by GPS to achieve a good balance between sensitivity and receiver interferer performance.

Increasing the local oscillator drive level, whilst reducing the LNA gain (to keep the same overall gain to the receiver test points TPX and TPY) can be used to increase the receiver interferer performance whilst maintaining a near constant sensitivity level. This is typically true for local oscillator signals in the range 10mVrms to 50mVrms as measured at the receiver local oscillator input pins LOX and LOY.

1. Local Oscillator (LO) Drive Level

a) Check that the LO frequency is the same as the intended carrier frequency.

b) The amplitude level at the device pins LOX and LOY should be measured as follows:

The levels can be measured with a high impedance RF FET probe, with an adjustment made for the FET probe loading. It has been assumed here that the RF FET probe will be used with a spectrum analyser that will display the measured voltage in dBm, assuming a 50ohm impedance level. This will not be the actual LO drive level power to the SL6609A as the impedance at the pins LOX and LOY is not 50ohm. For example to measure the level at the pin LOX:

i) Apply an RF input signal at -73dBm, at a deviation frequency offset from the local oscillator frequency. If the SL6609A audio AGC circuitry is used in the application, it must be disabled by directly connecting pin GTHADJ to pin VR, leaving all existing circuitry connected to pins GTHADJ and VR connected.

ii) With a scope probe, measure the signal level at the pin TPX, call this level TPX1.

iii) With a high impedance FET probe measure the level at the pin LOX. Note the new level at pin TPX, call this level TPX2.

iv) LO drive level(V) =

FET probe measurement(V) * [TPX1(V) / TPX2(V)]
making appropriate conversions for units.

worked example:

FET probe LOX measurement = -21.9dBm (50ohm system)
TPX1 = 116mVpp
TPX2 = 102mVpp
Actual LOX level = -21.9dBm + 20 log (116/102)
= -20.78dBm (50ohm system)
= 20.44mVrms

The LO drive level correction procedure for FET probe loading, described above, assumes that the SL6609A LO inputs are still being driven in their linear region, i.e. a 1dB increase in LO drive level producing a 1dB increase in receiver gain. This assumption is valid up to LO drive levels of around 25mVrms at the pins LOX and LOY.

For an external LO drive at 150MHz the following are typical measured levels with the passive RC quadrature network (shown in Fig. 2):

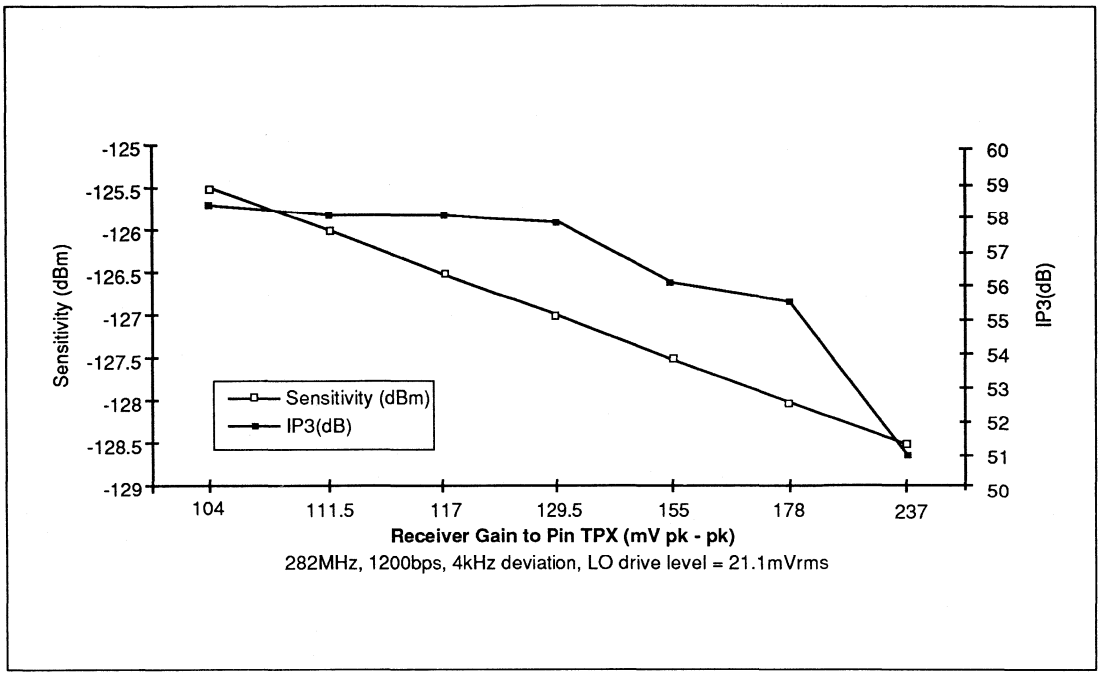


Fig.1a: Sensitivity, IP3 vs receiver gain

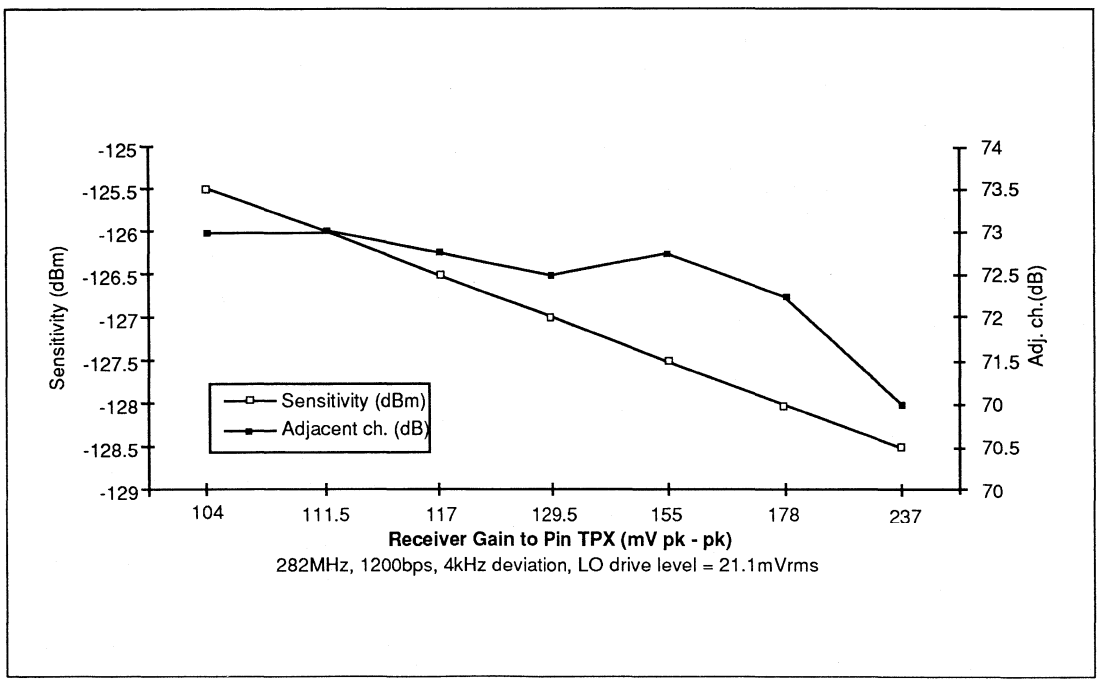


Fig.1b: Sensitivity, adjacent channel vs receiver gain

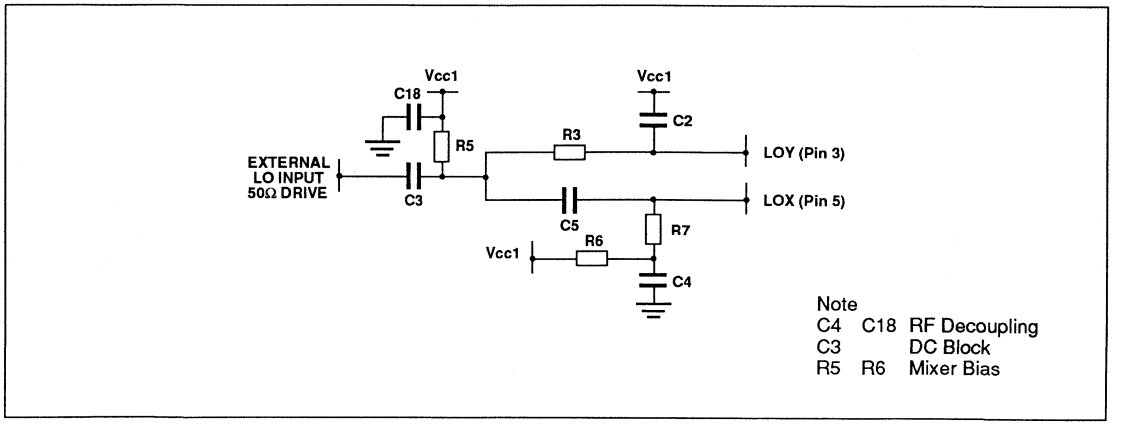


Fig.2: Local oscillator drive network

External LO DriveLevel at device pin LOX or LOY

-15dBm 23.4mVrms ±1dB = -19.6dBm ±1dB (50ohm system)
-18dBm 16.6mVrms ±1dB = -22.6dBm ±1dB (50ohm system)
-20dBm 13.2mVrms ±1dB = -24.6dBm ±1dB (50ohm system)

For an external LO drive at 282MHz the following are typical levels with the passive RC quadrature network (shown in Fig. 2):

External LO DriveLevel at device pin LOX or LOY

-15dBm 21.1mVrms ±1dB = -20.5dBm ±1dB (50ohm system)
-18dBm 14.9mVrms ±1dB = -23.5dBm ±1dB (50ohm system)
-20dBm 11.9mVrms ±1dB = -25.5dBm ±1dB (50ohm system)

2.SL6609A Gain

If the audio AGC function of the SL6609A is used in a given application circuit, this must be disabled before undertaking the gain measurement described in this section. To disable the audio AGC action connect pin GTHADJ directly to pin VR, leaving all existing circuitry connected to pins GTHADJ and VR connected.

a) Match the receiver RF input to 50ohm.

b) At the receiver RF input, apply a signal at the RF carrier frequency plus a deviation frequency offset, at a level of -73dBm.

c) Using a 10:1 scope probe measure the levels at pins TPX and TPY. These levels should be 160mVpp ±10mV. The difference in levels between the signals at TPX and TPY should be less than 10%, and they should be in quadrature to within an accuracy of 10%. They should also be sinewaves at the same frequency as the RF input deviation frequency.

3. SL6609A Signal To Noise Ratio

Please note, when reading this section that if the receiver gain has been set higher or lower than the specified value in Section 2, then the measured values of signal and noise at the pins TPLIMX and TPLIMY will need to be adjusted accordingly.

a) Match the receiver RF input to 50ohm.

b) At the receiver RF input apply a signal at the RF carrier frequency plus the deviation frequency, and at a level of -99dBm.

c) With a 10:1 scope probe measure the gain at pins TPLIMX and TPLIMY. The amplitude measured should be 60mVpp ±10mV. The difference in levels between the signals at TPLIMX and TPLIMY should be less than 10%, they should be in quadrature, and they should be sinewaves at the same frequency as the RF input deviation frequency offset.

d) Turn off the RF signal generator connected to the receiver RF input, ensuring that the receiver RF input is still terminated in 50ohm.

e) Using a 1:1 scope probe measure the amplitude of the noise at the pins TPLIMX and TPLIMY. If the gain has been set to the level specified in Section 2 the maximum noise level should be 3mVpp. Note that this must be a measurement of the absolute peaks of the waveforms.

Optimum sensitivity will not be achievable if the noise exceeds the expected value. See the section on "Possible Noise Problems" to try to reduce this noise level to the correct level.

f) The receiver's RF input should now be connected and matched to an antenna and placed in a TEM cell.

Assuming that the gain of the antenna in the chosen TEM cell is known, it will be possible to calculate the TEM cell RF input level that is equivalent to the -99dBm signal applied in step b). Apply this level and check that the same level is observed at the test points as in step c). Note that extreme care has to be taken to ensure that any connections made to the circuitry in the TEM cell have a minimum affect. If the signal level is not correct, it is likely that the antenna is not correctly matched to the receiver RF input, or that the LNA is oscillating (or is close to oscillation) via the antenna.

g) Ensure that the receiver's RF input is still connected and matched to an antenna. Place the receiver in a TEM cell. Switch the TEM cell RF signal input off, and repeat step e), measuring the noise at pins TPLIMX and TPLIMY. If the noise level is too high it is likely that the excess noise is being picked up by the antenna. See the section on "Possible Noise Problems" to try to reduce this noise level to the correct level.

POSSIBLE NOISE PROBLEMS

Due to the very low RF signal levels that a paging receiver is required to work with, great care has to be taken to minimise noise added to the received signal. The SL6609A has been designed to be a very low noise device, but care has to be taken to ensure that the pcb layout and external circuitry does not become the major noise source. Typical noise degradation mechanisms are:

1. Power Supply Noise
2. Digital Noise Pickup
3. Local Oscillator Re-radiation
4. LNA Oscillation

These mechanisms are now described in detail:

1. Power Supply Noise.

The SL6609A is a direct conversion receiver and so the RF signal is down-converted to baseband when still at a low amplitude. Excess noise on the power supply lines can degrade the receiver signal to noise ratio. Noise in the frequency range 500Hz to 25kHz should be minimised. This can be achieved by:

- Careful supply de-coupling. RC low pass power supply filters are recommended.
- Careful choice of voltage doubler/regulator to supply Vcc2. Supply filtering can be most effectively achieved if all frequency components of the voltage doubler lie outside the frequency range 500Hz to 25kHz.
  Two voltage doubler circuits that have been used with the SL6609A are shown in Fig. 3. It is good practice to use a two board design if possible, one for the RF circuitry and one for the digital circuitry. It is preferable to place the voltage doubler/regulator circuitry on the digital board.
- Careful pcb grounding. A continuous ground-plane for good RF performance is strongly advised. Care should be taken with signal and power supply grounding. Power supply de-coupling should be placed as close to the SL6609A as possible. RF de-coupling capacitors should be placed as close as possible to the appropriate RF circuit nodes.

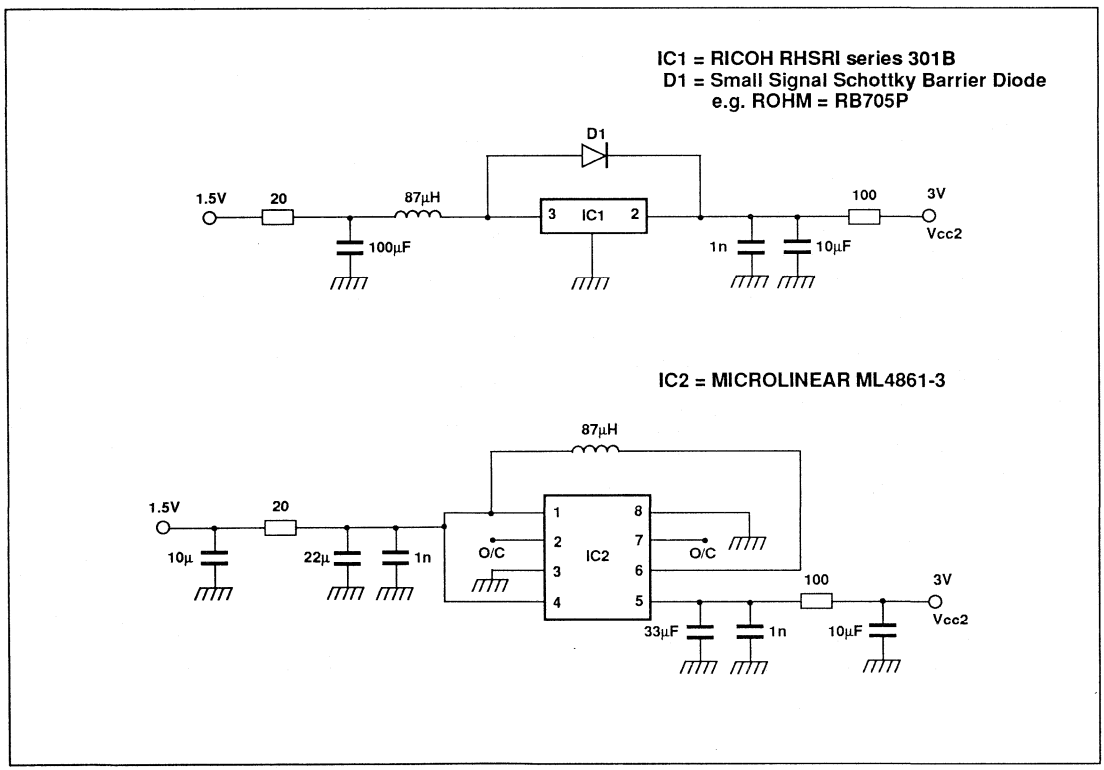


Fig.3: Suggested voltage doubler circuits

- Antenna grounds should be joined at one point to the ground plane. The ground plane should not run underneath the antenna.
- It is important that where possible the appropriate RF de-coupling capacitors within the LNA circuitry that are creating a local RF short (e.g. capacitor pair: C17 and VC3) (see Fig. 5) are connected to the RF ground plane by a common via hole.

2. Digital Noise Pickup.

Due to the low RF signal levels that the SL6609A is required to receive, noise generated at the RF frequency by harmonics of digital signals can degrade the receiver's performance by coupling in the LNA circuitry directly or via the antenna. Particular care should taken with the SL6609A data output pin (Pin 14 DATA O/P). This problem can be minimised by:

- Using a good continuous RF ground plane.
- Careful pcb layout, ensuring that digital signal pins and track routing are kept away from the sensitive receiver RF front end components and the antenna.
- Using low pass filters (e.g. a capacitor) to reduce the level of the higher harmonics on digital tracks.
- The digital decoder and display driver circuits can also generate harmonics that are at the same frequency as the RF frequency. To minimise their affect it is preferable to have these components mounted on a separate board from the antenna, LNA, SL6609A and LO circuitry. It is also good practice to have as much of the digital circuitry inactive during the RF paging message reception period. An example would be to delay writing to the LCD display until after the end of the RF paging message reception.
- Incorporating good RF decoupling on the digital board power supplies and data tracks.

3. Local Oscillator Re-Radiation.

As the SL6609A is a direct conversion receiver the local oscillator frequency is the same as the incoming RF frequency. The receiver antenna is therefore tuned to the local oscillator frequency and can easily pick up the local oscillator signal feeding it into the receiver's RF input. This signal will then be mixed in the SL6609A with the local oscillator signal applied directly to the SL6609A local oscillator ports, LOX and LOY. If the local oscillator pickup at the RF receiver input is too large, the sensitivity of the receiver will be de-graded. Both the phase and amplitude of the local oscillator picked-up at the RF input will affect the level of receiver degradation. With worst case phasing the level of local oscillator signal picked up at the LNA input must be kept below -70dBm (as measured using a high impedance RF FET probe), if the receiver performance is to be unaffected. To minimise local oscillator pickup at the receiver RF inputs the following guidelines should be followed:

- Use a good continuous RF ground plane.
- Position the local oscillator circuitry away from the antenna and the LNA circuitry.
- Keep the local oscillator circuitry on the pcb as compact as possible and minimise the lengths of the tracks connecting the local oscillator output to the receiver local oscillator inputs (LOX and LOY).
- Place a good RF screen over the local oscillator circuitry.
- Ensure that there is no AM modulation on the local oscillator caused by power supply noise. This can be effectively achieved by powering the local oscillator circuitry using the 1V regulator function provided on the SL6609A (pins VREG, REGCNT with an external PNP transistor) and effective RF power supply decoupling. Particular care should be taken that decoupling is made to the appropriate AC ground, e.g. Vcc1, GND or Vref.

4. LNA Oscillation.

Careful circuit design and layout is required to ensure that this is not a problem. Two main forms of oscillation can occur:

- Oscillation of the LNA near the upper frequency limit of the LNA transistors. This frequency is typically in the region of 1GHz to 5GHz, much higher than the received RF signal frequency. One cause of this is inadequate RF de-coupling, or too much circuit gain near the transistor upper frequency limit. The latter can usually be cured by adding a small capacitor to the LNA circuitry to reduce the gain near the upper frequency of the LNA transistor. This type of oscillation can be checked for by observing the SL6609A mixer inputs with a spectrum analyser that is capable of observing the 1 to 5GHz frequency range.
- Oscillation of the LNA at the RF input frequency. This can occur both with the RF receiver input connected to a 50ohm input and when an antenna is connected. If oscillation of the LNA, with the RF receiver input connected to a 50ohm input is suspected, it can usually be confirmed by checking the input match with a network analyser. If a good 50ohm match cannot be achieved it is likely that the LNA is oscillating or very close to oscillating.

If good RF receiver performance and a good RF input match are obtained when the receiver RF input is connected to a 50ohm input, but sensitivity with an antenna is slightly below that expected, it is possible that the LNA is oscillating, or very close to oscillating, through a feedback loop via the antenna. This is possible because the antenna and LNA output load circuitry are tuned to the RF input frequency. To minimise the chance of this occurring the LNA output circuitry should be placed as far as is practically possible away from the antenna. Clues that the LNA is oscillating via the antenna are:

- The receiver large signal interferer measurements (i.e. IP3) with an antenna connected are significantly worse (>2dB) than the same measurement carried out with the receiver RF input matched to a 50ohm signal generator.
- The expected gain to the test points TPX and TPY in the TEM cell is significantly different (usually higher) than that expected from the same gain measurement with the receiver RF input matched to a 50ohm signal generator input.

ANTENNA ISSUES

The choice of Antenna size and shape will be largely dependent on the decoder board used and the Pager case size. The GPS RF demonstration board employs a 1mm diameter double loop antenna, the size and shape being determined by the chosen decoder board and case (See Fig.8).

Antenna gain increases with larger enclosed loop area and/or frequency of operation. Hence, using a physically larger antenna for the same frequency or, the same antenna at a higher frequency should result in an improved TEM Cell Sensitivity. This assumes that the Terminal Sensitivity remains constant and that the TEM Cell Sensitivity does not become limited by an antenna noise pick-up problem (e.g. LO reradiation or Data O/P spikes). If such a noise problem exists then increasing the antenna loop area will make no difference to the TEM Cell Sensitivity, because the Signal/Noise Ratio remains the same (i.e more signal and noise are picked-up by the antenna).

Any losses due to Low-Q components in the antenna matching network will result in a direct loss in TEM Cell Sensitivity. Try to use only capacitors in the antenna to LNA matching network.

The antenna gain is also very dependant on the loop resistive loss, and at RF this resistance is dominated by skin effects. It is therefore important that the antenna is made from, or coated with, a low resistivity metal. (e.g. silver).

Antenna gain can be measured with reasonable accuracy by tuning the antenna matching circuit in to 50 ohms and measuring the power output with the antenna mounted on the pager board and in the TEM Cell. The antenna gain is the TEM Cell input power minus the antenna output power. For the GPS dual-loop antenna board, this gain is approximately -39dB in the Elena ETC150F TEM Cell. With this antenna power matched to the LNA (with no losses) a board with a terminal sensitivity of -128dBm should attain a TEM Cell Sensitivity of -89dBm assuming there are no additional noise problems introduced.

AUDIO AGC PROBLEMS

If the loop gain of the Audio AGC circuit is made too great it is liable to break into oscillation at certain input signal levels.

This usually occurs just as the PIN diode turns on, typically about 30dB above the sensitivity level. An oscillation of around 400Hz will be visible at the test points TPLIMX and TPLIMY. The loop gain can be decreased by reducing the value of R8 in Fig. 4. Note that R20 in Fig. 4 "softens" the turn on of D1.

GPS RF DEMONSTRATION BOARD

Fig. 4 shows the circuit diagram and Figs. 5, 6 and 7 show the 3 layer pcb layout. The performance that this board typically achieves when connected to a digital board of a standard pager design, measured in an Elena ETC150F TEM cell system is described below. It should be noted that the Elena ETC150F TEM cell system has a 20dB attenuator connected to the TEM cell input. The TEM cell power inputs quoted below are the values before the 20dB attenuator, so that the level applied to the actual TEM cell is 20dB lower.

Frequency	150MHz
Frequency deviation	4.0kHz
Data Rate	1200bps
Sensitivity	8μV/m (body effect uncorrected)
Sensitivity	4μV/m (6dB body effect correction applied)
	-89dBm (TEM Cell Drive)
IP3	57dB
Adjacent Channel	73dB
IP2	48dB

The drive level at the local oscillator input pins LOX and LOY was 20mVrms.

A level of 70mVpp (measured at TPLIMX) was observed for a TEM Cell system input level of -60dBm (corresponds to 220uV/m actual field strength).

The antenna used was a double loop, as shown in Fig. 8.

The peak noise measured at TPLIMX was 3mVpp with the RF carrier switched off.

With the antenna removed and the receiver RF input matched to 50ohms:

- A level of 160mVpp (measured at TPX) was observed for an RF input level of -73dBm, with the RF offset from the local oscillator frequency by 4kHz.
- A level of 60mVpp (measured at TPLIMX) was observed for an RF input level of -99dBm, with the RF offset from the local oscillator frequency by 4kHz.
- The peak noise measured at TPLIMX was 3mVpp with the RF carrier switched off.

Specific points to note on the pcb layout are:

- Careful RF circuitry layout and positioning on the pcb. Special care had to be taken with the ground plane connections of the capacitors directly associated with the antenna circuitry.
- The use of a three layer PCB with the middle layer used exclusively to provide a good continuous RF ground plane.
- The compact LO circuitry layout, short track length of the LO signal lines to the SL6609A LOX and LOY pins and the provision for a full screen over the LO circuitry. The LO circuitry has been powered using the 1V regulator function provided on the SL6609A.
- LNA output load circuitry has been positioned away from the antenna.
- The output track from the SL6609A DATA O/P (Pin 14) is positioned well away from the antenna.
- Special attention to RF decoupling.
- Antenna grounds joined to one ground plane point.

The TEM Cell Sensitivity of the GPS RF demonstration board is antenna limited, therefore using a larger loop area antenna should improve sensitivity.

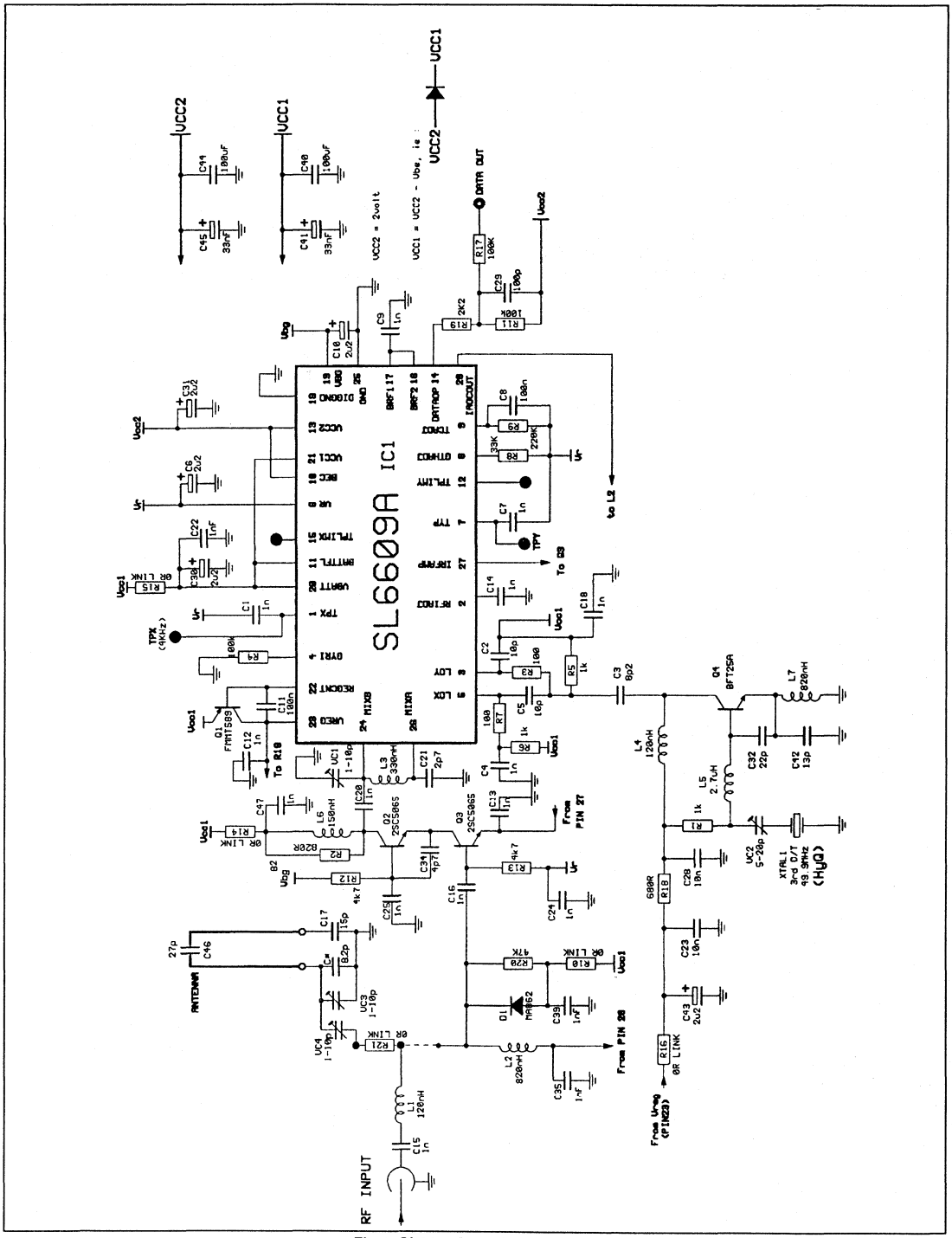


Fig.4: SL6609A application circuit

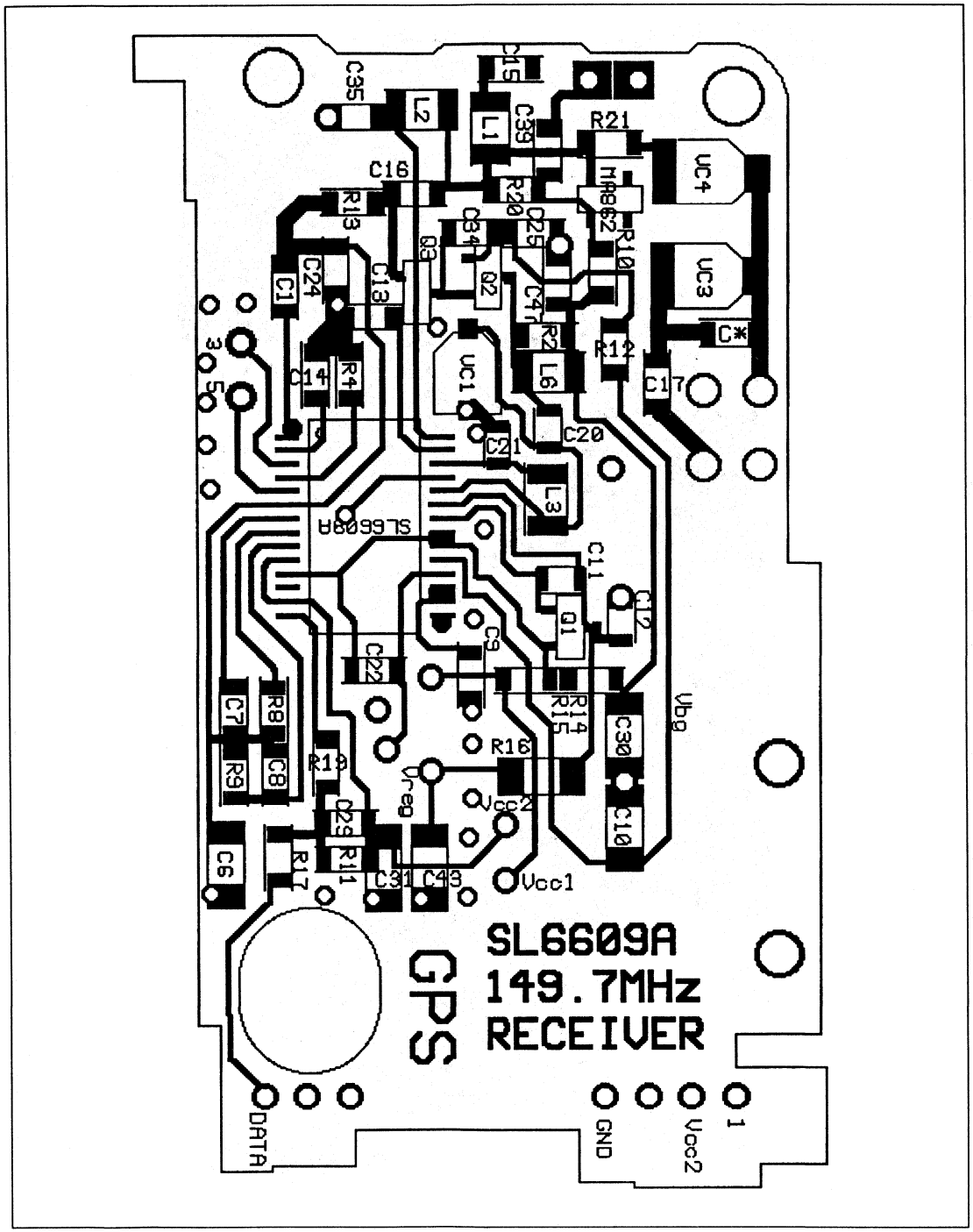


Fig.5: SL6609A application circuit pcb layer 1

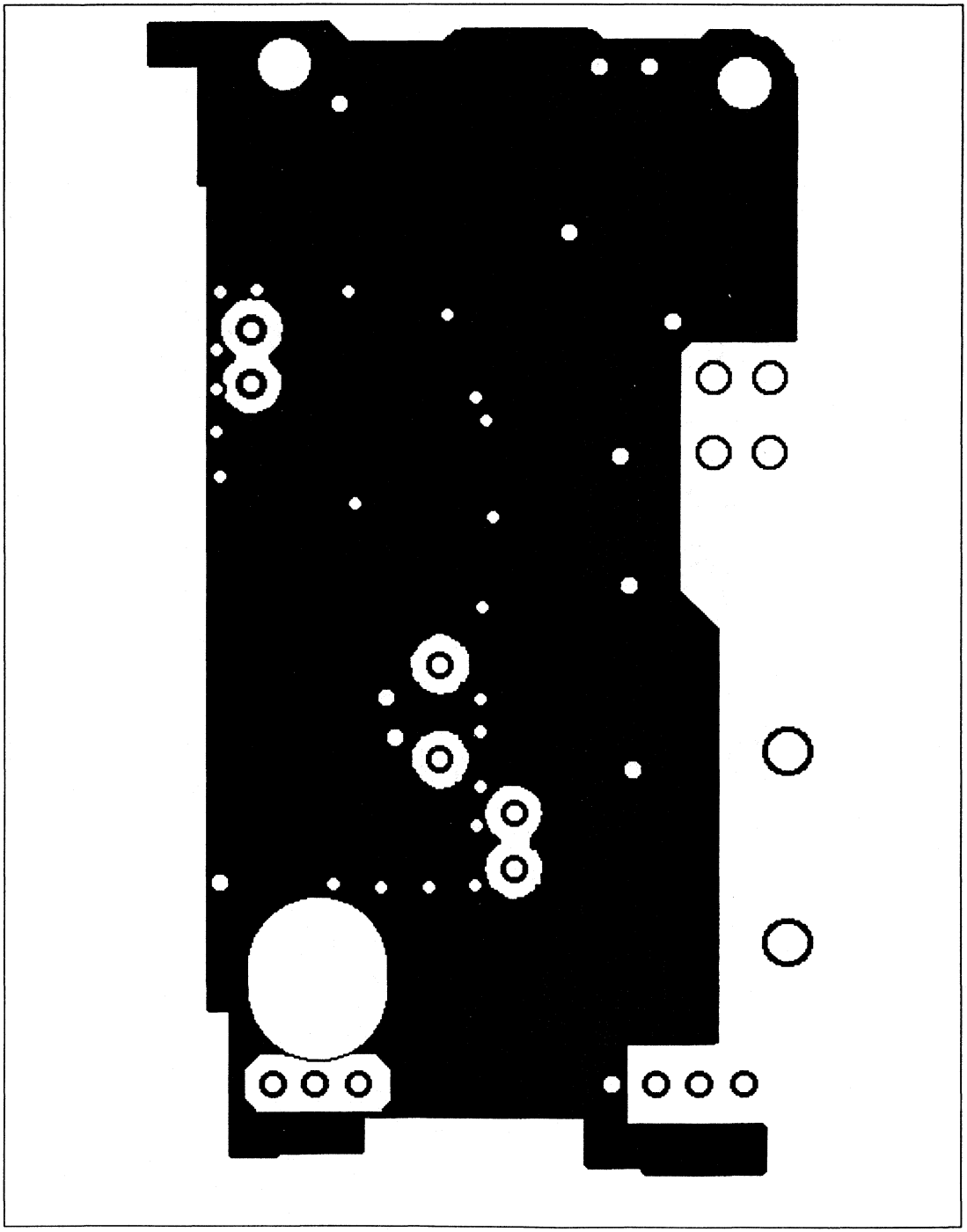


Fig.6: SL6609A application circuit pcb layer 2

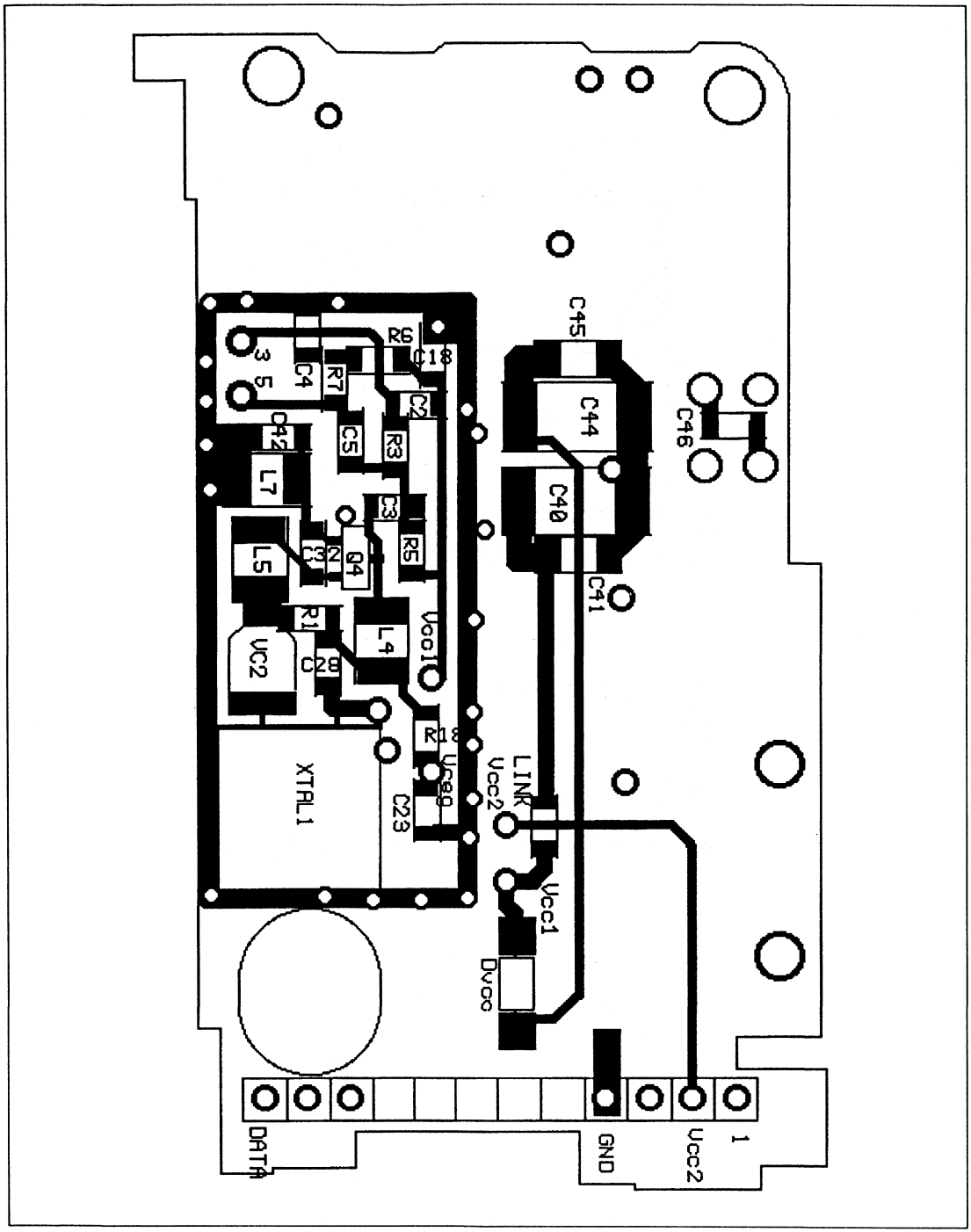


Fig.7: SL6609A application circuit pcb layer 3

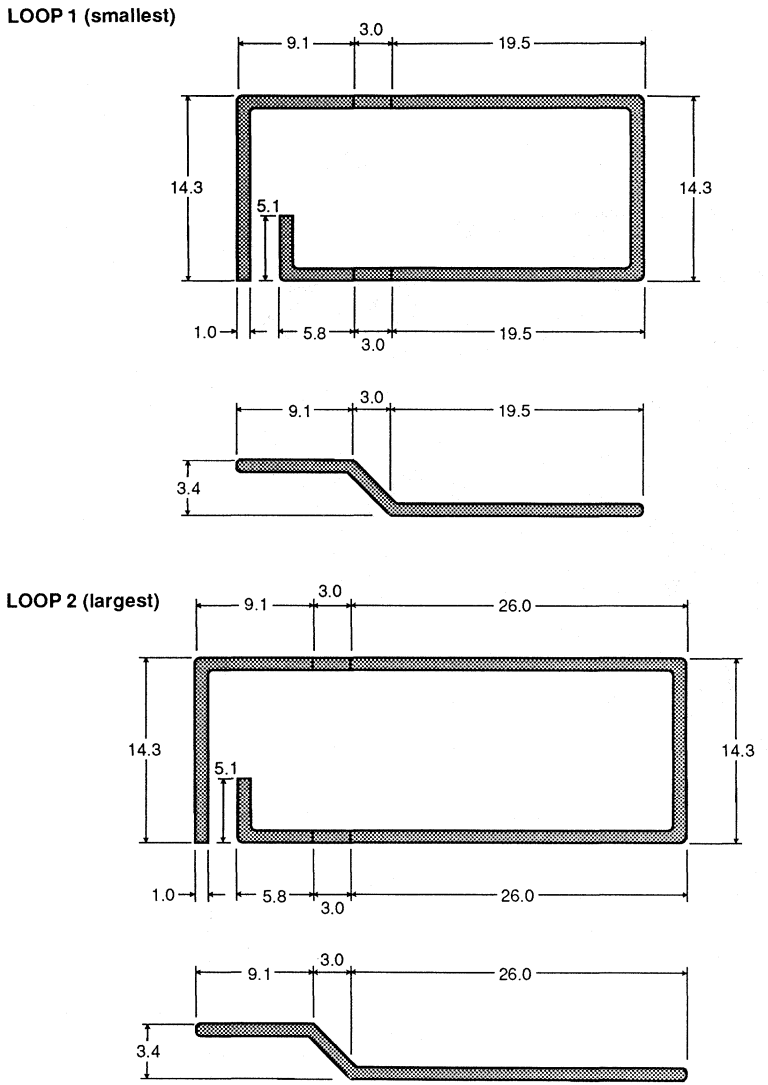


Fig.8 Double wire loop pager antenna.
Dimensions : mm Material : gold plated, hard drawn copper.

PERFORMANCE MEASUREMENTS ON THE SL6609A/SL6610 DEMONSTRATION BOARDS

INTRODUCTION

The objectives of this application note are to:

- Aid understanding of the receiver measurements as listed in the datasheets for SL6609A and SL6610.
- Assist users of the SL6609A/SL6610 demonstration boards when replicating the receiver measurements.

The characterisation analysis performed by GPS was on a large scale and in order to reduce the time required for analysis a bit error rate (BER) meter under IEEE control was used. This differs from the descriptions below which suggest the use of a POCSAG encoder and decoder. A BER of 1 in 30 has been found to be equilvalent to a successful call reception rate of 80% with a POCSAG encoder and decoder.

A test set-up as shown in Fig.1 is recommended. A POCSAG Encoder generates address data that matches the address of the decoder and is at the chosen baud rate (i.e. 512, 1200 or 2400). The data is FM modulated onto an RF Carrier and applied to the demonstration board via the combiner. The detected data output from Pin 14 is passed to the decoder to acknowledge successful call detection by the SL6609A/SL6610. Signal Generators B and C provide the interfering signals required in some measurements.

For all measurements the local oscillator frequency must be the same as the nominal RF carrier frequency used.

SENSITIVITY

Definition

The Sensitivity is the minimum power that is sufficient to produce successful call reception at the defined rate of 80%. It is a measure of the lowest signal strength the SL6609A/SL6610 is capable of working with.

Measurement

Signal Generator A is programmed to provide an RF signal equal to the nominal frequency of the demonstration board (usually around 153MHz, 282MHz or 470MHz).

Address data from the POCSAG Encoder is DC FM modulated onto the RF signal from Signal Generator A (i.e. external modulation) with a 4.5kHz ΔF for 512 baud or 4kHz ΔF for 1200 baud.

The level of the RF Carrier from Signal Generator A is repeatedly reduced while monitoring the ability of the SL6609A/SL6610 to successfully detect the address data on the RF Carrier.

Note: Signal Generators B and C are not used for this measurement.

The Sensitivity as recorded is the minimum RF Carrier level at the input to the Low Noise Amplifier of the demonstration board which permits the 80% rate of successful data detection to be maintained. The value is used as the Reference Sensitivity Threshold for subsequent measurements.

ADJACENT CHANNEL REJECTION

Definition

The Adjacent Channel Rejection measurement establishes the capability of the SL6609A/SL6610 to operate at the 80% rate of successful call detection when there is an unwanted modulated interfering signal which differs from the wanted signal by a single channel spacing (i.e. 25kHz).

Measurement

The RF Carrier from Signal Generator A remains at the nominal frequency of the demonstration board but has the level adjusted to the Reference Sensitivity Threshold plus 3dB. This is known as the wanted signal.

Signal Generator B provides the interfering signal and is set to a frequency one channel spacing (i.e. 25kHz) below the RF Carrier and has sinusoidal FM modulation of 400Hz at 3kHz ΔF generated internally.

The level of the interfering signal is adjusted to reach the maximum at which the 80% rate of successful call detection can be maintained.

Note: Signal Generator C is not used for this measurement.

The recorded Adjacent Channel Rejection is the difference in dBs between the wanted and interfering signal levels i.e. the difference between the Reference Sensitivity Threshold plus 3dB and the interfering signal level at the RF signal input to the Low Noise Amplifier.

THIRD ORDER INTERMODULATION PRODUCT REJECTION PERFORMANCE (IP3)

Definition

The IP3 measurement establishes the capability of the SL6609A/SL6610 to operate when there are two interfering signals such that the 3rd order product is at a frequency equal to the wanted signal.

Measurement

The RF Carrier from Signal Generator A remains at the nominal frequency of the demonstration board but has the level adjusted to the Reference Sensitivity Threshold plus 3dB. This is known as the wanted signal.

Signal Generator B provides the first interfering signal and is set to a frequency one channel (i.e. 25kHz) below the RF Carrier. This signal is unmodulated.

Signal Generator C provides a second interfering signal and is set to a frequency two channels (i.e. 50kHz) below the RF Carrier. Sinusoidal FM modulation of 400Hz at 3kHz ΔF is applied to this signal.

Signal generators B and C are set to the same RF output level but are then adjusted simultaneously to reach the maximum at which the 80% rate of successful call detection can still be maintained.

The recorded IP3 is the difference in dBs between the wanted and interfering signal levels at the RF signal input to the Low Noise Amplifier (i.e. the difference between the Reference Sensitivity Threshold plus 3dB and the interfering signal levels).

SECOND ORDER INTERMODULATION PRODUCT REJECTION PERFORMANCE (IP2).

Definition

The IP2 measurement establishes the capability of the SL6609A/SL6610 to operate in the presence of two interfering RF signals, not within the wanted signal channel. The two interfering RF signals are separated in frequency by a spacing that corresponds to a frequency within the SL6609A/SL6610 baseband bandwidth (e.g. a frequency separation of 4kHz).

Measurement

The RF Carrier from Signal Generator A remains at the nominal frequency of the demonstration board but has the level adjusted to the Reference Sensitivity Threshold plus 3dB. This is known as the wanted signal.

Signal Generator B provides the first interfering signal and is set to a frequency one channel minus $\Delta F/2$ below the RF Carrier. This signal is unmodulated.

Signal Generator C provides a second interfering signal and is set to a frequency one channel plus $\Delta F/2$ below the RF Carrier. Sinusoidal FM modulation of 400Hz at 3kHz ΔF is applied to this signal.

For example, assuming a Channel spacing of 25kHz, and a ΔF of 4kHz:

- signal generator B will be set to:
  Nominal Frequency - 23kHz

- signal generator C will be set to:
  Nominal Frequency - 27kHz

Interfering Signal Generators B and C are set to the same RF output level. The level of both interfering signals is then adjusted simultaneously to reach the maximum at which the 80% rate of successful call detection can still be maintained.

The recorded IP2 is the difference in dBs between the wanted and unwanted interfering signal levels at the Low Noise Amplifier input (i.e. the difference between the Reference Sensitivity Threshold plus 3dB and the interfering signal levels).

CENTRE FREQUENCY ACCEPTANCE

Definition

The Centre Frequency Acceptance identifies the maximum tolerable frequency offset from the nominal RF Carrier frequency that can be experienced before a 3dB degradation in sensitivity is seen.

Measurement

The RF Carrier from Signal Generator A is set to the nominal frequency of the demonstration board and has the level adjusted to the Reference Sensitivity Threshold plus 3dB.

The frequency of Signal Generator A is adjusted higher and then lower to reach the limits about the nominal RF Carrier frequency at which the 80% rate of successful call detection can still be maintained.

Note: Signal generators B and C are not used for this measurement.

The centre frequency acceptance 'above' is defined as the highest frequency reached minus the nominal RF carrier frequency.

The centre frequency acceptance 'below' is defined as the nominal RF carrier frequency minus the lowest frequency reached.

The recorded centre frequency acceptance is the average of the centre frequency acceptance 'above' and 'below' measurement results.

DEVIATION ACCEPTANCE

Definition

Deviation Acceptance indicates the maximum tolerable offset from the nominal deviation frequency of the RF Carrier FM modulation that can be experienced before a 3dB degradation in sensitivity is seen.

Measurement

The RF Carrier from Signal Generator A remains at the nominal frequency of the demonstration board but has the level adjusted to the Reference Sensitivity Threshold plus 3dB.

The ΔF of Signal Generator A is modified from the nominal (i.e. 4.5kHz at 512 baud, 4kHz at 1200 baud) to reach the maximum difference at which the 80% rate of successful call detection can still be maintained.

The measurement is performed for ΔF varied both above and below the nominal deviation frequency.

Note: Signal Generators B and C are not used for this measurement.

The deviation acceptance 'up' is defined as the highest deviation frequency reached minus the nominal deviation frequency.

The deviation acceptance 'down' is defined as the nominal deviation frequency minus the lowest deviation frequency reached.

LARGE SIGNAL IP3

Definition

This is an extension to the standard IP3 test, with measurements being made starting at sensitivity and continuing to wanted signal levels well above sensitivity. The measurement assesses the large signal intermodulation performance of the device.

Measurement

Large signal IP3 is measured with the same set-up and technique as the standard IP3 test. However, as well as being measured at 3dB above sensitivity, the IP3 is assessed at 5dB steps up from this to a wanted signal level of approx -40dBm. The calculation for large signal IP3 is interferer level minus wanted level at the Low Noise Amplifier.

The results of this measurement are shown for a typical device in Fig.11 in the SL6609A/SL6610 datasheet. The graph shows a continous roll-off of large signal IP3 verses wanted signal (refer to AGC OFF graph).

The AGC ON graph depicts the large signal IP3 performance that can be obtained by employing the AGC function. This circuit monitors the wanted signal level and effectively holds it constant at approximately -95dBm at the RF input by use of a PIN diode in the Low Noise Amplifier. This has the affect of holding up the large signal IP3 at approximately 40dB for an input range of -93 to -60dBm. Beyond that, the PIN diode runs out of attenuation range and the large signal IP3 begins to drop again.

LOCAL OSCILLATOR (LO) REJECTION

Definition

The LO Rejection indicates the maximum local oscillator level at the Low Noise Amplifier input that can be tolerated before a specified degradation in sensitivity is seen.

Note: This measurement is difficult to undertake on the GPS Demonstration Board. It was performed during characterisation analysis and is listed in the data sheet.

Measurement (GPS Characterisation Analysis Only)

The Local Oscillator signal was split to provide the original Local Oscillator signal and a signal to be combined with the wanted RF Carrier via a variable phase shift network and variable attenuator.

The RF Carrier from Signal Generator A remained at the nominal frequency of the demonstration board but the level was adjusted to the Reference Sensitivity Threshold plus a specified level; either 0.5dB or 3dB (the shifts as listed in the data sheet).

The variable phase shift network was adjusted to cause maximum receiver degradation and then the level of the Local Oscillator combined with the wanted RF Carrier was adjusted, using the variable attenuator, to reach the maximum at which the 80% rate of successful call detection could still be maintained.

Note: The Local Oscillator signal applied to the device local oscillator input pins (LOX and LOY) was kept at a constant level. Signal generators B and C were not used for this measurement.

The measurement as recorded is the level of the Local Oscillator signal at the RF Input to the Low Noise Amplifier and is recorded against the degradation from the Reference Sensitivity Threshold (i.e. 0.5dB or 3dB).

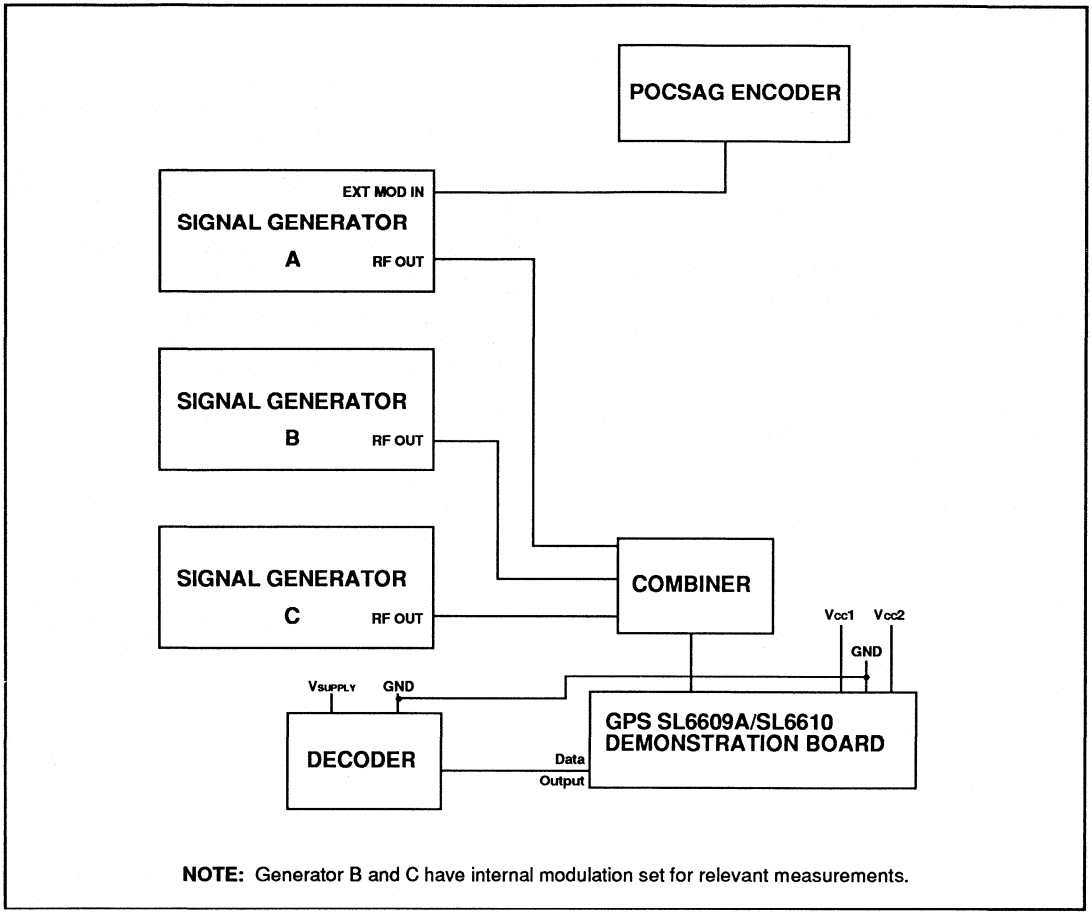


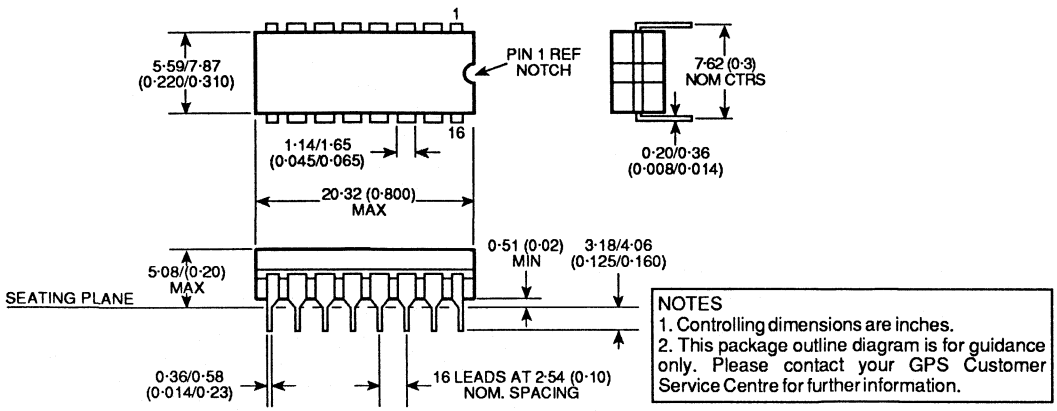
Fig. 1 Suggested Test Set-up

Section 12
Package Outlines

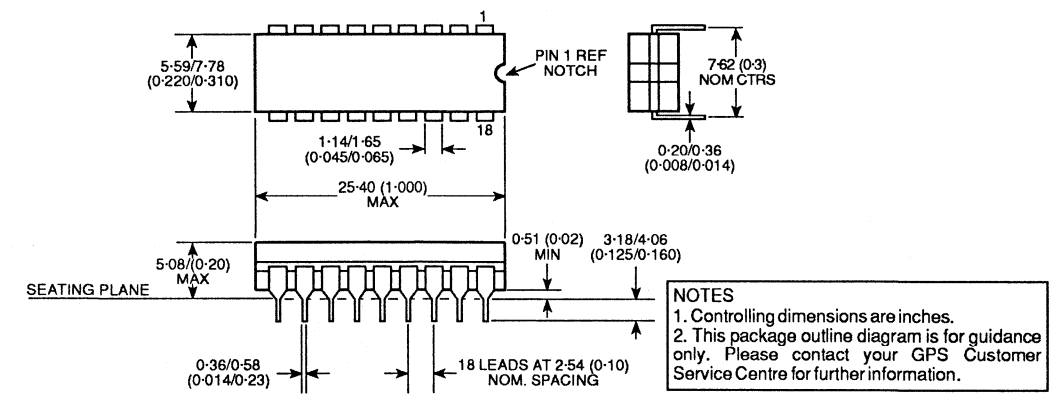
NOTES

1. Dimensions are shown thus: mm (in).
2. Unless otherwise indicated, controlling dimensions are in inches.
3. All package outline diagrams are for guidance only. Please contact your nearest GPS Customer Service Centre for further information.

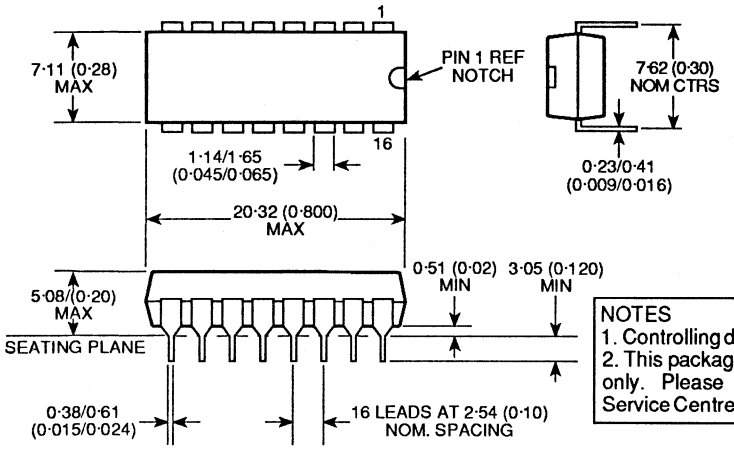
GEC PLESSEY
SEMICONDUCTORS



16-LEAD CERAMIC DIL - DG16

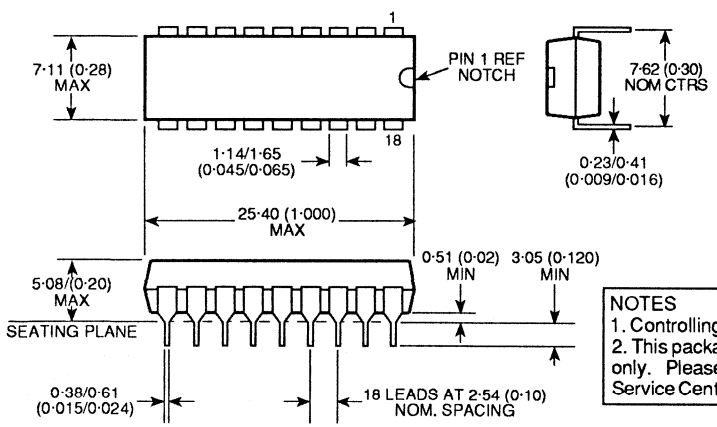


18-LEAD CERAMIC DIL - DG18



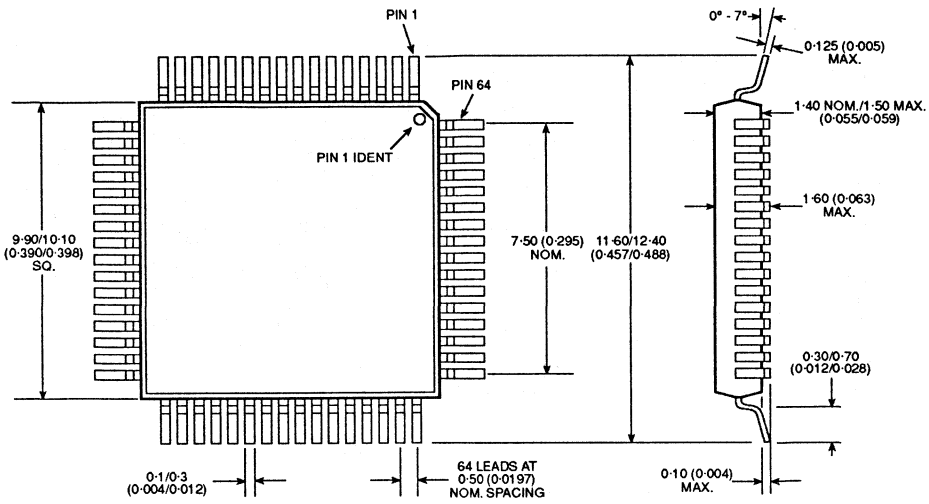
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

16-LEAD PLASTIC DIL - DP16



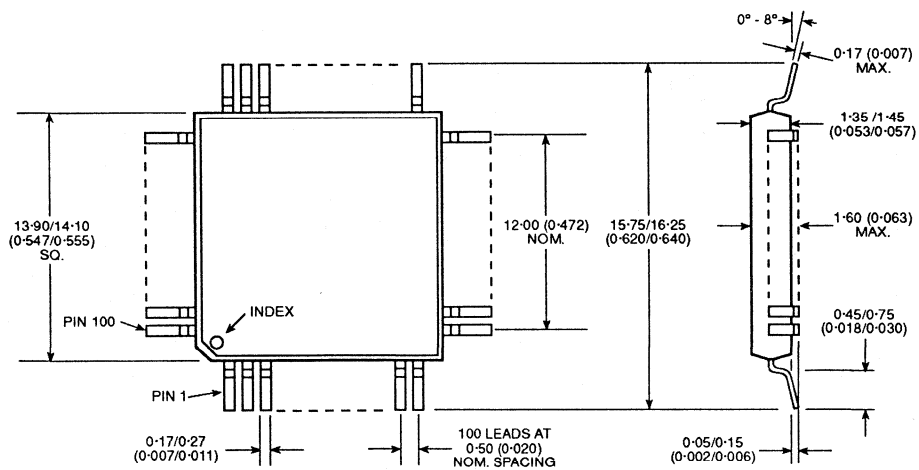
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

18-LEAD PLASTIC DIL - DP18



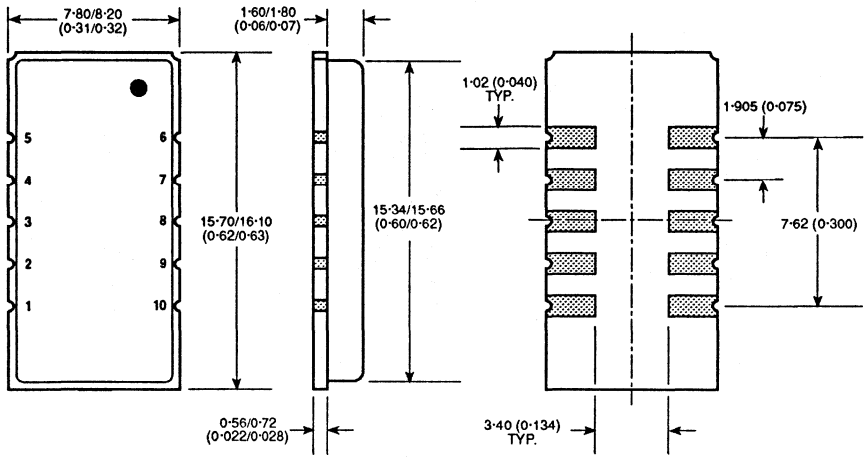
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

64-LEAD FINE PITCH PLASTIC QUAD FLATPACK – FP64



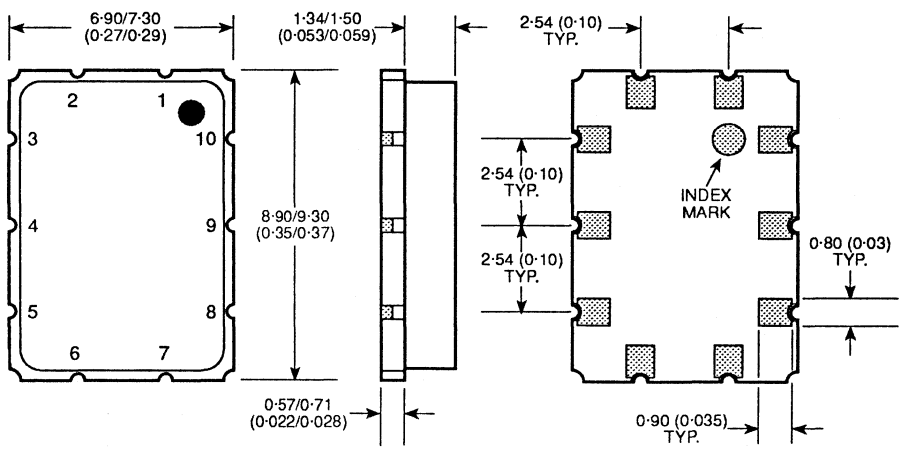
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

100-LEAD FINE PITCH PLASTIC QUAD FLATPACK – FPD100



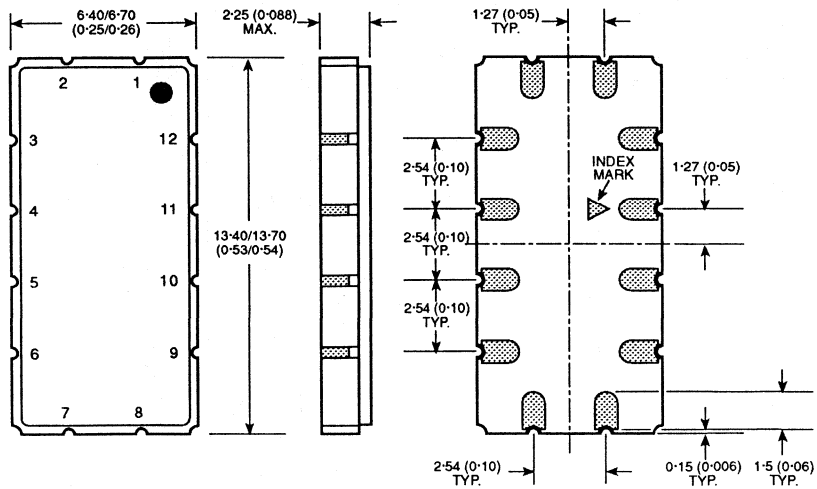
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

10-PAD LEADLESS CHIP CARRIER (SLAM) - LCS10/1



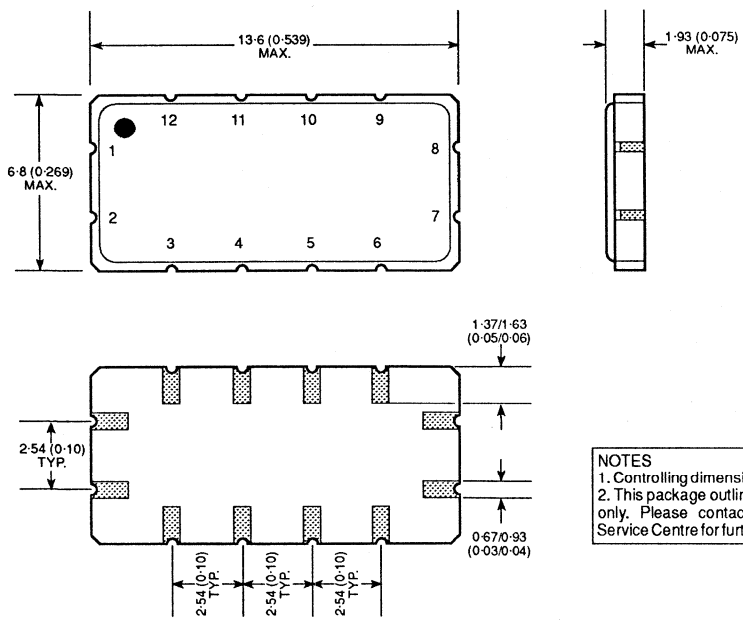
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

10-PAD LEADLESS CHIP CARRIER (SLAM) - LCS10/2



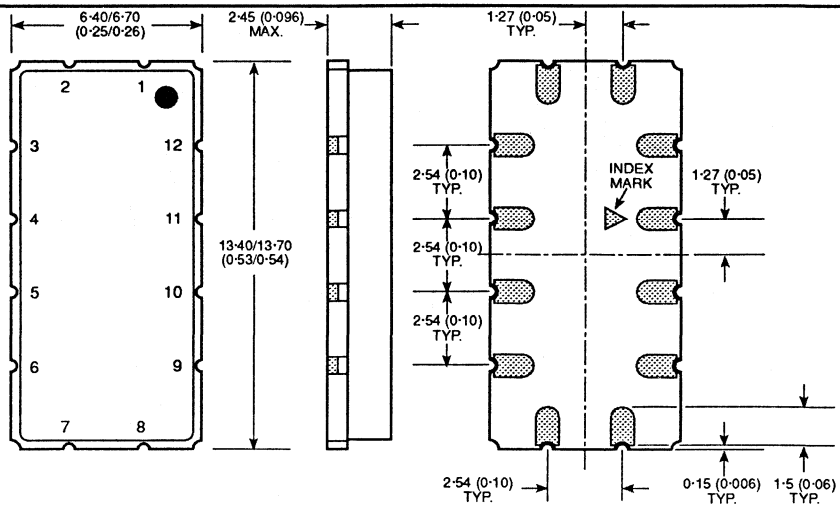
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

12-PAD LEADLESS CHIP CARRIER (SEAM SEAL) - LCS12/1



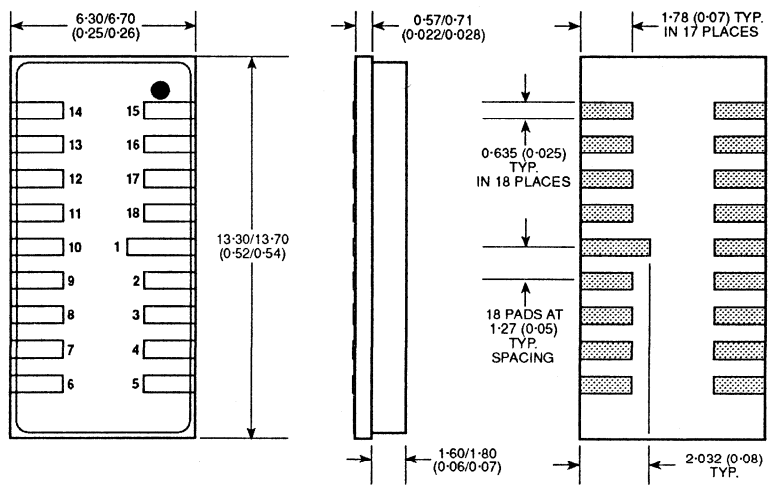
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

12-PAD LEADLESS CHIP CARRIER (SEAM SEAL) - LCS12/2



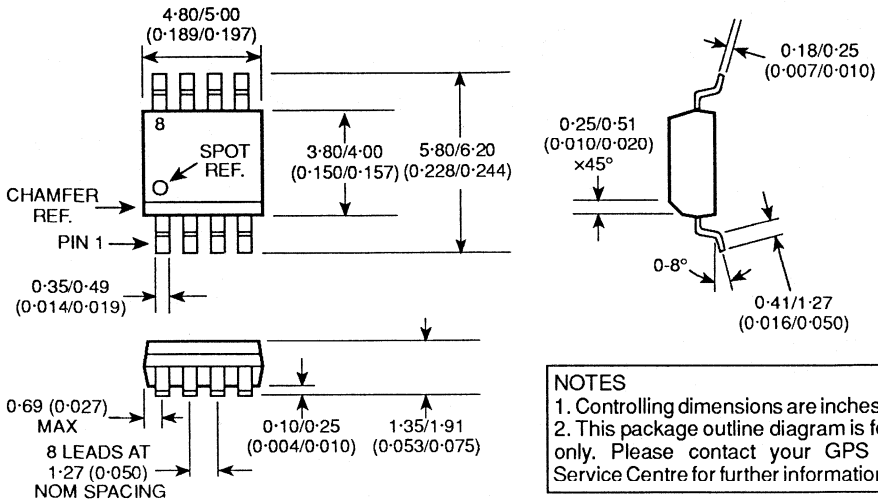
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

12-PAD LEADLESS CHIP CARRIER (SLAM) - LCS12/4



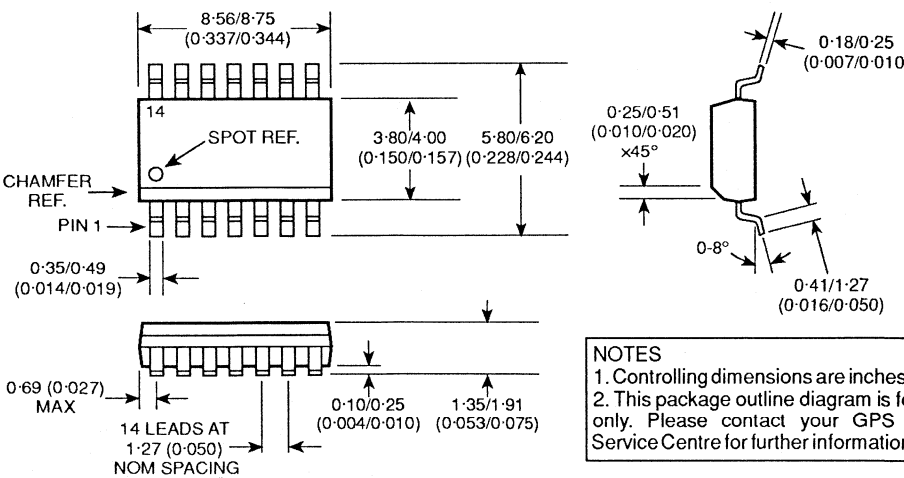
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

18-PAD LEADLESS CHIP CARRIER (SLAM) - LCS18



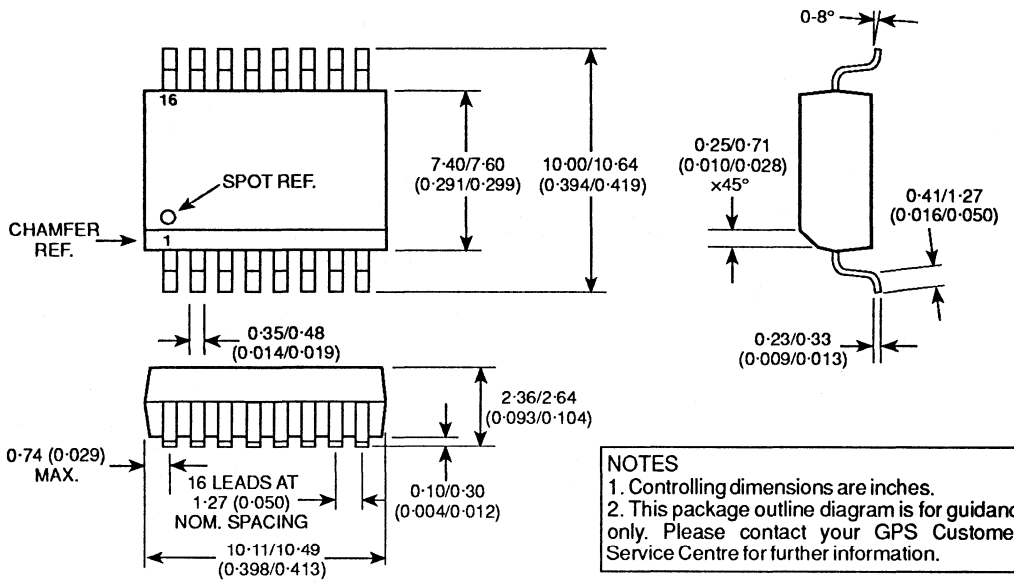
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

8-LEAD MINIATURE PLASTIC DIL - MP8



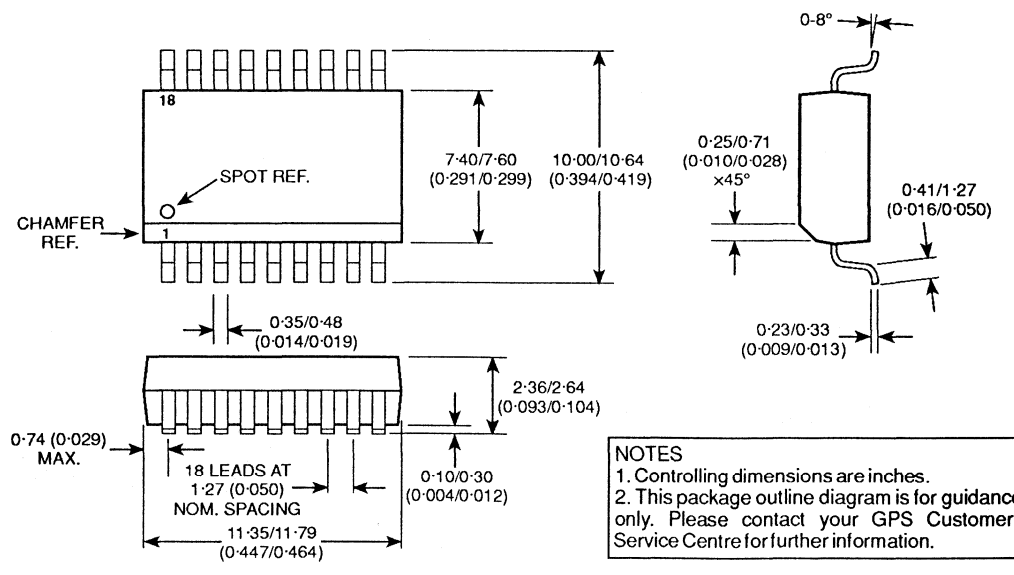
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

14-LEAD MINIATURE PLASTIC DIL - MP14



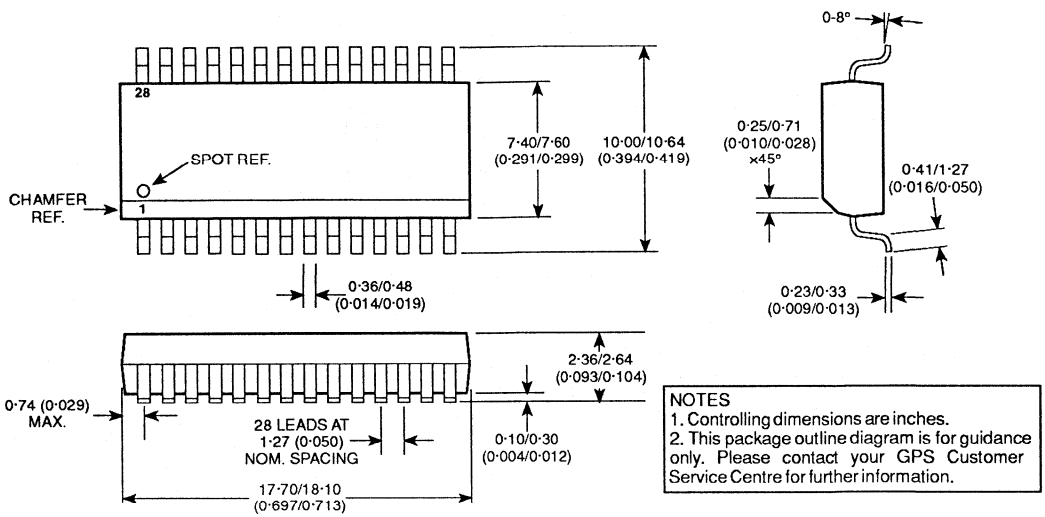
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

16-LEAD MINIATURE PLASTIC DIL(WIDE BODY) - MP16/L



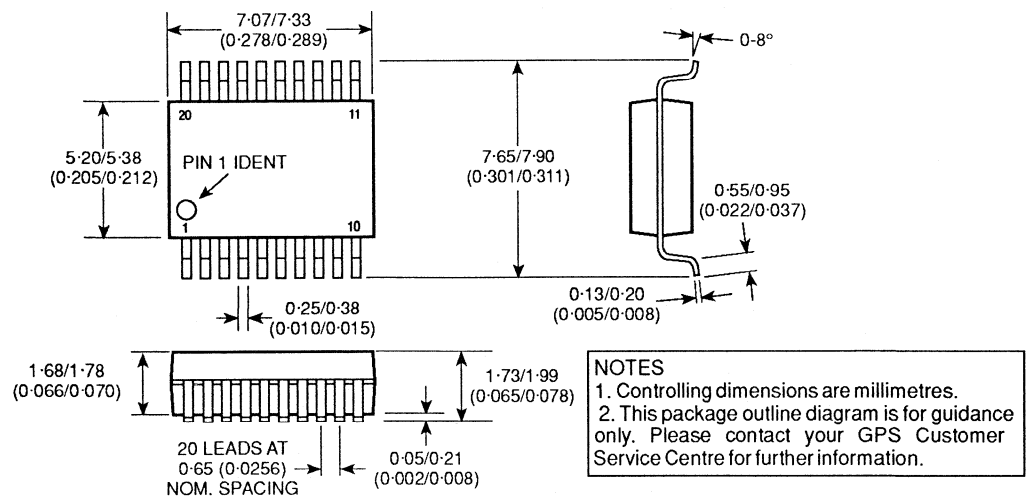
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

18-LEAD MINIATURE PLASTIC DIL - MP18



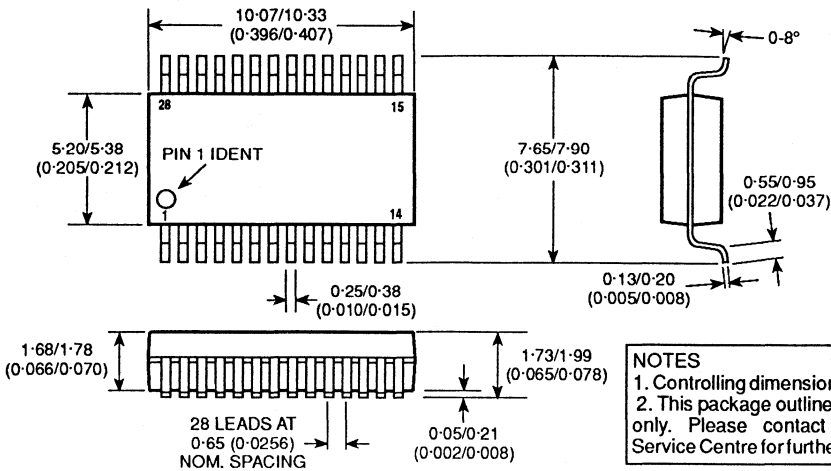
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

28-LEAD MINIATURE PLASTIC DIL - MP28



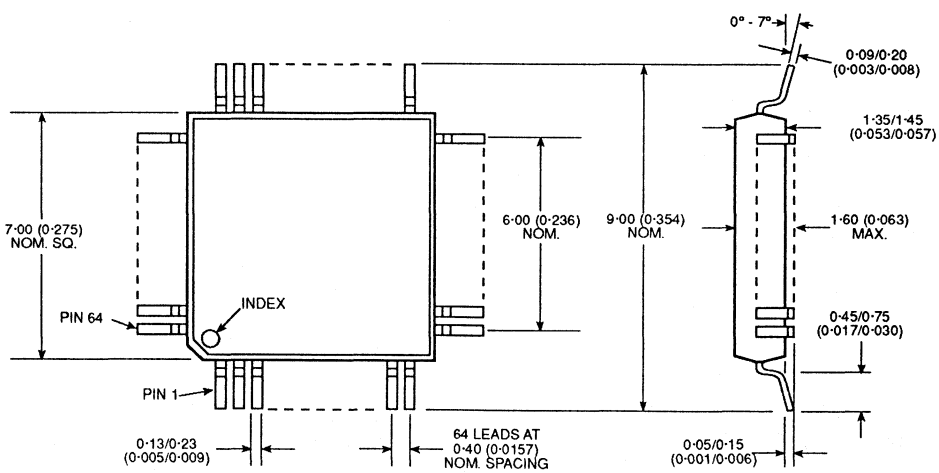
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

20-LEAD SHRUNK MINIATURE PLASTIC DIL (SSOP) - NP20



NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

28-LEAD SHRUNK MINIATURE PLASTIC DIL (SSOP) - NP28



NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

64-LEAD FINE PITCH PLASTIC QUAD FLATPACK – VP64

Section 13
GPS Locations

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MISSOURI	**Lorenz Sales, Inc.,** 10176 Corporate Square Dr., Suite 120, St. Louis, MO 63132. Tel: (314) 997-4558. Fax: (314) 997-5829.
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PUERTO RICO	**American Micro Sales,** La Electronica Bldg, Suite 316, Calle Bori 1608, Urb. Caribe, Rio Piedreas, PR 00927. Tel: (809) 274-1661. Fax: (809) 756-6152.
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	O. & M. Sales, P.O. Box 9384, The Woodlands, TX 77387. Tel: (713) 894-5021. Fax: (713) 894-5022.
WASHINGTON	**Venture Electronics,** P.O. Box 3034, 12503 Bel-Red Road, Suite 101, Bellevue, WA 98005. Tel: (206) 454-4594. Fax: (206) 454-9003.
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Scansupply A/S, Marselisborg Havnevej 36, DK-8000 Aarhus C. Tel: 45 45 82 50 90. Fax: 45 86 12 77 18.

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3 rue Berthelot, 69627 Villeurbanne CEDEX. Tel: 72 35 22 00. Fax: 72 34 67 72.
Z.I. du terroir, rue de l'industrie, 31140 Saint Alban. Tel: 61 37 44 00. Fax: 61 37 44 29.
Parc Club du golf, Batiment 1, 13856 Aix-en-Provence CEDEX 3. Tel: 42 16 77 88 Fax: 42 39 4728.
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